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Article

GaAs Templates Selectively Grown on Silicon-on-Insulator for Lasers in Silicon Photonics

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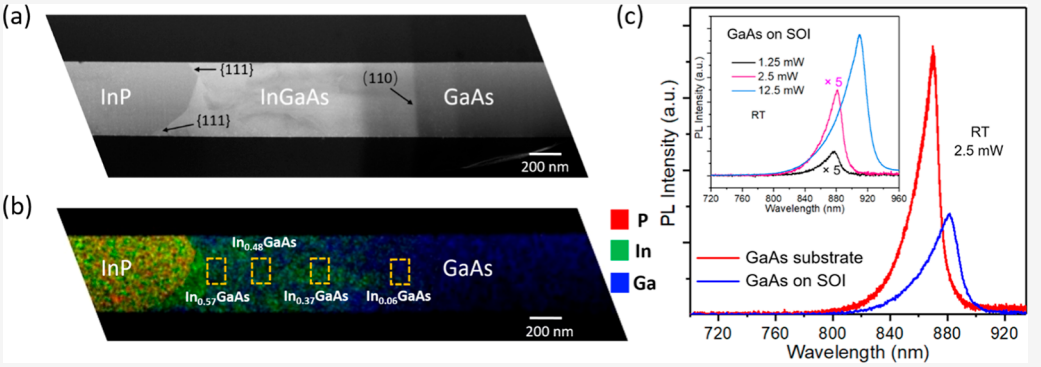

ABSTRACT: Realizing efficient on-chip light sources on Si is a crux for Si-based photonic integrated circuits (PICs). Lateral aspect ratio trapping (LART) by MOCVD for selective epitaxy of III−V materials on (001) silicon-on-insulator (SOI) is a promising technique for monolithic integration of light sources on silicon and deployment of Si-based PICs. In this report, a monolithic microscaled GaAs/Si platform is obtained through the selective growth of GaAs membranes on industry-standard (001)-oriented SOI wafers by the LART technique. The GaAs membranes are laterally grown from {111}-oriented Si surfaces inside patterned oxide trenches, with dimensions defined by lithography. GaAs microdisk lasers (MDLs) fabricated on the GaAs membranes laterally grown on (001) SOI lase at room temperature (RT) by optical pumping. RT-pulsed lasing was achieved with a threshold of 880 μJ/cm^2. This work provides a crucial step toward fully integrated Si photonics.

INTRODUCTION

Si-based photonic integrated circuits (PICs) are desirable for large-capacity data communications due to their superiority on low latencies, low-power consumption, and unprecedentedly high bandwidth compared to the conventional electronic interconnects.[1,2] The numerous applications of PIC, including high-speed communication, quantum technologies, and optical sensing, have attracted rapidly increasing research interest.[3] Integrating III−V materials on Si has been under extensive study in recent years, leveraging the mature CMOS manufacturing capabilities.[4−7] Various light source architectures using heterogeneous integration have been extensively investigated and deployed for Si−PICs with large wafer-scale silicon fabrication facilities.[8−11] Other techniques have also been developed to directly integrate III−V alloys on (001) Si substrates over the past three decades.[12−15] Although high-performance III−V lasers have been successfully monolithically grown on Si wafers by using conventional blanket hetero-epitaxy,[16−18] several-micron-thick buffer layers are needed to reduce the defects such as antiphase boundaries, stacking faults (SFs), and threading dislocations (TDs) resulted from the large lattice mismatch between the III−V materials and Si substrates. Micrometer-thick buffers make it difficult to couple light efficiently between the III−V light sources and the Si-waveguide. Compared to blanket epitaxy, selective hetero-epitaxy eliminating thick buffers and blocking defects using the aspect ratio trapping (ART) technique can be applied in integrated Si-photonics easier.

Optically pumped nanoridge lasers and III−V photo-detectors have been demonstrated on silicon-on-insulator (SOI) wafers using selective heteroepitaxy techniques such as vertical ART and nanoridge engineering.[19−22] However, the small material volume in the high aspect ratio nanometer-scale space makes demonstration of electrically driven devices challenging, and the coupling efficiency is likely to be degraded by the height difference between the III−V active region and Si waveguides. Template-assisted selective epitaxy (TASE) and lateral aspect ratio trapping (LART) are the alternative growth

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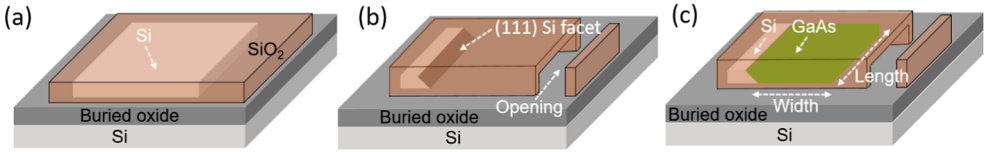

Figure 1. Concept of growing GaAs membranes on (001) SOI wafers. (a) Schematic showing the patterning of the Si layer and oxide deposition. (b) Schematic showing formation of the oxide opening and lateral silicon trench. (c) Laterally grown GaAs membranes inside deep trenches surrounded by oxide.

techniques in selective epitaxy to enable fabrication of photonic devices in lateral configuration.[23,24] These two techniques offer an ideal solution for the monolithic III−V/Si platform with potential efficient light coupling in device designs. While GaAs microdisk lasers (MDLs) emitting at 860 nm have been demonstrated on (001) Si by TASE,[25] the device with dimensions in the deep subwavelength scale limit the device design and future applications.[26] In contrast, LART allows the growth of III−V materials with large dimensions in the same plane as Si[27] and thus makes it promising for efficient coupling between III−V and Si using monolithic integration, which has been demonstrated in our previous work with InP.[28] GaAs is desirable for a wide variety of applications due to its good optical and electronic properties, such as high-saturated electron velocity, high electron mobility, less noise, and high luminous efficiency. Here, we report characteristics of laterally grown GaAs on SOI substrates with two different structural designs. With the optimized growth structure, we demonstrate GaAs MDLs fabricated on SOI substrates. Room temperature (RT)-pulsed lasing of GaAs MDLs was achieved with a threshold of 880 $\mu J/cm^2$.

EXPERIMENTAL SECTION

The materials studied in this report were grown in an AIXTRON closed couple showerhead metal−organic chemical vapor deposition system, using triethylgallium (TEGa), trimethylgallium (TMGa), trimethylindium (TMIn), tertiarybutylarsine (TBA), and tertiarybutylphosphine (TBP) as precursors and a growth pressure of 50 mbar. GaAs was grown in predefined oxide trenches on commercial SOI wafers by photolithography using deposited oxide mask and Si layer wet etching. Figure 1 schematically shows the selective epitaxy of site-controlled and in-plane GaAs membranes grown on (001)-oriented SOI wafers. Lateral trenches in the silicon device layer with a width of 7 μm and a height of 480 nm were formed on the commercial SOI wafers. The detailed fabrication process of the SOI templates for large-area selective growth has been described in our previous publication.[24] The 55° angle between the {111} and {001} Si facets was formed after wet etching with the {111} facet exposed as the growth front.

In our first growth structure, a three-step growth procedure was adopted for the lateral growth of GaAs seeded on the etched Si facets. Prior to the growth, thermal annealing was carried out at 810 °C in H_2 ambient for 16 min to remove the residual oxide at the Si surfaces. TBA preflow was introduced into the reactor before GaAs nucleation to create As-terminated {111} Si facets to ease the GaAs nucleation. Afterward, a thin nucleation layer of GaAs was deposited first at 400 °C on the etched (111) Si surfaces with a V/III ratio of 84, followed by the growth of GaAs at 500 °C. The reactor temperature was then ramped to 600 °C for the GaAs main layer growth, as schematically depicted in Figure 2a. Figure 2b illustrates the optical microscopy images of the 2 and 5 μm-long GaAs segments grown on SOI using the LART. GaAs segment arrays with different lengths were obtained by patterning the Si layer with standard lithography during the fabrication of the SOI templates.

The crystalline quality of the GaAs membranes was investigated by transmission electron microscopy (TEM) characterization. The TEM

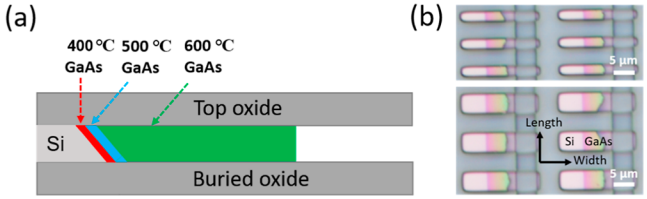

Figure 2. (a) Schematic of the GaAs membranes grown inside oxide trenches using the LART technique. (b) Optical microscopy images of as-grown GaAs segment arrays with two different lengths of 2 and 5 μm, respectively.

lamellae were prepared using focus-ion-beam milling. Cross-sectional TEM investigations were performed on a longer GaAs segment with a patterned length of 5 μm. Figure 3a displays a representative global-

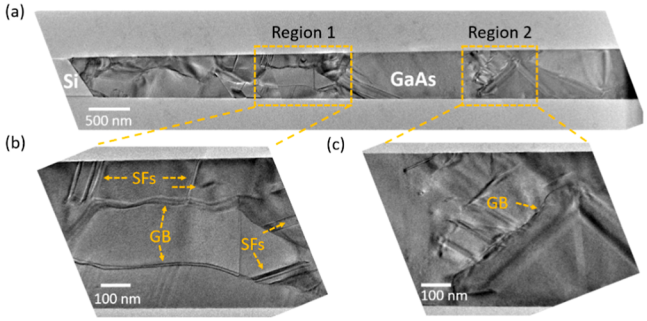

Figure 3. (a) Cross-sectional TEM image of the GaAs segment (width: 7 μm, length: 5 μm) grown on SOI. (b,c) Zoomed-in TEM images for region 1 and region 2.

view TEM image of the GaAs segment. The planar defects such as grain boundaries (GBs) and SFs were observed clearly in the epitaxial GaAs sandwiched between the top and the buried oxide layer. The majority of {111}-oriented SFs generated at the GaAs/Si interface could be blocked by the top and buried oxide layers. However, GBs formed at the GaAs/Si interface could propagate along the growth direction and cannot be trapped effectively by oxide trenches. Figure 3b,c shows the zoomed-in TEM images of regions 1 and 2, respectively. GBs are essentially transition regions where the crystal structure of GaAs changes abruptly and contain a high density of coincident lattice sites. Furthermore, coherent boundaries can interact with one another to produce new boundaries.[29] SFs are disruptions or deviations from the ideal crystal lattice structure and can be influenced by the local atomic arrangement. Thus, SFs running parallel to the {111} planes are more likely to form and cluster in the GB regions in epitaxial GaAs. The presence of GBs can adversely affect the electrical and optical properties of the grown GaAs. To minimize the impact of GBs on device performance, growth conditions must be optimized to eliminate GBs along the growth direction.

In our laboratory, we have obtained dislocation-free InP membranes selectively grown on SOI by LART.[30,31] To grow larger GaAs membranes without GB, we used a second structure, as shown in Figure 4a. A thin InP nucleation layer was first deposited on the

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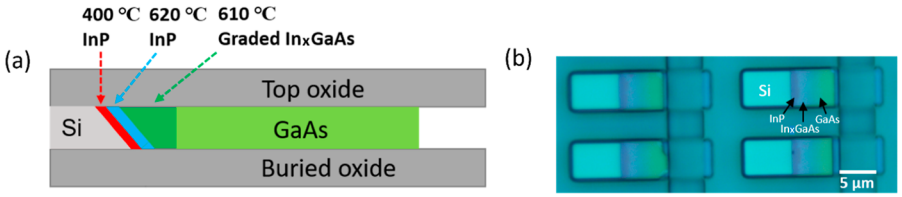

Figure 4. (a) Schematic of the III−V segments grown inside oxide trenches using InP and In_xGaAs intermediate layers. (b) Top-view optical microscopy image of as-grown InP/In_xGaAs/GaAs segment arrays with a patterned length of 5 μm.

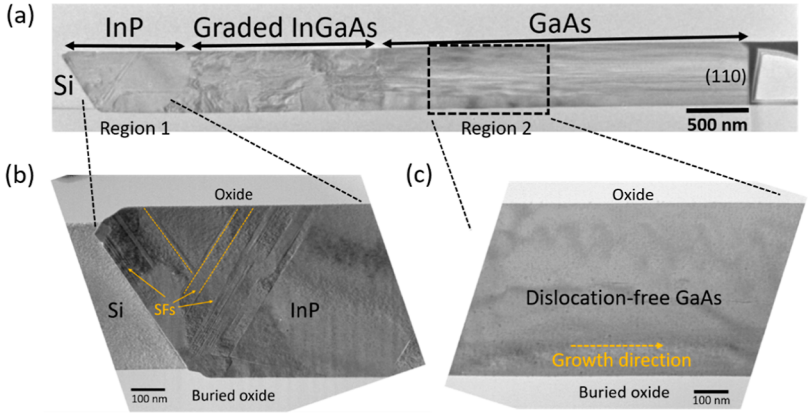

Figure 5. (a) X-TEM image of the GaAs segment with InP and In_xGaAs intermediate layer grown on SOI. Zoomed-in X-TEM images of (b) InP buffer and (c) the GaAs portion in the InP/InxGaAs/GaAs membrane grown after the In_xGaAs intermediate layer.

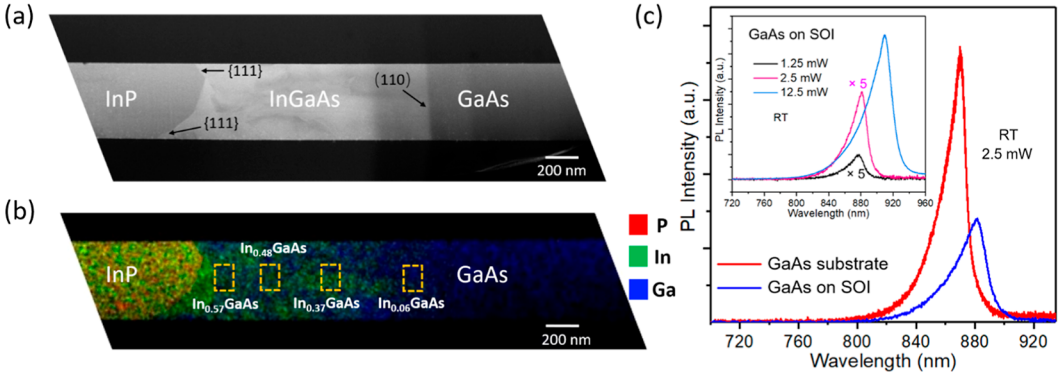

Figure 6. (a) STEM image of the interfaces of InP/In_xGaAs and In_xGaAs/GaAs and (b) EDS results for the composition of phosphorus, indium, and gallium at different regions in graded In_xGaAs. (c) μPL spectra of the GaAs on SOI and SI-GaAs substrate. Inset: power-dependent PL spectra of GaAs on SOI.

(111) Si surface at 400 °C, followed by an InP layer grown at 620 °C, and the growth details of the InP are described in ref 27. Then, graded In_xGaAs was grown at 610 °C in oxide trenches. The designed InP and In_xGaAs widths are 1 and 1.5 μm, respectively. Finally, main GaAs with a designed width of 4 μm was deposited to add tolerance to device fabrication. The as-grown III−V membranes have good uniformity and sufficient width of GaAs for device fabrication, as evidenced in the top-view optical microscopy image of the InP/In_xGaAs/GaAs segment arrays with a patterned length of 5 μm in Figure 4b.

The crystalline quality of the as-grown III−V membranes along the lateral growth direction was further investigated by cross-sectional TEM (X-TEM), as illustrated in Figure 5a. Figure 5b,c shows zoomed-in X-TEM images of the InP and GaAs portions in the InP/In_xGaAs/GaAs membrane, respectively. SFs formed at the InP/Si interface can be attributed to the relaxation of large strain caused by the large lattice mismatch between Si and InP and terminated at the top and the buried oxide layers. In the laterally grown InP, In_xGaAs, and GaAs, no TDs or GBs were observed, except for a few SFs found exclusively in the InP. The growth front of the InP membrane gradually changes as growth proceeded along the trench direction. Originally, the growth front of the InP follows the etched {111}-oriented Si facet. As the epitaxy continues, the growth front gradually changes into a multifaceted surface and varies along the oxide trenches as evidenced in ref 32. The diffusion difference between indium and phosphorus atoms during the epitaxy may give rise to the variation of growth conditions in the different facets.

Figure 6a shows a representative global-view scanning TEM (STEM) image of the specific segment with InP, graded In_xGaAs, and GaAs, clearly showing the sharp interface of InP/In_xGaAs. The end facets of InP consist of three different components: two {111} facets formed near the oxide layer and a higher order transitional facet. The growth front of the laterally graded In_xGaAs changes from a multifaceted surface to the (110) facet, which could be attributed to the deposition preference on different facets for minimizing the total surface energy.[33] Figure 6b illustrates the energy dispersive spectroscopy (EDS) characterization for the corresponding segment shown in Figure 6a. Four different regions were intentionally chosen to analyze the composition of the indium and gallium. Initially, the indium composition was 57% near the InP/In_xGaAs interface and

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decreased to 37%, then to only 6% close to the GaAs/In_xGaAs interface. The strain induced by the lattice mismatch between InP and GaAs could be relaxed by graded In_xGaAs. The indium composition has a distinct contrast in different regions near the InP/In_xGaAs interface. We ascribe the variation in indium composition near the InP/In_xGaAs interface to the nonuniform deposition of In_xGaAs at the start of the growth of graded In_xGaAs.

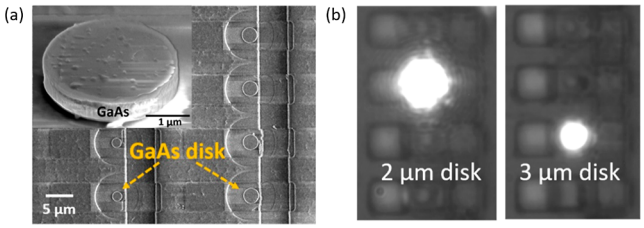

Figure 7. (a) Top-view SEM image of fabricated GaAs MDLs (diameter: 2 and 3 μm) on SOI. (b) Emission images of MDLs above threshold.

Microphotoluminescence (μPL) measurements under the excitation of a 514 nm diode laser with a ~2 μm diameter spot were carried out. The spectra of the as-grown GaAs on SOI and a semi-insulating (Supporting Information) GaAs substrate for reference are presented in Figure 6c. The GaAs wafer exhibits a peak wavelength of 869 nm and a full width at half-maximum (fwhm) of 17 nm, while the peak wavelength of the GaAs grown on the SOI locates at 881 nm with a fwhm of 25.5 nm, presumably a result of incorporated impurities and residual strain caused by lattice mismatch.[32] Power-dependent spectra of GaAs on the SOI are shown in the inset of Figure 6c. Under a high excitation of 12.5 mW, the PL peak of GaAs on SOI red shifts to 909 nm with an extended fwhm of 34 nm. The peak energy and band gap of the PL spectra of carbon-doped GaAs could shift to lower energy with increasing temperature.[34] The red shift and broadening of the emission spectra under high pumping power could be ascribed to the thermal shifts of the band gap in GaAs.

DEVICE RESULTS AND DISCUSSION

The as-grown optimized structure was fabricated into GaAs MDLs with a diameter of 2 and 3 μm to illustrate the quality of the laterally grown GaAs. Dry etching was first adopted to thin the top oxide. The position and contours of MDLs were defined by E-beam lithography and oxide etching steps, respectively. Subsequently, cylindrical pillars were formed by inductively coupled plasma (ICP) etching. The fabricated MDLs were pumped by a mode-locked Ti/Sapphire laser (750 nm, 100 fs pulses, and a repetition rate of 76 MHz) with a spot diameter of ~2 μm. Figure 7a displays the top-view SEM image of the fabricated GaAs MDL arrays on the SOI with circular cavities in a global view. The inset in Figure 7a shows the tilted-view SEM image of a fabricated air-cladding MDL with circular cavity (3 μm-diameter). The surface roughness of the disk could be further improved to minimize the optical loss resulting from light scattering at the microdisk surface. Wan et al. have investigated the impact of etching parameters on the sidewall roughness and obtained a smooth sidewall on MDLs.[35] Experiments to recover our previous parameters are ongoing. Figure 7b shows the recorded images of the representative MDL lasing above the threshold, with the obvious brightness and coherent emission observed.

Figure 8a presents representative RT-PL spectra of an MDL with a diameter of 2 μm. Under low pump power, spontaneous emission was exhibited by broad PL emission. Above threshold, the transition from spontaneous to stimulated emission was verified by a peak at 900 nm with a line width of 3 nm. The light−light (L−L) curve and the evolution of the line width of the corresponding MDL are plotted in Figure 8c. The evident "kink" in L−L curve together with a clear drop of the line width near the threshold indicates the lasing behavior of MDL at RT, and the threshold is extracted to be around 880

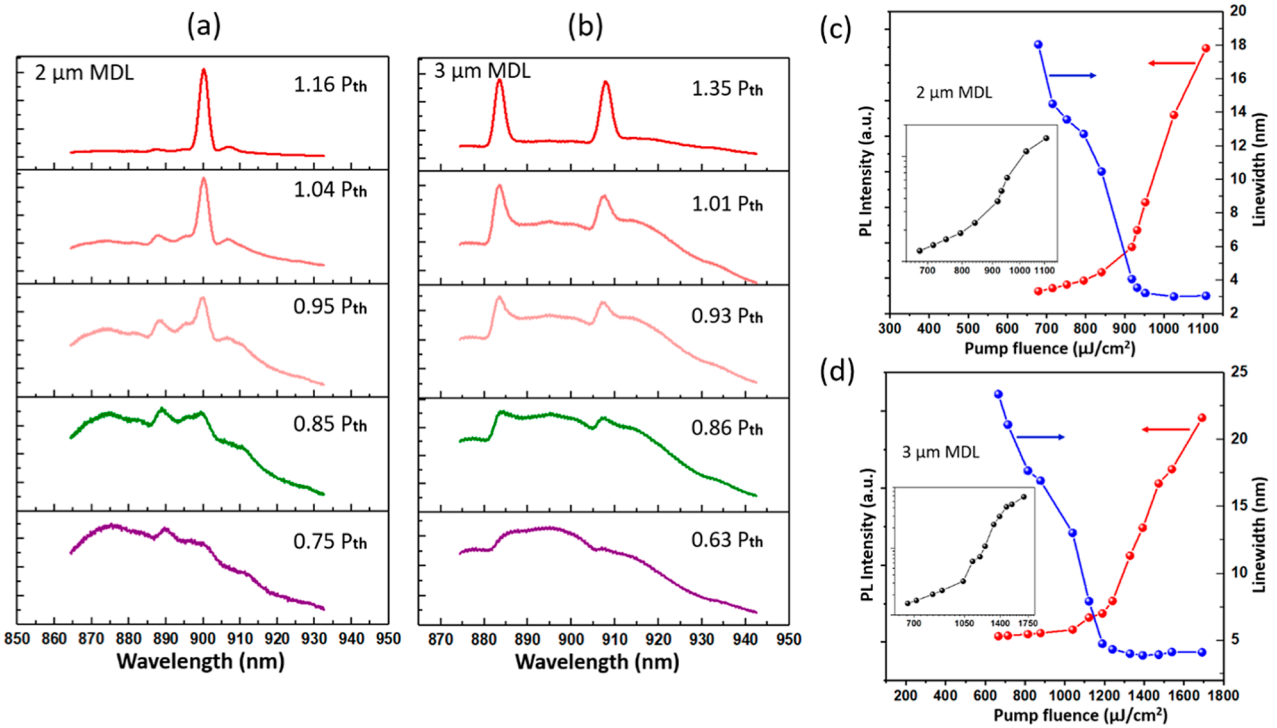

Figure 8. RT power-dependent PL spectra of MDLs with a diameter of (a) 2 and (b) 3 μm. Line width reduction and L−L curves of corresponding MDLs with a diameter of (c) 2 and (d) 3 μm. Insets in (c) and (d) corresponding log−log plots of the L−L curves.

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$\mu J/cm^2$. A logarithmic plot of the L−L curve in the inset illustrates the "S-shaped" transition from the spontaneous mode to lasing. Spectral emission signatures of the 3 μm-diameter MDL with different modes were illustrated in Figure 8b. Whispering-gallery mode (WGM) oscillation at the periphery of the disk cavity could generate multimode lasing in a microdisk due to a broader gain spectrum and a narrow free spectral range (FSR = $\lambda^2/2\pi r n_{eff}$).[36] The broader spectrum of as-grown GaAs on SOI under high-power excitation (as shown in the inset of Figure 6c) interacts with neighboring azimuthal order WGMs in the first radial order, giving rise to a distinct secondary lasing peak at a longer wavelength of 908 nm with an FSR of 25 nm. The FSR increases as the disk size shrinks (FSR ≈41 nm for 2 μm-diameter). Multimode MDLs have higher thresholds compared to those single-mode lasers due to mode competition. A distinct "kink" in the L−L curve and a clear line width reduction around the threshold (1200 $\mu J/cm^2$) were observed when progressively increasing the excitation level, as plotted in Figure 8d. The lasing behavior could prove the uniform GaAs quality with effective InP/In_xGaAs insertion. GaAs-based MDLs with InAs quantum dots (QDs) active medium show ultralow threshold and excellent laser performance at RT under continuous-wave mode on Si.[37,38] To get better laser performance, active regions such as quantum wells and QDs could be deposited in lateral GaAs on SOI in the near future. Furthermore, the surface state on the GaAs surface is a type of nonradiative recombination center, degrading the threshold and lifetime of GaAs MDLs. Surface passivation could be adopted to suppress the nonradiative recombination on the disk surface and thus contribute to a low threshold.[39]

CONCLUSIONS

To sum up, an in-plane GaAs crystal was selectively grown on patterned SOI by the LART technique. Uniform GaAs segments with good crystalline quality were achieved, as verified by TEM characterization and laser performance. Our results show that GaAs selectively grown on SOI could potentially act as a monolithic GaAs/SOI platform for GaAs-based alloys in Si photonics. Compared with InP/SOI, monolithic GaAs/SOI with efficient light coupling enables the extension of PICs to GaAs-based systems in the integration of III−V light sources on Si. Future work will be concentrated on further extending the growth width and length of GaAs as well as improving the uniformity of the GaAs segments. These in-plane GaAs/SOI platforms with flexible dimensions can be employed to fabricate various photonic devices, and it marks an important step forward toward fully integrated Si photonics.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.cgd.3c01279.

Additional information for comparison of two GaAs/Si structures grown on SOI and TEM image of the lateral growth of GaAs on SOI (PDF)

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Author Contributions

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Notes

The authors declare no competing financial interest.

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