Fully-Vertical GaN-on-SiC Trench MOSFETs

Jialun Li, Renqiang Zhu, *Member, IEEE*, Ka Ming Wong, and Kei May Lau, *Life Fellow, IEEE*

***Abstract*— This letter presents the first demonstration of fully-vertical GaN-on-SiC trench MOSFETs enabled by a conductive AlGaN buffer. Good ON-state device performance including a maximum drain current density of 2.43 kA/cm^2 and a high threshold voltage of 5 V has been demonstrated. The relatively high specific ON-resistance at low V_{DS} is a result of a knee voltage induced by the yet to be optimized AlGaN/SiC heterojunction. A breakdown voltage of 334 V has been measured. Compared with quasi-vertical GaN-on-silicon trench MOSFETs, less current crowding effect is observed for fully-vertical GaN-on-SiC trench MOSFETs, as well as a better performance at elevated temperatures.**

***Index Terms*— Gallium nitride, fully-vertical, GaN-on-SiC, conductive buffer, trench MOSFETs.**

I. Introduction

VERTICAL GaN-based power devices have received extensive research attention in the recent years, due to their potential in achieving high power handling capabilities with a better thermal performance compared with lateral GaN HEMTs [1]. Various kinds of vertical GaN power transistors have been demonstrated on bulk GaN substrates with excellent performance, including current aperture vertical electron transistors (CAVETs), in-situ oxide, GaN interlayer based vertical MOSFETs (OG-FETs), vertical fin MOSFETs (FinFETs) and vertical trench MOSFETs [2], [3], [4], [5], [6], [7], [8], [9]. Among them, trench MOSFETs stand out as a simple choice that can offer intrinsic normally-off operation with a p-GaN inversion channel, providing a high positive threshold voltage to prevent false turn-on. The p-n junction for OFF-state blocking can provide avalanche capability, which is vital for high power applications. Furthermore, a relatively simple fabrication process requiring no regrowth has been demonstrated [10].

Quasi-vertical GaN trench MOSFETs on cost-effective foreign substrates, such as sapphire and silicon have been reported [11], [12], [13], [14]. However, optimal utilization of wafer area cannot be implemented with drain contacts on the frontside, and the current crowding effect impedes the scaling of current with the device area and increases the resistance. For fully-vertical devices with drain contact at the substrate backside, these two problems can be alleviated [15]. Researchers successfully demonstrated fully-vertical GaN-on-silicon trench MOSFETs with a maximum drain current of around 5 mA, utilizing a complicated substrate removal process [16]. The full advantages of fully-vertical devices are yet to be demonstrated.

Alternatively, trench MOSFETs on a conductive buffer grown on doped substrates would greatly simplify the fabrication process. SiC has been shown to be the most sensible choice to realize high-performance fully-vertical GaN-on-SiC diodes with a conductive AlGaN buffer [17], [18], [19]. In addition to the advantage of smaller mismatch between GaN and SiC, the high thermal conductivity of SiC substrates is highly desirable for power applications. It's also possible to integrate GaN and SiC devices to combine their advantages if a GaN-on-SiC platform is used [20]. Recently, quasi-vertical GaN-on-SiC FinFETs are demonstrated [21]. However, there is no demonstration of fully-vertical GaN power transistors on foreign substrates by conductive buffer yet.

In this work, we report the first demonstration of fully-vertical GaN-on-SiC trench MOSFETs enabled by a conductive AlGaN buffer. Good device performance, including a maximum drain current density ($J_{D,max}$) of 2.43 kA/cm^2, a specific ON-resistance ($R_{ON,sp}$) of 9.58 mΩ·cm^2, a high threshold voltage (V_{th}) of 5 V and a breakdown voltage (V_{BR}) of 334 V is achieved. The advantage of our fully-vertical devices is demonstrated by comparing with quasi-vertical GaN-on-silicon trench MOSFETs. Less current crowding effect and better performance at high temperatures are observed for fully-vertical GaN-on-SiC trench MOSFETs. This work reveals the promising future of direct epitaxially-grown fully-vertical GaN-on-SiC devices for high power applications.

II. Epitaxial Growth and Device Fabrication

The epitaxial structure for fully-vertical GaN-on-SiC trench MOSFETs was grown on n-type 4H-SiC substrates by metal-organic chemical vapor deposition (MOCVD). The epilayers, from bottom to top, consist of a 70-nm n-$Al_{0.12}Ga_{0.88}N$ layer [Si: 2×10^{19} cm^{-3}], a 90-nm n-$Al_{0.12->0}Ga_{0.88->1}N$

Received 20 November 2024; revised 8 December 2024; accepted 16 December 2024. Date of publication 19 December 2024; date of current version 29 January 2025. This work was supported in part by the Innovation and Technology Fund of Hong Kong under the Midstream Research Program under Grant MRP/039/21 and in part by the Innovation and Technology Fund of Hong Kong under Guangdong–Hong Kong Technology Cooperation Funding Scheme under Grant GHP/014/21GD. The review of this letter was arranged by Editor G. H. Jessen. *(Corresponding author: Kei May Lau.)*

Jialun Li and Kei May Lau are with the Division of Emerging Interdisciplinary Area, The Hong Kong University of Science and Technology, Hong Kong (e-mail: eekmlau@ust.hk).

Renqiang Zhu is with the Division of Emerging Interdisciplinary Area, The Hong Kong University of Science and Technology, Hong Kong, and also with Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, Shenzhen 518000, China.

Ka Ming Wong was with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong. He is now with the School of Physics and Astronomy, Cardiff University, CF24 3AA Cardiff, U.K.

Digital Object Identifier 10.1109/LED.2024.3520200

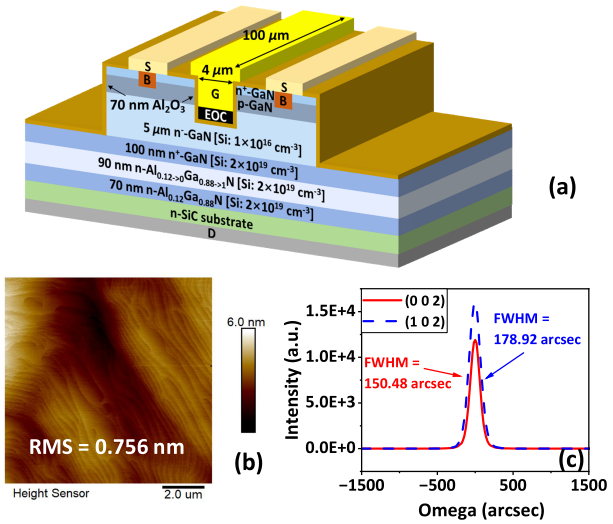

Fig. 1. (a) 3-D cross-sectional schematic of fabricated single trench fully-vertical GaN-on-SiC trench MOSFETs. "S", "D", "G" and "B" refers to "source", "drain", "gate" and "p-body" metal, respectively. (b) AFM scan image of the as-grown sample. (c). XRD rocking curves of the as-grown sample.

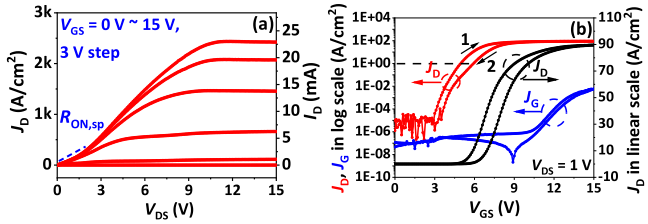

Fig. 2. Representative (a) output curves and (b) transfer curves of a single trench device.

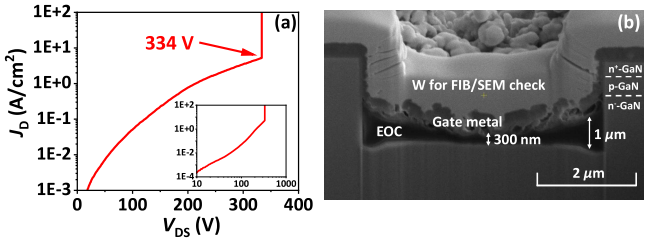

Fig. 3. (a) Representative reverse *J*-*V* characteristics of a single trench device in semi-log scale (inset: in log scale). (b) Cross-sectional SEM image of the gate trench region.

layer [Si: 2×10^{19} cm^{-3}], a 100-nm n$^+$-GaN layer [Si: 2×10^{19} cm^{-3}], a 5-μm n$^-$-GaN drift layer [Si: 1×10^{16} cm^{-3}], a 400-nm p-GaN layer [Mg: 4×10^{18} cm^{-3}] and a 300-nm n$^+$-GaN capping layer [Si: 2×10^{19} cm^{-3}], as shown in Fig. 1(a) [19]. The net doping concentration in the drift layer was determined to be around 4×10^{15} cm^{-3} from *C*-*V* measurements [22]. Fig. 1(b) and (c) are the atomic force microscope (AFM) scan and XRD rocking curves of the as-grown sample. For the AFM scan image (10×10 μm^2), clear step-flow surface morphology is observed, and the sample has a low root-mean-square surface roughness of 0.756 nm. For the XRD rocking curves, the threading dislocation density (TDD) estimated from empirical equations is 9.53×10^7 cm^{-2} [23], which is lower than the typical TDD of GaN grown on silicon or sapphire substrates [16], [24], due to the smaller lattice and thermal mismatch between GaN and SiC.

The fabrication process started with Cl-based ICP dry etching of trench, p-contact and mesa with hard mask. Hot tetramethylammonium hydroxide (TMAH) treatment was used after etching to smooth the etched surface and cure the etching damage [25]. Then, Ni was evaporated on the substrate backside as the drain contact. The sample was then annealed at 950°C in N_2 to form Ni-SiC ohmic contact and activate p-GaN [19]. Next, 70 nm Al_2O_3 gate oxide was grown by atomic layer deposition (ALD) and contact hole was opened. Finally, the p-body metal (Ni/Au) and source metal (Ti/Al/Ni/Au) were evaporated, and the gate metal (Ti/Cu/Au) was sputtered. Ethylene octene copolymer (EOC) was used as a thick bottom dielectric (TBD) in the trench to improve the OFF-state performance [13].

III. Device Results and Discussion

Fig. 2(a) shows the representative output curves of a single trench device. The device has a 4 μm $\times$ 100 μm rectangular trench, and the active area used for current density and specific ON-resistance normalization is 945 μm^2, after considering a 45-degree lateral current spreading in the drift layer [3]. The non-linearity in the deep triode region of the output curves is mainly caused by the AlGaN-SiC heterojunction [19], [26], which results in a knee voltage of around 2 V. At V_{GS} = 15 V, $R_{ON,sp}$ calculated at V_{DS} = 0.1 V is 9.58 m$\Omega\cdot$cm^2, which is dominated by the heterojunction, while $R_{ON,sp}$ calculated in the linear region at a higher V_{DS} is 3.13 m$\Omega\cdot$cm^2. Fig. 2(b) shows the representative transfer curves. A large V_{th} of 5 V (defined at 1 A/cm^2) is obtained, and the hysteresis is around 1 V. The ON/OFF current ratio is around 10^7, and the subthreshold swing is extracted to be 309 mV/dec.

Fig. 3(a) shows the representative reverse *J*-*V* characteristics of a single trench device in semi-log scale. The device has a hard breakdown voltage of 334 V. From the nearly linear log scale curve in the inset, the leakage current is dominated by space-charge limited conduction mechanism [24]. The destructive breakdown happens at the gate trench region resulted from electric field peaks at the bottom corners of the trench at reverse bias, indicating that the breakdown voltage can be much improved by optimizing the trench and gate oxide formation process [13], [14], [27]. It is worth mentioning that there are few observable cracks on the as-grown epi sample, which may also lead to the unsatisfactory breakdown voltage. Fig. 3(b) shows the cross-sectional SEM image of the gate trench region of a device. EOC TBD is clearly visible at the trench bottom.

One of the most important advantages of fully-vertical devices compared with quasi-vertical ones is the reduced current crowding effect, allowing more effective scaling of current with the device area [28]. To study this effect, a reference quasi-vertical GaN-on-silicon trench MOSFET sample (device structure similar to our work [14]) was fabricated together with fully-vertical GaN-on-SiC trench MOSFETs for comparison. Besides the single trench device with an active area of 945 μm^2, multi-finger trench MOSFETs with active area of 2835, 4725 and 90900 μm^2 were designed [14]. The maximum drain current density of these devices is plotted

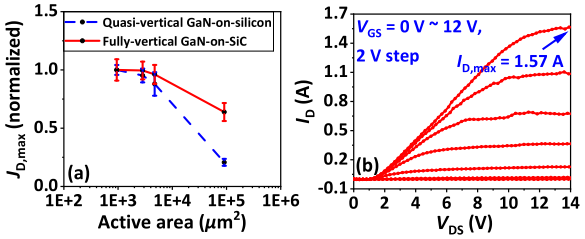

Fig. 4. (a) Normalized $J_{D,max}$ versus active area for quasi- and fully-vertical devices. (b) Output curves of a representative fully-vertical GaN-on-SiC trench MOSFET with an active area of 90900 μm^2.

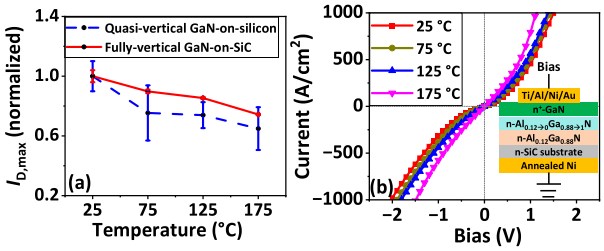

Fig. 5. (a) Normalized $I_{D,max}$ versus temperature for the quasi- and fully-vertical devices. (b) Vertical *J-V* characteristics of the buffer test structure at elevated temperatures (inset: buffer test structure).

against the active area in Fig. 4(a). To make a fair comparison between the quasi-vertical and fully-vertical devices, the $J_{D,max}$ values are all normalized to that of the smallest device. As the device area increases, $J_{D,max}$ of fully-vertical devices decreases much slower than quasi-vertical devices, especially for the largest device, due to more uniformly distributed current in the fully-vertical devices, compared with current crowding near the mesa edge for quasi-vertical devices [28], [29]. $J_{D,max}$ of the fully-vertical GaN-on-SiC devices still shows a dependence on the device area due to non-uniform current distribution and more pronounced self-heating effect in larger devices [29], [30], and this dependence is also observed in fully-vertical GaN-on-GaN devices [3], [22], [31]. Fig. 4(b) shows the output curves of a large fully-vertical GaN-on-SiC trench MOSFET (active area: 90900 μm^2) in our study. It has a high maximum drain current of 1.57 A, benefiting from the reduced current crowding effect and good thermal conductivity of the SiC substrate to mitigate the self-heating effect [29], [30], [32]. To the best of our knowledge, this is the highest current demonstrated among vertical GaN transistors on foreign substrates.

The quasi- and fully-vertical devices were tested at elevated temperatures to investigate the device temperature dependence. The normalized maximum drain current ($I_{D,max}$) is plotted against temperature in Fig. 5(a). Theoretically, $I_{D,max}$ drops as temperature increases due to reduced carrier mobility associated with increased phonon scattering. It's observed that $I_{D,max}$ drops slower with temperature for fully-vertical GaN-on-SiC trench MOSFETs. This can be explained by the better thermal conductivity of SiC substrates for heat dissipation, and improved buffer conductivity compensating for the reduction of carrier mobility at high temperatures, as shown in Fig. 5(b). The buffer test structure in the inset is tested at elevated temperatures. The buffer resistance reduces, and the vertical *J-V* characteristic becomes more linear as temperature increases, which can be explained by improved carrier tunneling at the AlGaN-SiC heterojunction, thermally enhanced ionization of the donors in the AlGaN buffer layers and improved Ni-SiC contact [33], [34]. This high-temperature feature gives our fully-vertical GaN-on-SiC trench MOSFETs a special advantage.

IV. Conclusion

In summary, we demonstrate the first fully-vertical GaN-on-SiC trench MOSFETs with good ON-state current density and threshold voltage. With further improvement of the AlGaN/SiC heterostructure growth, the knee voltage and $R_{ON,sp}$ can be minimized. The advantage of reduced current crowding effect in fully-vertical devices is demonstrated, and a high current of 1.57 A is achieved in large area fully-vertical GaN-on-SiC trench MOSFETs. The fully-vertical GaN-on-SiC trench MOSFETs also have a better high-temperature performance than quasi-vertical GaN-on-silicon devices. These initial results offer an important step towards the development of fully-vertical GaN-on-SiC power devices, which is promising for power electronics.

Acknowledgment

The authors would like to thank Dr. Huaxing Jiang for many helpful discussions and the staff of the Nanosystem Fabrication Facility (NFF) and Material Characterization and Preparation Facility (MCPF) at HKUST, for their technical support.

References

[1] Y. Zhang, M. Sun, Z. Liu, D. Piedra, H.-S. Lee, F. Gao, T. Fujishima, and T. Palacios, "Electrothermal simulation and thermal performance study of GaN vertical and lateral power transistors," *IEEE Trans. Electron Devices*, vol. 60, no. 7, pp. 2224–2230, Jul. 2013, doi: 10.1109/TED.2013.2261072.

[2] D. Ji, M. A. Laurent, A. Agarwal, W. Li, S. Mandal, S. Keller, and S. Chowdhury, "Normally OFF trench CAVET with active mg-doped GaN as current blocking layer," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 805–808, Mar. 2017, doi: 10.1109/TED.2016.2632150.

[3] D. Ji, C. Gupta, A. Agarwal, S. H. Chan, C. Lund, W. Li, S. Keller, U. K. Mishra, and S. Chowdhury, "Large-area in-situ oxide, GaN interlayer-based vertical trench MOSFET (OG-FET)," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 711–714, May 2018, doi: 10.1109/LED.2018.2813312.

[4] Y. Zhang, M. Sun, J. Perozek, Z. Liu, A. Zubair, D. Piedra, N. Chowdhury, X. Gao, K. Shepard, and T. Palacios, "Large-area 1.2-kV GaN vertical power FinFETs with a record switching figure of merit," *IEEE Electron Device Lett.*, vol. 40, no. 1, pp. 75–78, Jan. 2019, doi: 10.1109/LED.2018.2880306.

[5] H. Otake, K. Chikamatsu, A. Yamaguchi, T. Fujishima, and H. Ohta, "Vertical GaN-based trench gate metal oxide semiconductor field-effect transistors on GaN bulk substrates," *Appl. Phys. Exp.*, vol. 1, no. 1, Jan. 2008, Art. no. 011105, doi: 10.1143/apex.1.011105.

[6] T. Oka, Y. Ueno, T. Ina, and K. Hasegawa, "Vertical GaN-based trench metal oxide semiconductor field-effect transistors on a free-standing GaN substrate with blocking voltage of 1.6 kV," *Appl. Phys. Exp.*, vol. 7, no. 2, Jan. 2014, Art. no. 021002, doi: 10.7567/apex.7.021002.

[7] T. Oka, T. Ina, Y. Ueno, and J. Nishii, "1.8 mΩ·cm^2 vertical GaN-based trench metal–oxide–semiconductor field-effect transistors on a free-standing GaN substrate for 1.2-kV-class operation," *Appl. Phys. Exp.*, vol. 8, no. 5, May 2015, Art. no. 054101, doi: 10.7567/apex.8.054101.

[8] T. Oka, T. Ina, Y. Ueno, and J. Nishii, "Over 10 a operation with switching characteristics of 1.2 kV-class vertical GaN trench MOSFETs on a bulk GaN substrate," in *Proc. 28th Int. Symp. Power Semicond. Devices ICs (ISPSD)*, Prague, Czech Republic, Jun. 2016, pp. 459–462, doi: 10.1109/ISPSD.2016.7520877.

[9] T. Oka, T. Ina, Y. Ueno, and J. Nishii, "100 a vertical GaN trench MOSFETs with a current distribution layer," in *Proc. 31st Int. Symp. Power Semicond. Devices ICs (ISPSD)*, Shanghai, China, May 2019, pp. 303–306, doi: 10.1109/ISPSD.2019.8757621.

[10] R. Zhu, H. Jiang, C. W. Tang, and K. M. Lau, "Effects of p-GaN body doping concentration on the ON-state performance of vertical GaN trench MOSFETs," *IEEE Electron Device Lett.*, vol. 42, no. 7, pp. 970–973, Jul. 2021, doi: 10.1109/LED.2021.3080260.

[11] C. Liu, R. A. Khadar, and E. Matioli, "GaN-on-Si quasi-vertical power MOSFETs," *IEEE Electron Device Lett.*, vol. 39, no. 1, pp. 71–74, Jan. 2018, doi: 10.1109/LED.2017.2779445.

[12] Z. Guo, C. Hitchcock, R. F. Karlicek, G. Piao, Y. Yano, S. Koseki, T. Tabuchi, K. Matsumoto, M. Bulsara, and T. P. Chow, "Integrable quasivertical GaN U-shaped trench-gate metal-oxide-semiconductor field-effect transistors for power and optoelectronic integrated circuits," *Phys. Status Solidi A*, vol. 217, no. 7, Apr. 2020, Art. no. 1900615, doi: 10.1002/pssa.201900615.

[13] R. Zhu, H. Jiang, C. W. Tang, and K. M. Lau, "Enhancing ON- and OFF-state performance of quasi-vertical GaN trench MOSFETs on sapphire with reduced interface charges and a thick bottom dielectric," *IEEE Electron Device Lett.*, vol. 43, no. 3, pp. 346–349, Mar. 2022, doi: 10.1109/LED.2022.3146276.

[14] R. Zhu, H. Jiang, C. W. Tang, and K. M. Lau, "GaN quasi-vertical trench MOSFETs grown on Si substrate with ON-current exceeding 1 a," *Appl. Phys. Exp.*, vol. 15, no. 12, Nov. 2022, Art. no. 121004, doi: 10.35848/1882-0786/aca26e.

[15] Y. Zhang, M. Yuan, N. Chowdhury, K. Cheng, and T. Palacios, "720-V/0.35-m $\Omega \cdot cm^2$ fully vertical GaN-on-Si power diodes by selective removal of Si substrates and buffer layers," *IEEE Electron Device Lett.*, vol. 39, no. 5, pp. 715–718, May 2018, doi: 10.1109/LED.2018.2819642.

[16] R. A. Khadar, C. Liu, R. Soleimanzadeh, and E. Matioli, "Fully vertical GaN-on-Si power MOSFETs," *IEEE Electron Device Lett.*, vol. 40, no. 3, pp. 443–446, Mar. 2019, doi: 10.1109/LED.2019.2894177.

[17] D. Yoo, J. B. Limb, J.-H. Ryou, W. Lee, and R. D. Dupuis, "Epitaxial growth and device design optimization of full-vertical GaN p-i-n rectifiers," *J. Electron. Mater.*, vol. 36, no. 4, pp. 353–358, Feb. 2007, doi: 10.1007/s11664-006-0069-1.

[18] Y. Li, S. Yang, K. Liu, K. Cheng, K. Sheng, and B. Shen, "Fully-vertical GaN-on-SiC Schottky barrier diode: Role of conductive buffer structure," *IEEE Trans. Electron Devices*, vol. 70, no. 2, pp. 619–626, Feb. 2023, doi: 10.1109/TED.2022.3227227.

[19] J. Li, R. Zhu, K. M. Wong, and K. M. Lau, "Fully vertical GaN-on-SiC p-i-n diodes with BFOM of 2.89 GW/cm^2," *IEEE J. Electron Devices Soc.*, vol. 12, pp. 318–321, 2024, doi: 10.1109/JEDS.2024.3386857.

[20] S. Feng, Z. Zheng, Y. Wang, G. Lyu, K. Liu, Y. Cheng, J. Chen, T. Chen, L. Zhang, W. Song, H. Liao, Y. H. Ng, M. Hua, K. Cheng, J. Wei, and K. J. Chen, "HyFET-A GaN/SiC hybrid field-effect transistor," in *IEDM Tech. Dig.*, Dec. 2023, pp. 1–4, doi: 10.1109/IEDM45741.2023.10413796.

[21] P. Gribisch, R. D. Carrascon, V. Darakchieva, and E. Lind, "Tuning of quasi-vertical GaN FinFETs fabricated on SiC substrates," *IEEE Trans. Electron Devices*, vol. 70, no. 5, pp. 2408–2414, May 2023, doi: 10.1109/TED.2023.3263154.

[22] K. Nomoto, B. Song, Z. Hu, M. Zhu, M. Qi, N. Kaneda, T. Mishima, T. Nakamura, D. Jena, and H. G. Xing, "1.7-kV and 0.55-m$\Omega \cdot cm^2$ GaN p-n diodes on bulk GaN substrates with avalanche capability," *IEEE Electron Device Lett.*, vol. 37, no. 2, pp. 161–164, Feb. 2016, doi: 10.1109/LED.2015.2506638.

[23] M. A. Moram and M. E. Vickers, "X-ray diffraction of III-nitrides," *Rep. Prog. Phys.*, vol. 72, no. 3, Mar. 2009, Art. no. 036502, doi: 10.1088/0034-4885/72/3/036502.

[24] Y. Zhang, H.-Y. Wong, M. Sun, S. Joglekar, L. Yu, N. A. Braga, R. V. Mickevicius, and T. Palacios, "Design space and origin of off-state leakage in GaN vertical power diodes," in *IEDM Tech. Dig.*, Dec. 2015, pp. 35.1.1–35.1.4, doi: 10.1109/IEDM.2015.7409830.

[25] Y. Zhang, M. Sun, H.-Y. Wong, Y. Lin, P. Srivastava, C. Hatem, M. Azize, D. Piedra, L. Yu, T. Sumitomo, N. A. de Braga, R. V. Mickevicius, and T. Palacios, "Origin and control of OFF-state leakage current in GaN-on-Si vertical diodes," *IEEE Trans. Electron Devices*, vol. 62, no. 7, pp. 2155–2161, Jul. 2015, doi: 10.1109/TED.2015.2426711.

[26] A. Nishikawa, K. Kumakura, and T. Makimoto, "Low on-resistance of GaN p-i-n vertical conducting diodes grown on 4H-SiC substrates," *Phys. Status Solidi C*, vol. 4, no. 7, pp. 2662–2665, Jun. 2007, doi: 10.1002/pssc.200674713.

[27] Y. Zhang, M. Sun, Z. Liu, D. Piedra, J. Hu, X. Gao, and T. Palacios, "Trench formation and corner rounding in vertical GaN power devices," *Appl. Phys. Lett.*, vol. 110, no. 19, May 2017, Art. no. 193506, doi: 10.1063/1.4983558.

[28] Y. Zhang, M. Sun, D. Piedra, J. Hennig, A. Dadgar, and T. Palacios, "Reduction of on-resistance and current crowding in quasi-vertical GaN power diodes," *Appl. Phys. Lett.*, vol. 111, no. 16, Oct. 2017, Art. no. 163506, doi: 10.1063/1.4989599.

[29] X. Zhang, X. Zou, X. Lu, C. W. Tang, and K. M. Lau, "Fully- and quasi-vertical GaN-on-Si p-i-n diodes: High performance and comprehensive comparison," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 809–815, Mar. 2017, doi: 10.1109/TED.2017.2647990.

[30] B. Chatterjee, D. Ji, A. Agarwal, S. H. Chan, S. Chowdhury, and S. Choi, "Electro-thermal investigation of GaN vertical trench MOSFETs," *IEEE Electron Device Lett.*, vol. 42, no. 5, pp. 723–726, May 2021, doi: 10.1109/LED.2021.3065362.

[31] S. Jeong, K. Lee, J. Chun, R. Soman, and S. Chowdhury, "Scaling study on high-current density low-dispersion GaN vertical FinFETs," *IEEE Electron Device Lett.*, vol. 44, no. 5, pp. 841–844, May 2023, doi: 10.1109/LED.2023.3259002.

[32] J. Dallas, G. Pavlidis, B. Chatterjee, J. S. Lundh, M. Ji, J. Kim, T. Kao, T. Detchprohm, R. D. Dupuis, S. Shen, S. Graham, and S. Choi, "Thermal characterization of gallium nitride p-i-n diodes," *Appl. Phys. Lett.*, vol. 112, no. 7, Feb. 2018, Art. no. 073503, doi: 10.1063/1.5006796.

[33] K. Zhu, M. L. Nakarmi, K. H. Kim, J. Y. Lin, and H. X. Jiang, "Silicon doping dependence of highly conductive n-type $Al_{0.7}Ga_{0.3}N$," *Appl. Phys. Lett.*, vol. 85, no. 20, pp. 4669–4671, Nov. 2004, doi: 10.1063/1.1825055.

[34] J. Crofton, P. G. Mcmullin, J. R. Williams, and M. J. Bozack, "High-temperature ohmic contact to n-type 6H-SiC using nickel," *J. Appl. Phys.*, vol. 77, no. 3, pp. 1317–1319, Feb. 1995, doi: 10.1063/1.358936.