A Fully-Integrated Micro-Display System With Hybrid Voltage Regulator

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***Abstract*—A fully-integrated active matrix light-emitting diode (AMLED) micro-display system is demonstrated in this paper. The system consists of a 36 × 64 AMLED array chip based on GaN-on-Silicon epilayers and a silicon driving chip integrating an on-chip hybrid voltage regulator, pixel drivers, and peripheral circuits. Then two chips are bonded with low-cost Au-free flip-chip bonding technology. As such, this system is able to directly operate with a battery without any external passive components. Multiple techniques were proposed to achieve the system integration: (1) A fully-integrated hybrid voltage regulator consisting of a step-up switched-capacitor (SC) converter cascaded by a step-down linear voltage regulator was fabricated in a 0.18 μm CMOS technology. It achieved only 1.38% output voltage ripple without external capacitors, and be able to deliver a maximum power of 216mW with peak efficiencies of 91% in the linear mode and 78% in the SC mode; (2) Micro-LEDs are fabricated on GaN-on-Silicon substrate that significantly suppresses the light crosstalk between pixels and reduces the cost; (3) An Au-free flip-chip bonding technique is developed to reduce the bonding cost and achieved reliable connections between AMLED array chip and silicon driving chip. The whole system achieved 635 pixel/in (PPI) pixel density. Images and videos with 4-bit grayscale could be rendered. This prototype achieved a high integration level and demonstrates the tremendous potential of the highly efficient, low cost fully integrated AMLED micro-display system.**

***Index Terms*—Active matrix light-emitting diodes, active matrix LED, AMLED, micro-display, micro display system, LED driver, pixel drivers, fully integrated, voltage regulator, switched-capacitor converter, SC converter, GaN-on-Silicon, flip-chip bonding, Au-free flip-chip, battery-connected, grayscale.**

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I. Introduction

Micro-display systems are rapidly gaining demands in consumer electronics such as augmented reality (AR), virtual reality (VR) [1-5], and visible light communication applications (VLC) [6], especially after the concept of metaverse was introduced. Micro-displays are also showing an increasingly potential in the industry X.0 applications, such as being head-mounted displays (HMDs) or wearable devices in manufacturing, logistics, and constructions, due to their compact size, high image quality, and ability to provide the real-time information and data.

In particular, active matrix light-emitting diode (AMLED) is attracting massive interests from both the academia and also the industry. Compared with traditional liquid crystal display (LCD) technology [7], AMLED is self-emissive that can produce light without a power-hungry backlight and is thus thinner, smaller, and more power-efficient. Compared with organic LED (OLED) [8], semiconductor-based AMLED has advantages of a longer lifetime, lower fabrication cost, better reliability, and higher brightness, becomes one of the most promising technologies in micro-displays [1-6].

Fig. 1(a) shows the conventional implementation of the AMLED micro-display system. The display panel formed by the AMLED array which is usually implemented by a gallium nitride (GaN) process. The control and pixel drivers are realized by the standard CMOS process in a silicon chip. The turning-on and -off of each LED pixel is controlled by the pixel drivers. In some designs, the silicon chip may bond with the GaN chip as a backplane, but it needs external a power management integrated circuit (IC) to convert the battery voltage to a required voltage of micro-displays. From a system-level perspective, the external power management IC [9], [10] with bulky inductors and capacitors is the major factor that limits the system volume. Therefore, to make the system more compact and further reduce the cost, it is quite beneficial to integrate the power supply with the control and driver together on the silicon driving chip, as shown in Fig. 1(b).

Integrating the switching DC-DC converter is a major challenge as it is difficult to fabricate a good power inductor on-chip [9-12]. By comparison, linear regulators only need transistors while switched-capacitor (SC) converters only need capacitors and switches that are feasible on-chip [13-14]. Therefore, they are good candidates to be the integrated voltage

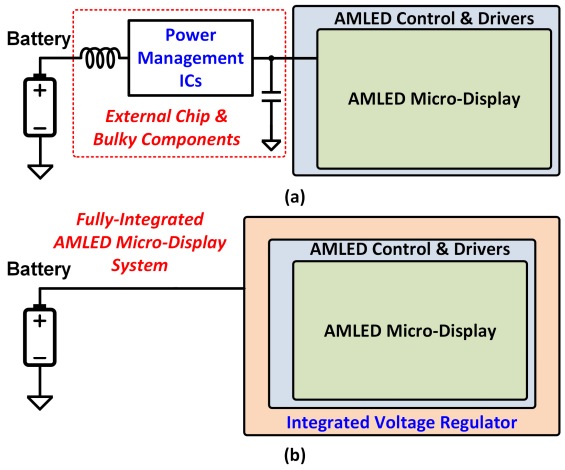


Fig. 1. (a) Conventional AMLED micro-display powered by external power management ICs; (b) Proposed fully-integrated AMLED Micro-display system with integrated voltage regulator.

regulator. In particular, the efficiency of an SC converter could be high when the ratio of the output voltage V_O to the input voltage V_{IN} is closed to the ideal voltage conversion ratio (VCR) of the converter [16-17].

Another important requirement for the power supply is low output voltage ripple [9-10], especially for driving an AMLED micro-display, as the current of a micro-LEDs is very sensitive to its supply voltage. A large voltage ripple may result in a large variation of light intensity, thus degrading the uniformity of the whole display panel. For an SC converter, a low voltage ripple could be achieved by the multiphase interleaving scheme [18], [33] or by modulating the turn-on resistance [19], [20]. For a linear regulator, the ripple voltage is much reduced through the operation of the linear feedback circuit.

Besides the requirements from the integrated power supply, the fabrication and implementation of micro-LEDs still have challenges. First, for micro-LEDs, up to now most of the works [1-5], [21-22] are fabrication on a sapphire substrate but may result in severe crosstalk between pixels. Also, the thermal mismatch between sapphire and silicon will degrade the reliability when making the flip-chip bonding. Therefore, silicon substrate based micro-LEDs are needed. To get a high-quality flip-chip bonding, Au metal-based bonding has been used in some works [21-24]. The metal layer in the bonding is usually very thick, which leads to a high cost. Thus, Au-free bonding technology is highly desirable to keep the cost low and obtain reliable connections between micro-LEDs to the pixel drivers.

To tackle the aforementioned challenges, in this research, we explored multiple technologies to demonstrate this fully integrated AMLED micro-display system: (1) We proposed an integrated hybrid voltage regulator to power up the display while eliminating all external components and achieving low voltage ripple [25]. It consists of a step-up switched-capacitor converter and a step-down linear regulator, so can cover the whole voltage range of a Li-ion battery. (2) The micro-LEDs are fabricated on GaN-on-Silicon substrate rather than the sapphire substrate to reduce the light crosstalk among the pixels [26]. (3) Au-free flip-chip bonding technique [26] is used to achieve both high yield and low cost. By doing so, this fully integrated system can operate directly connecting to a Li-ion battery without any external components, significantly reduces the system volume, and shows a great potential of large-scale, low cost, and high reliability. In this paper, we systematically present a methodology to implement the fully-integrated AMLED display system, from the system, circuit, device fabrication, and packaging prospective. The previous works [25-26, 33] were considerably reorganized and fully-integrated micro-display system is demonstrated from a more systematical perspective.

The remainder of this paper is organized as follows. Sections II discusses the system design and layout considerations. Section III describes the circuit implementation of the fully-integrated hybrid voltage regulator, on both

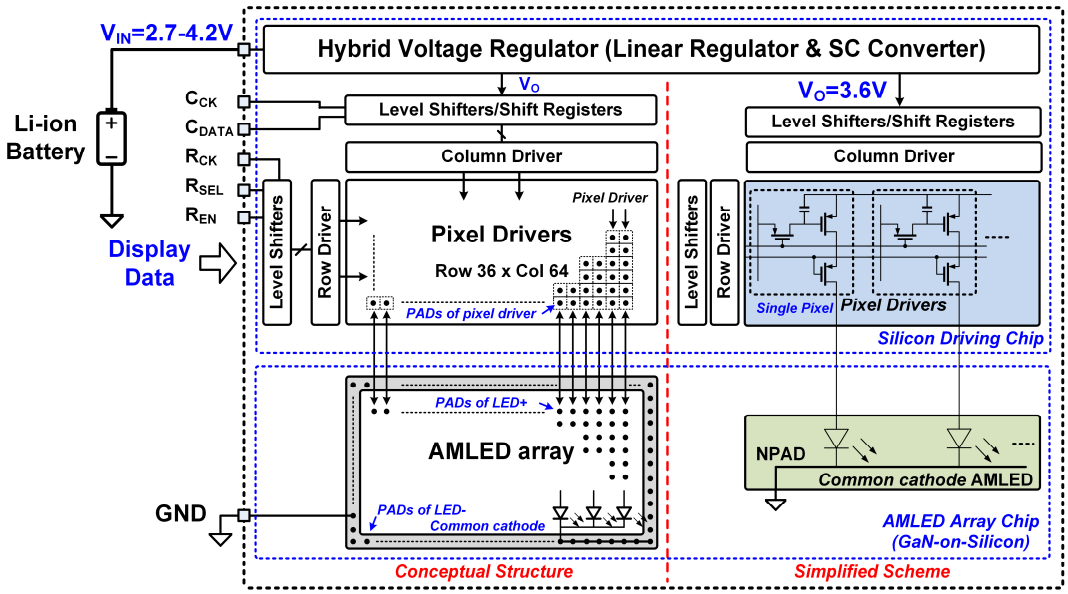


Fig. 2. The conceptual structure (left) and simplified scheme (right) of proposed micro-display system.

switched-capacitor converter and linear regulator. Section IV discuss the control scheme of the pixel drivers, and the frame setup of the display data. Section V introduces the process of AMLED array fabrication and flip-chip bonding technique. Measurement results are shown in Section VI and then followed by the conclusions.

II. System Architecture and Layout Floorplan

A. System Structure

Fig. 2 shows the conceptual structure (left) and the simplified scheme of the proposed fully integrated AMLED micro-display system. In general, it consists of two chips. The first chip is the silicon driving chip which is consisting of an integrated hybrid voltage regulator, pixel drivers, shift registers, level shifters, a row driver, and a column driver. The integrated hybrid voltage regulator converts the input Li-ion voltage (V_{IN} = 2.7 - 4.2V) to a stable and constant output voltage V_O=3.6V as the supply voltage for all the pixel drivers, and also providing currents to the micro-LEDs. The pixel drivers have a one-to-one correspondence to the micro-LEDs. The row and column drivers are located on the left and top of the pixel drivers, respectively. The display data (C_{CK}, C_{DATA}, R_{CK}, R_{SEL}, and R_{EN}) are sent from an external controller, and internal level shifters are used to convert these input data signals to the proper internal voltage domains.

The second chip is the AMLED array chip, which is built on a GaN-on-Silicon process. The AMLED array chip has 36 × 64 micro-LED pixels, and each pixel is common cathode connected. Such that it has 36 × 64 p-pads connecting to the silicon driving chip and one n-pad connecting to the ground.

Fig. 3 shows the vertical structure of the system. As the AMLED chip is flip-chip bonded on the silicon chip, the thermal generated by the AMLED chip is conducted through the flip-chip bumps to the silicon chip. The silicon chip is stuck at the PCB metal with thermally conductive material so that the thermal can eventually be passed to the PCB.

B. Layout Floorplan and Benefits

To drive the AMLED array, the power supply and distribution are required to have a good uniformity across the pixels and a low ripple voltage, as the brightness of micro-LEDs is sensitive to the voltage variations. To tackle these issues, we proposed to use a converter ring-based structure and distributive multiple interleaving scheme.

Fig. 3 shows the layout floorplan of the silicon driving chip. The pixel drivers, row and column drivers occupied the large central area. To distribute the power from outside to the middle, the SC converter of the voltage regulator is divided into multiple small power cells, forming a converter ring surrounding the central area. Pixels can get power from the V_{OUT} power rails around the chip via the shortest path. The thick top-metal is also laid on top of the pixel drivers to connect V_{OUT} and ground to reduce the path resistance. So the minimum IR drop and good uniformity can be achieved.

The multiphase interleaving scheme is also used to cancel the output voltage (V_{OUT}) ripple and input current (I_{IN}) ripple so

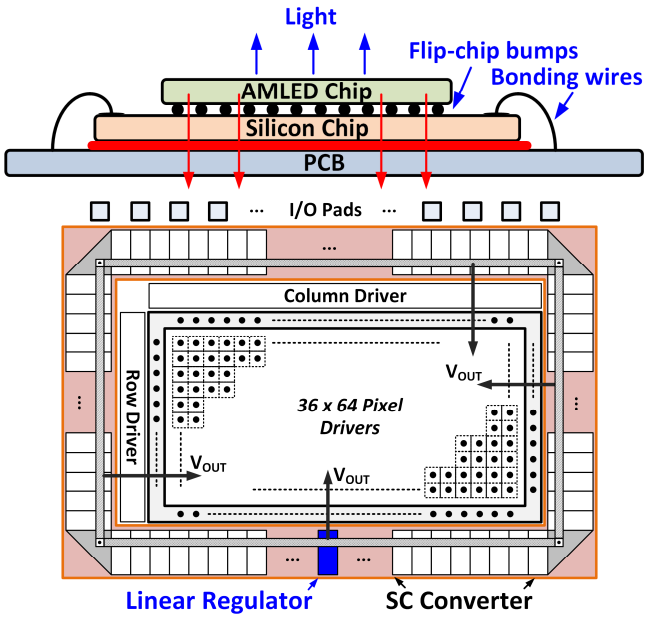


Fig. 3. The vertical structure of the system and the layout floorplan of the silicon driving chip.

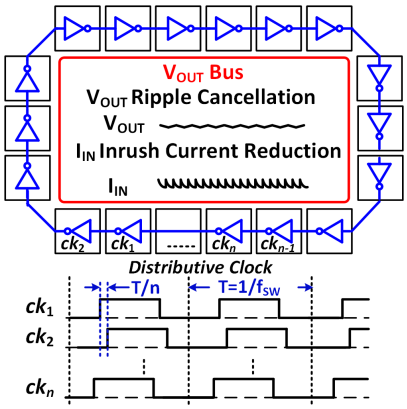


Fig. 4. Multiphase interleaving with distributive clock scheme.

that the input and output capacitors can be significantly reduced. Multiphase interleaving is reported to be a very effective method to reduce input current and output voltage ripple [18], [25], [27-31]. Fig. 4(a) shows the concept of multiphase interleaving. The power converter is divided into several small power cells. Adjacent power cells are operated by clock that have a small phase delay (T/n, T is the clock period and n is phase number). Such that the output voltages and input currents of each cell will have the same delay, and the total output voltage ripple and input current ripple will be at a higher frequency and theoretically be canceled. Consequently, this significantly reduces the requirement of output and input capacitors, so we can eliminate the external capacitors. It is noted that with more phases, a smaller ripple can be achieved.

It is beneficial for the on-chip switched-capacitor converter to use multiphase interleaving, but still, be challenging to generate a large number of phases. We proposed to use a distributive clock [18] scheme to generate 87 interleaving phases in this design, as shown in Fig. 4(b). Each power cell has its internal inverter to generate the clock and phase delay.

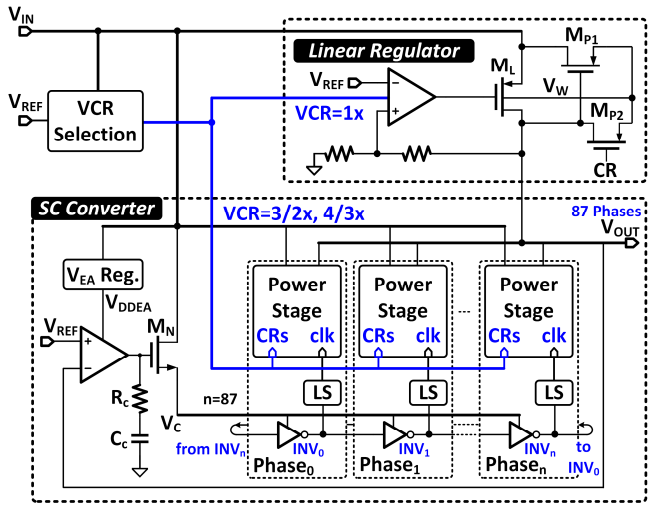


Fig. 5. System diagram of proposed integrated hybrid voltage regulator.

Connecting all these inverters can form a ring-oscillator to automatically generate phase delayed clocks and distribute the clocks across the chip. Compared with the clocks generated by the central ring-oscillator, this distributive scheme has a much lower power consumption, as it only has parasitic capacitance on one clock chain. Moreover, the shape of the converter ring is flexible to change according to the aspect ratio of the pixel drivers. It is not necessary to be in symmetrical shape (e.g. H-tree) to avoid clock mismatches. In this work, the number of phases and the aspect ratio of the power cell are defined by the perimeter of the AMLED array. The maximum output current of SC converter is set as 60mA, and 690μA for each power cell.

III. Hybrid Voltage Regulator Design

In this AMLED system, the typical voltage for the pixel driver branch to turn on the LED is 3.6V. The voltage from a Li-ion battery is from 2.7V when complexity discharged and is 4.2V when fully charged. In such a case, the voltage regulator needs to have both step-up and step-down voltage conversion features, to cater to the Li-ion battery voltage range. In this section, we will illustrate the fully-integrated voltage regulator design.

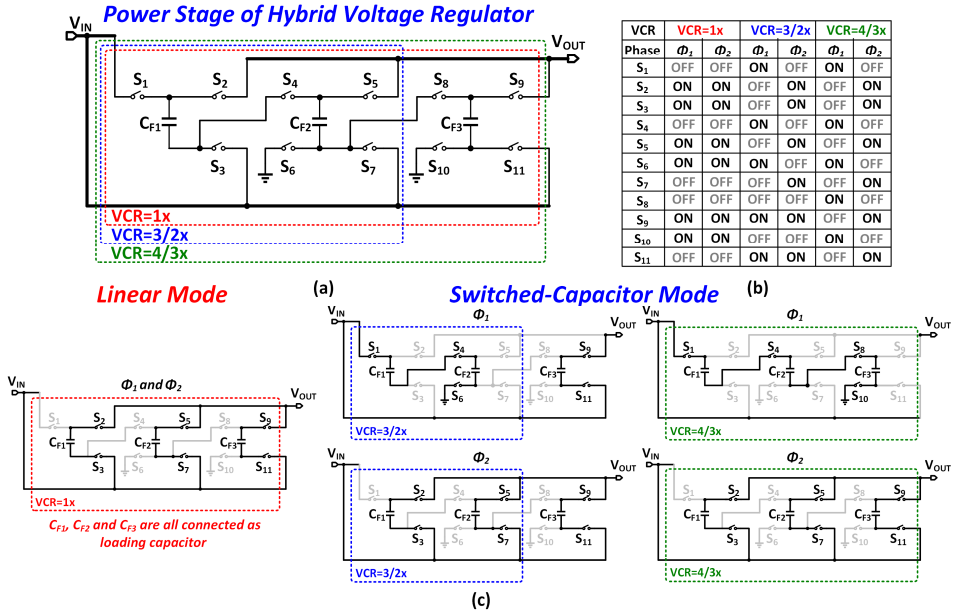
A. Overall Structure and Voltage Modes

Fig. 5 shows the system diagram of the proposed integrated hybrid voltage regulator, consisting of a linear regulator and an SC converter. It has three voltage conversion ratios (VCRs). When the input voltage is lower than 3.6V, the SC converter is enabled and the VCR could be adjusted to 3/2× or 4/3×. When the input voltage is higher than 3.6V, the linear regulator is enabled and the VCR is 1×.

Fig. 6 shows a generic schematic and operating principle of the integrated hybrid voltage regulator. The details of the turning-on and -off statuses of switches in 3 VCRs are tabulated in Fig. 6(b), and also the working principles are shown in Fig. 6(c). Clearly, the DC voltages of flying capacitors are $V_{CF1,\,F2} = 1/2\times V_{IN}$ (in 3/2× mode), and $V_{CF1,\,F2,\,F3} = 1/3\times V_{IN}$ (in 4/3× mode).

The circuit topology is determined by the VCR detection circuit that compares the input voltage V_{IN} with the reference voltage V_{REF}. In this design, V_{OUT} equals to 3.6 V, and the VCRs are assigned as follows. When V_{IN} is within 2.7V to 3.2V, VCR is 3/2×, and when V_{IN} is within 3.2V to 3.75V, VCR is 4/3×. When V_{IN} is higher than 3.75V, VCR is 1×. Voltage margins are reserved between adjacent modes to compensate for the V_{OUT} drop caused by the output resistance R_{OUT} of the SC converter. Also, hysteresis windows are intentionally built in the comparators to avoid frequent transitions of operating modes.

B. SC Converter Design: Power Stage, Close Loop, and Multi-Phase Interleaving



VCR	VCR=1x		VCR=3/2x		VCR=4/3x	
Phase	Φ_1	Φ_2	Φ_1	Φ_2	Φ_1	Φ_2
S_1	OFF	OFF	ON	OFF	ON	OFF
S_2	ON	ON	OFF	ON	OFF	ON
S_3	ON	ON	OFF	ON	OFF	ON
S_4	OFF	OFF	ON	OFF	ON	OFF
S_5	ON	ON	OFF	ON	OFF	ON
S_6	ON	ON	ON	OFF	ON	OFF
S_7	OFF	OFF	OFF	ON	OFF	ON
S_8	OFF	OFF	OFF	OFF	ON	OFF
S_9	ON	ON	ON	ON	OFF	ON
S_{10}	ON	ON	OFF	OFF	ON	OFF
S_{11}	OFF	OFF	ON	ON	OFF	ON

Fig. 6. (a) Schematic of power stage, (b) tabulated switches status in 3 VCRs, and (c) phase-by-phase working principles of 3 VCRs.

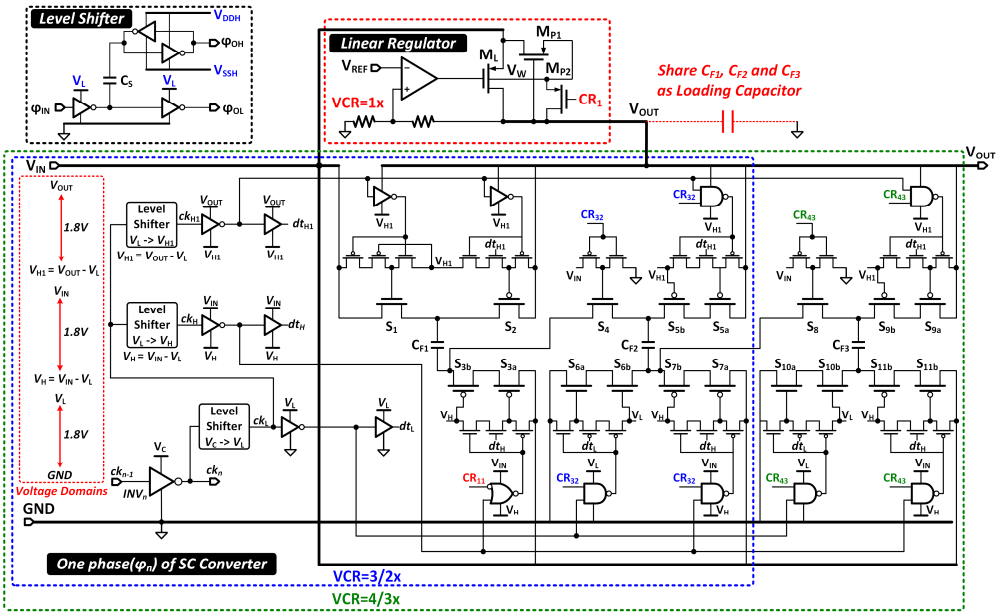


Fig. 7. Transistor level implementation of linear regulator and one power cell (phase-n), including level shifters.

Fig. 7 shows the transistor level circuit implementation of the power stage of the SC converter and linear regulator. For SC converter, one phase of power cell consists of three flying capacitors (CF_1, CF_2, and CF_3) that are realized from both thin-oxide MOS and MIM capacitors, maximizing the on-chip capacitance density to around 10nF/mm^2. The capacitance is around 33pF for each one. Three digital bits (CR_{11}, CR_{23}, and CR_{23}) are used to determine the VCR to be 1×, 3/2×, and 4/3×. In each mode, unused capacitors are connected between V_{OUT} and V_{IN} as decoupling capacitors, or as loading capacitors to increase the area utilization.

One power cell has eleven power transistors from S_1 to S_{11}. As discussed before, except for S_1, S_2, S_4, and S_8, other power switches are implemented by stacking two thin-oxide transistors together to tolerant higher voltages and reduce the switching loss when having the same turn-on resistance of the single thick-oxide transistor. Simulation results show that in 0.18μm CMOS process, when using a 1.8V stacking transistor, the switching loss can have 1.7× (PMOS) to 2.6× (NMOS), comparing to 5V transistors [32-34].

To properly bias the thin-oxide transistor, three internal voltage domains are created by internal voltage regulators: (GND to V_L), (V_H=V_{IN}-V_L, V_{IN}), and (V_{H1}=V_{OUT}-V_L, V_{OUT}). The typical voltage of each domain is 1.8V, such that the stacking transistors can be fixed to these domains, as well as the digital logic. Since these voltage domains are kept in a constant DC voltage, capacitive coupling level shifters are used. The clock signal ck_n is firstly level shifted from VCO's output voltage to V_L (ck_L), and then shifted to V_H (ck_H) and V_{H1} (ck_{H1}) domains. Before the power transistor drivers, dead-time signals (dt_L, dt_H, and dt_{H1}) are generated by delay cells.

To regulate the output voltage of the SC converter, frequency modulation is used, and 87 power cells are operating in a multiphase interleaving mode. The output voltage is fed back to the error amplifier, which then generates the signal to control VCO. The error amplifier is consisting of a current-mirror transconductor followed by a source follower M_N to increase the current driving capability. The source follower M_N also brings a low impedance node. Also, the output capacitance in the SC converter is very small, such that the pole at output node is higher than the unity-gain frequency (UGF). Such that the dominant pole of the SC converter is placed at error amplifier's output node, and the loop is compensated by a type-II pole-zero pair compensator.

C. *Linear Regulator Capacitor Sharing and Body Switch*

The linear regulator design uses an error amplifier and PMOS transistor as power transistor (Fig. 7). Comparing to conventional design, two considerations are taken. First, since the integrated hybrid voltage regulator does not require an external output capacitor, when the regulator is working in linear mode (VCR=1×), all flying capacitors in the SC converter are connected to the output V_O node. Switches S_2, S_3, S_5, S_7, S_9, and S_{11} are always on, so all flying capacitors are making the loading capacitors. It is particularly important for the linear regulator when setting the dominant pole at the output voltage node. The compensation scheme is much easier and simpler than the designs setting the dominant pole inside, and this scheme is different from the SC converter.

Second, when the regulator is in SC mode, output voltage V_O could be higher than input V_{IN}, causing the body diode of PMOS transistor M_L forward conduction. To avoid this issue, a body-selection switch (M_{P1} and M_{P2}) is employed to ensure the body of M_L is always connected to the highest voltage when V_O is higher than V_{IN}.

IV. Pixel Driver and Display Control

The pixel drivers are located in the center of the silicon driving chip. The AMLED pixel and pixel driver is one to one in corresponding, so a total of 64 × 36 pixel drivers were designed.

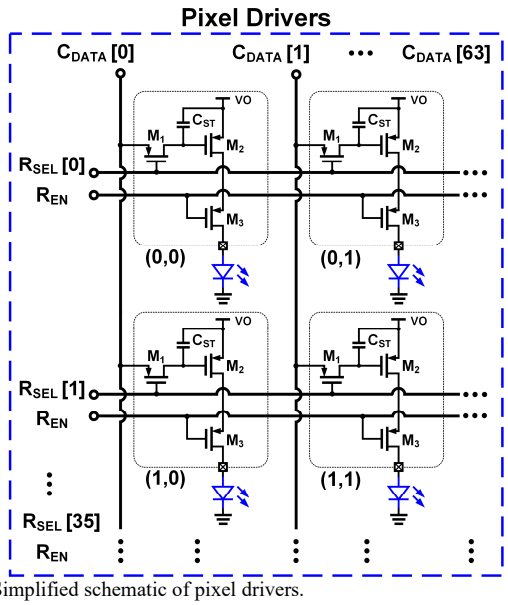
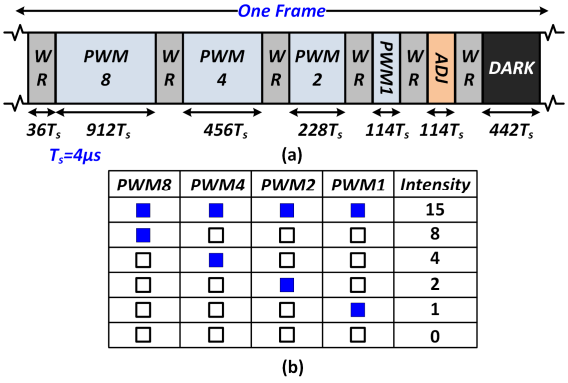


Fig. 8. Simplified schematic of pixel drivers.



PWM8	PWM4	PWM2	PWM1	Intensity
■	■	■	■	15
■	□	□	□	8
□	■	□	□	4
□	□	■	□	2
□	□	□	■	1
□	□	□	□	0

(b)

Fig. 9. (a) timing diagram of one display frame; (b) pixel intensity control with 4-bit PWM selection.

A. Pixel Drivers

Fig. 8 shows the simplified transistor level implementation of the pixel drivers. Each pixel driver occupies 40μm × 40μm area and consists of three PMOS transistors and one capacitor (3T1C). Voltage V_O is the output voltage of the hybrid regulator (typically 3.6V) and the input voltage of the pixel driver branch. M_2 is the main driving transistor using a 5V PMOS transistor. M_1 is the selection switch that enables the turning-on of M_2. The capacitor C_{ST} is connected between the gate of M_2 and V_O, to hold the gate V_{gs} voltage when switch M_2 is turned off. M_3 is controlled by the global enable signal R_{EN} to reset the whole panel of the pixels.

The operating principle is as follows. When one pixel is turned on, then a logic "0" enables the row selection signal R_{SEL}, turning on the corresponding M1 and the display data will be written from C_{DATA} to the V_{gs} of M_2. The voltage across C_{ST} controls the status of the main driving transistor M_2. The voltage is stored in the capacitor C_{ST} and be held during one frame.

The display data is updated through row-by-row progressive scanning. First, the first-row display information (64-bit) is written into the column driver in a series sequence, so loaded into data signal lines (from $C_{DATA}[0]$ to $C_{DATA}[63]$). Then, row selection signal $R_{SEL}[0]$ is set to low, enabling each C_{ST} of the first row to store data from C_{DATA} line. After that, $R_{SEL}[0]$ is set to high to finish the scanning of the first row. The same procedure is continuously repeated for the following rows (from $R_{SEL}[0]$ to $R_{SEL}[31]$). After all the pixels are loaded with the display information, R_{EN} is enabled to trigger and display the programmed image.

B. Display Control and 4-Bit Pixel Intensity Control

To control the intensity of each pixel so to form a picture, pulse-width modulation (PWM) is employed. Fig. 9(a) shows the timing diagram of one display frame. The refresh rate is et to be 100Hz so the period of one frame is 10ms. The period from the display data controller is T_s = 4μs. One frame consists of six sub-frames with different intensities. Each sub-frame starts with a WR (write) period, which has 36×T_s=144μs to scan 36 rows in this work. The data signals were loaded in one T_s period. The LED pixel intensity control period PWM8/4/2/1 is chosen by the picture data and brightness requirement, enabling a maximum 4-bit PWM intensity resolution control (from 0 to 15) as shown in Fig. 9(b). After the PWM1 sub-frame, ADJ (adjustable) sub-frame is set to compensate for the brightness across process, voltage, and temperature (PVT) variations. At last, a DARK sub-frame is added to improve the contrast ratio. The display data was processed and sent by an Arduino DUE micro-controller.

V. AMLED Array Design and System Integration

The detailed processes of AMLED array fabrication and flip-chip bonding packing are discussed in this section.

A. AMLED Array fabrication

The AMLED array chip consists of 36 × 64 pixels with a 40μm pitch size, fabricated using blue LED epilayers which are grown on 6-inch Silicon (111) substrate. The epilayers include a 1.2-μm-thick graded AlGaN buffer layer, a 0.5-μm-thick undoped GaN layer, a 2-μm-thick Si-doped n-type GaN layer, ten pairs of InGaN/GaN multiple quantum wells (MQWs), and a 0.2-μm-thick Mg-doped p-type GaN layer [35]. As depicted in Fig. 10(a), the epilayers were isolated to form individual micro-LEDs, each of which contained one independent p-type electrode and common n-type electrode. The metal stacks in the p-type electrode were designed to achieve multiple functions. First, a layer of indium tin oxide (ITO) was patterned on top of the micro-LEDs, based on a self-align process [26], to establish ohmic contact to p-GaN. Second, Cr/Al-based metal layers were deposited on both the ITO patterns and n-GaN area, to spread current for the micro-LED and build ohmic contact to n-GaN, respectively. Third, a bilayer of TiW/Cu was sputtered as seed layer thus Cu/Sn bumps could be electroplated as bonding metal. A layer of SiO2 is applied to passivate the sidewall of the micro-LED, using plasma enhanced chemical vapor deposition (PECVD).

After the fabrication of the micro-LED array, the Si growth substrate is grinded down to 150 μm to speed up the substrate removal process after the flip-chip bonding.

The measured I-V curve of single LED pixel is shown in Fig. 10(b). The current of the LED is 30 μA when the forward bias voltage is 3.2 V, and reverse leakage current is less than 5 pA in reverse bias region [26]. The measured light wavelength is 440 nm at the peak intensity.

B. Au-Free Flip-Chip Bonding Package

Conventionally, to achieve a high connection reliability, Au metal material is usually used in the flip-chip bonding techniques (e.g. Au/In [21, 22], Au/Au [23] and Au/Sn [24]) were reported and adopted in AMLED packages. Using a thick Au layer results in a higher cost, which is not desired in our proposed cost-effective AMLED micro-display system. In such a case, we proposed to use one Cu/Sn metal bonding (Au-free) [26], that can achieve similar reliability but lower cost comparing to the Au metal bonding scheme [21-24].

Fig. 11 shows the process on AMLED array chip. In this work, a Cu/Sn bump electron-plating technique with two steps was developed to obtain a high bump quality to avoid bump shorting issues. First, 5μm-thick Cu square bumps of 30μm × 30μm size were electro-plated on the top side of the AMLED array chip. Second, smaller 5μm-thick Cu/Sn bumps of a 20μm diameter were plated on top of Cu bumps. Fig. 11(b) shows the zoomed-in image of the plated bumps on the AMLED array chip, which have a pitch size of 40μm. The scanning electron microscope (SEM) photo of the dump is shown in Fig. 11(c). The size and the material of bumps can be cleared observed.

The next step is the process on silicon driving chip as shown

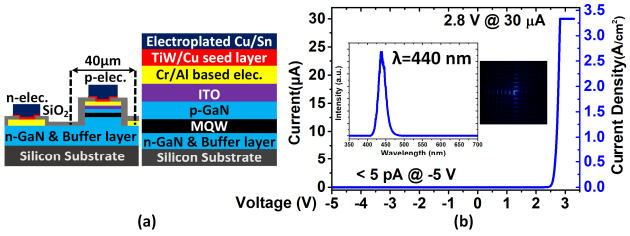


Fig. 10. (a) Vertical structure of AMLED fabrication layer; (b) I-V curve of one LED pixel [26].

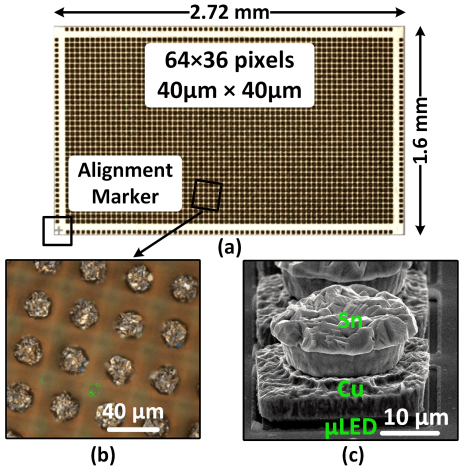


Fig. 11. (a) Micrograph of the AMLED array chip; (b) Micrograph of the Cu/Sn bumps on the top of AMLED array chip; (c) SEM photo of Cu/Sn bumps [21], [26].

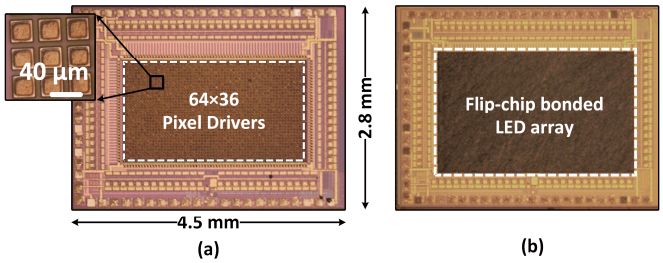


Fig. 12. (a) The micrograph of the PAD after additional Ti/Cu bilayer on silicon driving chip; (b) The integrated display system after the AMLED array chip bonded on the silicon driving chip using flip-chip packing [26].

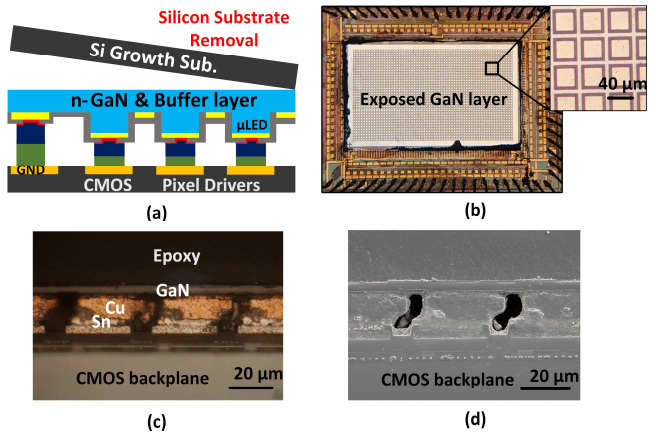


Fig. 13. (a) Silicon substrate removal process; (b) micrograph of the integrated chip after silicon substrate removal; (c), (d) micrograph and SEM image of the vertical structure of the bonding package [26].

in Fig. 12. In the center of the silicon driving chip, pads with 30μm × 30μm (40μm pitch) were fabricated. Before the growth of other layers, the pads were slightly wet etched to remove all the possible residue of the passivation layer. In this 0.18μm standard CMOS process, the top metal for the pad was fabricated by Al, so inherently it can not be bonded with Sn on the micro-LED side. To overcome this issue, a buffer layer that uses Ti/Cu (100nm/1μm) was grown on top of the Al-based pixel driver pads (connecting to the anode of AMLED pixel) and the ground pad (connecting to the common cathode of AMLED pixel). Then AMLED array chip was flip-chip bonded to the silicon driving chip with a force of 5N at 280°C for 30s. Two chips are aligned by reserved alignment markers as shown in Fig. 12(b).

Fig. 13 illustrates the final step at AMLED array to expose the LED display region. The silicon growth substrate (on the top now) was removed using SF_6 by reactive ion etching (RIE). The silicon RIE will automatically stop at the AlN buffer layer since AlN is highly sensitive to silicon. As a result, as shown in Fig. 13(b), a smooth and crack-free AMLED display region is obtained.

In summary, Fig. 13 (c) and (d) show the micrograph and SEM image indicating the vertical structure of the flip-chip bonding technique. It can be observed that the AMLED array chip is well supported by the silicon driving chip through our proposed Cu/Sn bumps. The alignment between each AMLED pixel and pixel driver is well established without any short

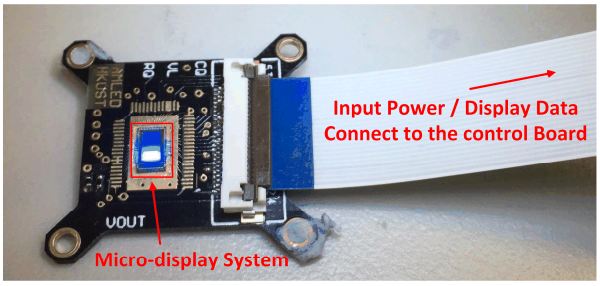


Fig. 14. PCB test board of AMLED display system with flexible cable.

connection between neighboring pixels.

VI. Measurement Results

To demonstrate this system, the silicon driving chip and the AMLED array chips were fabricated by standard 0.18 µm 1P6M CMOS process and in-house GaN process separately. Before the system integration, a fully-integrated SC power converter was firstly fabricated to verify the functionality and performance which has been reported in [33]. And based on the first-run result, the pixel driver was combined with power converter, and fabricated again as the silicon driving chip.

The size of the AMLED array chip was measured with 1.6 mm × 2.72 mm (Fig. 11(a)), while the silicon driving chip was measured 2.8 mm × 4.5 mm (Fig. 12(a)). As shown in Fig. 14, the micro-display was placed on a PCB and bond wires were used to connect power and display data signals. A flexible cable was used to connect micro-display to the controller. In this section, we summarize the measurement results of the hybrid voltage regulator, micro-LEDs, and image display.

A. Hybrid Voltage Regulator Measurement

In Fig. 15, the measured output ripple voltage ΔV_O of the integrated hybrid voltage regulator is shown. Under SC mode (VCR=4/3× or 3/2×), the maximum ΔV_O was 50mV. When the regulator is under the linear mode, the ripple voltage is negligible. In summary, the ripple voltages were all less than 50mV under the full-load condition (I_O=60mA) and different input voltages V_{IN}, while the power converter does not require any external loading capacitor.

Fig. 16 shows the measured efficiency versus the input voltages under full (I_O = 60mA) and half (I_O = 30mA) brightness conditions. When the voltage regulator is in the SC modes (VCR = 4/3× or 3/2×), a 78% peak efficiency was achieved in 3/2× mode (V_{IN} = 2.7V and V_O = 3.6V). When the voltage regulator is in the linear mode, as high as 91% peak efficiency can be achieved under (V_{IN} = 3.7V and V_O = 3.6V) condition. Since for SC converter and linear regulator, a higher efficiency can be obtained when V_O/V_{IN} is close to the ideal VCR. The integrated hybrid voltage regulator can deliver a maximum power of 216 mW (60mA @ 3.6V), and has a 70.4 mW/mm^2 power density.

The performance of proposed integrated hybrid voltage regulator is summarized and compared with state-of-the-art works in Table I. Thanks to the stacking transistors technique

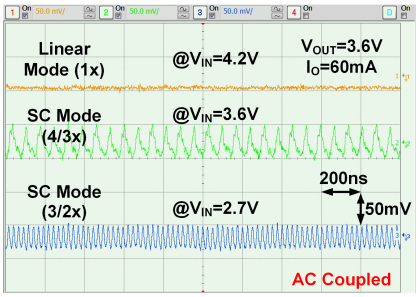


Fig. 15. Measured steady-state output voltage and voltage ripple versus I_O and V_{IN} [25].

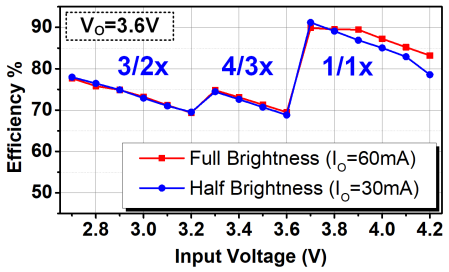


Fig. 16. Measured efficiency of hybrid voltage regulator versus input voltages [25].

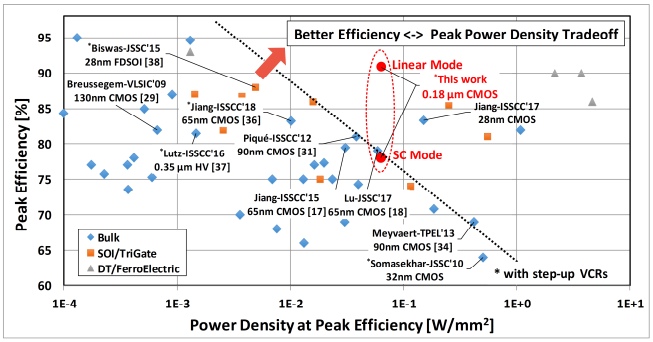


Fig. 17. Performance survey of state-of-the-art integrated SC converters [39].

and power stage efficiency optimization, our integrated hybrid voltage regulator achieved much higher power density while maintaining similar peak efficiency comparing to [36], [37]. Our integrated hybrid voltage regulator has more interleaving phases and higher efficiency while delivering more current than [38]. Fig. 17 shows the recent survey [39] that compares performance of state-of-the-art works regarding the peak efficiency versus power density. This work in two modes were marked as red points. It can be observed that our work is locating at the performance tradeoff line and is better than most of works using standard bulk CMOS processes. Moreover, when comparing to [18] and [36] in Table I, our work achieved much lower output voltage ripple (1.38% to 3% and 7.5%) without any external capacitors. In summary, our integrated voltage regulator demonstrates a good tradeoff between power efficiency and power density, while keeps a low cost in 0.18µm CMOS technology and lower output voltage ripple.

B. Monochromatic AMLED System Measurement

To compare the display quality and crosstalk of proposed GaN-on-silicon with conventional GaN-on-sapphire AMLED arrays, Fig. 18 shows two AMLED array chips fabricated using silicon substrate (Fig. 18(a)) and sapphire substrate (Fig. 18(b)).

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART FULLY INTEGRATED CONVERTERS

Work	This work	JSSC`17 [18]	ISSCC`18 [36]	ISSCC`16 [37]	JSSC`15 [38]
Technology	**0.18 µm Bulk**	65 nm Bulk	65 nm Bulk	0.35 µm HV Bulk	28 nm FDSOI
Topology	**Step-Up SC & LDO**	Step Down SC	Step-Up & Down SC	Step-Up & Down SC	Step-Up SC
Cap. Type	**MOS, MIM**	MOS, MIM, MOM	MOS MIM	MIM	MOS, MOM
Ideal VCRs	**3/2, 4/3, 1**	1/2, 2/3, 3/4	11 buck 13 boost	8 buck 9 boost	5/2, 2/1, 3/2
# of VCR	**3**	3	24	17	3
# of C_{fly}	**3**	3	20	4	4
# of Interleaving Phases	**87**	123	2	1	4
V_{IN}	**2.7-4.2V**	1.6-2.2V	0.22-2.4V	2-13V	1V
V_{OUT}	**3.6V**	0.6-1.2V	0.85-1.2V	5V	1.2-2.4V
$P_{OUT, MAX}$	**216mW**	152mW	34mW	10mW	2.7mW
η_{peak}	**78%* / 91%+**	79.0%	83.2%	81.5%	88%
Active Area	**3.07mm²**	0.84mm²	2.42mm²	6.8mm²	0.114mm²
Power Density @ η_{peak}	**70.4 mW/mm²**	50 mW/mm²	10.2 mW/mm²	1.47 mW/mm2	4.9mW/mm²
Internal C_{OUT}	**248pF**	~200pF#	0	~600pF#	300pF
Regulated	**Yes**	Yes	Yes	Yes	No
Max. ΔV_O%	**1.38%**	3%	7.5%	N/A	N/A

* Peak efficiency of the SC mode; + Peak efficiency of the linear mode; # Extracted from papers.

To have a fair comparison, the driving currents of these two chips were set to be similar, so that they have similar output powers around 200µW. From zoomed-in patterns, the AMLED array with sapphire substrate has an obvious blue background since the light has more reflection within sapphire. In contrast, the AMLED array with silicon substrate has a much darker background. Moreover, Fig. 18(c) measures the normalized intensity of AA' and BB' lines. It shows that the GaN-on-silicon AMLED array has much less crosstalk, resulting in a better contrast ratio than the GaN-on-sapphire counterpart.

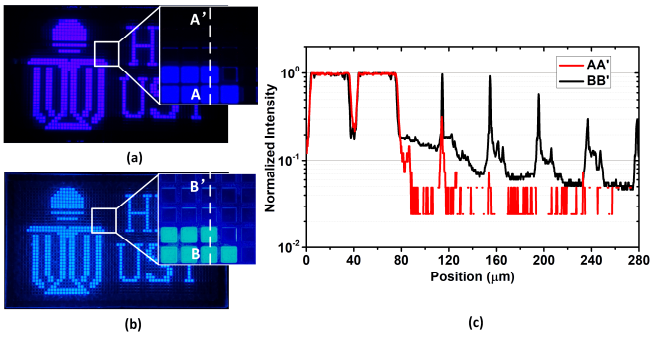


Fig. 18. Displayed and zoomed-in pattern of (a) AMLED array with silicon growth substrate removal; (b) AMLED array with conventional sapphire growth substrate; (c) Normalized intensity profiles along AA' and BB' [26].

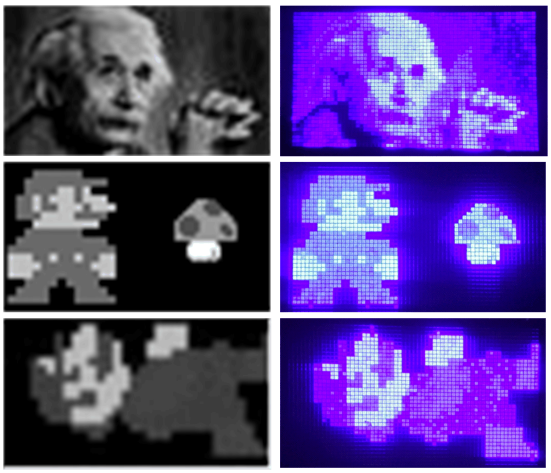


Fig. 19. Source files (left) and its corresponding display images (right) shown in the single color blue micro display system [25, 26].

The display image data was processed and sent by an Arduino DUE microcontroller board. A flexible cable connects the controller board and the display board. Fig. 19 shows the image displayed by a single blue color AMLED array. 4-bit grayscale control was used, and all images can be rendered. Almost no dead pixel was observed, resulting in a near 100% bonding yield rate was achieved. The micro-display is also able to display a video. As a result, the functionalities and performances were fully verified, and a highest integration level was achieved compared with start-of-the-art AMLED works [1], [2], [21-22].

VII. CONCLUSION

The fully integrated active matrix LED micro-display system is demonstrated in this paper, using a fully on-chip hybrid voltage regulator, GaN-on-silicon substrate based micro-LEDs, and Au-free flip-chip package. The on-chip hybrid voltage regulator consists of a step-up switched-capacitor power converter and a step-down linear regulator that can support a standard lithium-ion (Li-ion) battery input voltage range of 2.7V to 4.2V. The regulator achieves peak efficiencies of 91% at linear mode and 78% at SC mode, with a higher than 78% averaged efficiency and a maximum output power of 216mW. GaN-on-silicon AMLED arrays with 36 × 64 pixels were fabricated with a pitch size of 40µm. The contrast ratio of the GaN-on-Silicon micro-LED micro-display is improved while the crosstalk is significantly suppressed. Cu/Sn bump based flip-chip technique was proposed to replace Au employed techniques, achieved comparable reliability but lower cost.

This prototype achieved a highest integration level compared with start-of-the-art AMLED works, and demonstrates a low-cost integrated micro-display system that simply operates with a Li-ion battery, and suggests feasible manufacturability

and tremendous potential for large-scale and massive production in both consumer electronics and industrial applications (such as AR, VR and industry X.0 applications) in the future.

REFERENCES

[1] Z. J. Liu, et al., "A novel BLU-free full-color LED projector using LED on silicon micro-displays," *IEEE Photonics Technology Letters*, vol. 25, no. 23, pp. 2267–2270, 2013.

[2] Y.-Z. Lin *et al.*, "Active-Matrix Micro-LED Display Driven by Metal Oxide TFTs Using Digital PWM Method," *IEEE Trans. Electron Devices*, vol. 68, no. 11, pp. 5656–5661, Nov. 2021.

[3] X. Zhang, et al., "Active matrix monolithic micro-LED full-color micro-display," *J. Soc. Inf. Display*, vol. 29, no. 1, pp. 47–56, Jan. 2021.

[4] W. C. Chong, et al., "1700 pixels per inch (PPI) passive-matrix micro-LED display powered by ASIC," in *Proc. IEEE Compound Semicond. Integr. Circuit Symp.*, 2014, pp. 1–4.

[5] S. Zhang et al., "Directly color-tunable smart display based on a CMOS controlled micro-LED array," in *Proc. IEEE Photon. Conf.*, Sep. 2012, pp. 435–436.

[6] D. Tsonev et al., "A 3-Gb/s single-LED OFDM-based wireless VLC link using a gallium nitride μLED," *IEEE Photon. Technol. Lett.*, vol. 26, no. 7, pp. 637–640, Jan. 2014.

[7] S. Martin, "Milestone in the History of Field-Effect Liquid Crystal Displays and Materials", *Jpn. J. Appl. Phys.*, vol. 48, no. 3S2, Mar. 2009.

[8] B. Geffroy, et al., "Organic light-emitting diode (OLED) technology: materials, devices and display technologies", *Polym. Int.*, vol. 55, no. 6, pp. 572-582, Jun. 2006.

[9] "TPS65632: Triple-Output AMOLED Display Power Supply," *Texas Instruments Datasheet*, Mar. 2015.

[10] F. Mao *et al.*, "A hybrid single-inductor bipolar-output DC-DC converter with floating negative output for AMOLED displays," *IEEE J. Solid-State Circuits*, vol. 56, no.9, pp. 2760–27691, Sep. 2021.

[11] X. Liu, C. Huang, and P. K. T. Mok, "A high-frequency three-level buck converter with real-time calibration and wide output range for fast-DVS," *IEEE J. Solid-State Circuits*, vol. 53, no. 2, pp. 582–595, Feb. 2018.

[12] C. Huang and P. K. T. Mok, "A 100 MHz 82.4% efficiency package-bondwire based four-phase fully-integrated buck converter with flying capacitor for area reduction," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 2977–2988, Dec. 2013.

[13] G. V. Piqué, H. J. Bergveld, and E. Alarcon, "Survey and benchmark of fully integrated switching power converters: switched-capacitor versus inductive approach," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4156–4167, Sep. 2013.

[14] Y. Li, et al., "AC-coupled stacked dual-active-bridge DC–DC converter for integrated lithium-ion battery power delivery," *IEEE J. Solid-State Circuits*, vol. 54, no. 3, pp. 733–744, Mar. 2019.

[15] Z. Hua and H. Lee, "A Reconfigurable dual-output switched-capacitor DC-DC regulator with sub-harmonic adaptive-on-time control for low-power applications," *IEEE J. Solid-State Circuits*, vol. 50, no. 3, pp. 724–736, Mar. 2015.

[16] M. Seeman and S. Sanders, "Analysis and optimization of switched-capacitor DC-DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.

[17] J. Jiang, et al., "A 2-/3-phase fully integrated switched-capacitor DC-DC converter in bulk CMOS for energy-efficient digital circuits with 14% efficiency improvement," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2015, pp. 366-367.

[18] Y. Lu, J. Jiang, and W.-H. Ki, "A multiphase switched-capacitor DC–DC converter ring with fast transient response and small ripple," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 579–591, Feb. 2017.

[19] J. Jiang, W.-H. Ki, and Y. Lu, "Digital 2-/3-phase switched capacitor converter with ripple reduction and efficiency improvement", *IEEE J. Solid-State Circuits*, vol. 52, no. 7, July 2017.

[20] F. Su, W.-H. Ki, and C.-Y. Tsui, "Regulated switched-capacitor doubler with interleaving control for continuous output regulation," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1112–1120, Apr. 2009.

[21] X. Li, et al., "Design and characterization of active matrix LED microdisplays with embedded visible light communication transmitter," *IEEE J. Lightwave Technology*, vol. 34, no. 14, pp. 3449–3457, Jul. 2016.

[22] L. Wu et al., "An AMLED microdisplay driver SoC with built-in 1.25-Mb/s VLC transmitter," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2015, pp. c328–c329. (VLC)

[23] C.-C. An, et al., "Study on flip chip assembly of high density micro-LED array," in *Proc. 6th International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT)*, 2011, pp. 336–338.

[24] C. Choi *et al.*, "Localizing seizure activity in the brain using implantable micro-LEDs with quantum dot downconversion," *Adv. Mater. Technol.*, vol. 3, no. 6, p. 1700366, Jun. 2018.

[25] J. Jiang et al., "Fully-integrated AMLED micro display system with a hybrid voltage regulator," in *Proc. IEEE Asian Solid-State Circuits Conf.*, Jan. 2017, pp. 277–280.

[26] X. Zhang et al., "Active matrix monolithic LED micro-display using GaN-on-Si epilayers," *IEEE Photonics Technology Letters*, vol. 31, no. 11, pp. 865–868, Jun. 2019.

[27] H.-P. Le, S. R. Sanders and E. Alon, "Design techniques for fully integrated switched-capacitor DC-DC converters," *IEEE J. Solid-State Circuits*, vol. 46, no. 9, pp. 2120–2131, Sep. 2011.

[28] H.-P. Le, J. Crossley, S. R. Sanders and E. Alon, "A sub-ns response fully integrated battery-connected switched-capacitor voltage regulator delivering 0.19W/mm^2 at 73% efficiency," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2013, pp. 372–373.

[29] T. Breussegem and M. Steyaert, "A 82% efficiency 0.5% ripple 16-phase fully integrated capacitive voltage doubler," in *Proc. IEEE Symp. VLSI Circuits*, Jun. 2009, pp. 198-199.

[30] D. Somasekhar et al., "Multi-phase 1 GHz voltage doubler charge pump in 32 nm logic process," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 751–758, Apr. 2010.

[31] G. V. Piqué, "A 41-phase switched-capacitor power converter with 3.8mV output ripple and 81% efficiency in baseline 90nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2012, pp. 98–100.

[32] H. Meyvaert, et al., "A light-load-efficient 11/1 switched-capacitor DC-DC converter with 94.7% efficiency while delivering 100 mW at 3.3 V," *IEEE J. Solid-State Circuits*, vol. 50, no. 12, pp. 2849–2860, Dec. 2015.

[33] J. Jiang, X. Liu, W.-H. Ki, P. K. T. Mok, and Y. Lu, "A multiphase switched-capacitor converter for fully integrated AMLED microdisplay system," *IEEE Trans. Power Electronics*, vol. 35, no. 6, pp. 6001–6011, Jun. 2020.

[34] H. Meyvaert, T. V. Breussegem, and M. Steyaert, "A 1.65 W fully integrated 90 nm bulk CMOS capacitive DC-DC converter with intrinsic charge recycling," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4327–4334, Sep. 2013.

[35] X. Zou, et al., "Vertical LEDs on rigid and flexible substrates using GaN-on-Si epilayers and Au-free bonding," *IEEE Trans. Electron Devices*, vol. 63, no. 4, pp. 1587–1593, Apr. 2016.

[36] Y. Jiang, et al., "A 0.22-to-2.4V-input fine-grained fully integrated rational buck-boost SC DC-DC converter using algorithmic voltage-feed-in (AVFI) topology achieving 84.1% peak efficiency at 13.2mW/mm^2" in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2018, pp. 422–424.

[37] D. Lutz, P. Renz, and B. Wicht, "A 10mW fully integrated 2-to-13V-input buck-boost SC converter with 81.5% peak efficiency," in *Proc. IEEE Intl. Solid-State Circuits Conf.*, Feb. 2016, pp. 224–225.

[38] A. Biswas, Y. Sinangil, and A. P. Chandrakasan, "A 28 nm FDSOI integrated reconfigurable switched-capacitor based step-up DC-DC converter with 88% peak efficiency," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1540–1549, Jul. 2015.

[39] M. Steyaert, et al., "DCDC performance Survey", [Online]. Available: http://homes.esat.kuleuven.be/~steyaert/DCDC_Survey/DCDC_PS.html