Small V_{th} Shift and Low Dynamic R_{ON} in GaN MOSHEMT With ZrO_2 Gate Dielectric

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***Abstract*— The OFF-state stress-induced threshold voltage (V_{th}) instability and dynamic ON-resistance (R_{ON}) of GaN metal-oxide-semiconductor high-electron mobility transistor (MOSHEMT) with ZrO_2 gate dielectric are thoroughly investigated. Upon negative gate bias stressing, a small threshold voltage shift of −0.31 V is observed and the deviation is attributed to the emission of electrons at the ZrO_2/AlGaN interface. An emission activation energy of 0.28 eV and a capture activation energy of 0.30 eV are extracted by threshold voltage transient spectroscopy performed at various temperatures. When the device is exposed to OFF-state drain–source bias stressing, the drain current is found to decrease despite negative shift of V_{th}. A low dynamic R_{ON} of 2.05 is obtained by time-resolved measurements, given a 50-V drain voltage stressing for a duration of 100 s. The decrease in forward conductance is related to the capture of electrons in the access region, with a capture activation energy of 0.18 eV revealed by temperature-dependent drain current transient (DCT) analysis. The results indicate that high-quality ZrO_2 represents an attractive high-*k* gate dielectric option for GaN MOSHEMTs in power switching electronics.**

***Index Terms*— Dynamic ON-resistance (R_{ON}), GaN, metal–oxide–semiconductor high-electron mobility transistor (MOSHEMT), threshold voltage (V_{th}) instability, ZrO_2 dielectric.**

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I. Introduction

III-N-BASED high-electron mobility transistors (HEMTs) are promising candidates for next-generation high-frequency and high-power applications due to their unique material properties, including large energy bandgap, high-electron saturation velocity, high-critical breakdown electric field, and high-temperature stability. However, gate leakage and drain current collapse in HEMTs with Schottky-type gate greatly hindered their applications in power conversion [1], [2]. Replacing the Schottky-type gate with a metal–oxide–semiconductor (MOS) structure can significantly suppress gate leakage, giving rise to a large gate swing and improved terminal stability. Various gate dielectrics have been utilized to fabricate III-N MOSHEMT or MISHEMT, including SiO_2, SiN_x, Al_2O_3, and so on [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14].

In particular, high-*k* gate dielectrics have been extensively introduced in MOSHEMTs to enhance transconductance and minimize OFF-state leakage current. ZrO_2 is highly promising among the available high-*k* gate dielectric options due to its high dielectric constant (20–30), large bandgap (7.8 eV), excellent thermal stability, and large conduction band offset [15], [16], [17], [18]. With high-quality ZrO_2 gate dielectric by atomic-layer deposition (ALD), GaN MOSHEMTs exhibited an outstanding ON/OFF current ratio of 5×10^{10} and a low dynamic-to-static ON-resistance (R_{ON}) ratio of 1.78 at the OFF-state V_{ds} of 600 V [16]. In comparison with a Schottky-gate HEMT, it was revealed that the gate leakage of a ZrO_2-MOSHEMT was suppressed by four orders of magnitude [18]. Using a novel recess-free barrier engineering technique, ZrO_2 has been successfully incorporated in fabricating an *E*-mode GaN MOSHEMT [15]. This unique technique achieved a large threshold voltage (V_{th}) over 2 V and a low R_{ON}.

Despite the fact that dc performance of GaN MOSHEMTs with a ZrO_2 gate dielectric has been well documented, dynamic characteristics, including V_{th} instability and dynamic R_{ON}, have not been thoroughly investigated. In addition, time-resolved V_{th} shift and forward conductance degradation at various temperatures still remain unclear.

In this work, a comprehensive study on threshold voltage instability and dynamic R_{ON} of GaN MOSHEMTs with a ZrO_2 gate dielectric layer is reported. First, threshold voltage instabilities of GaN MOSHEMT upon various gate and drain bias voltages were investigated. Subsequently, temperature-dependent threshold voltage transient spectrums during the stressing and recovery process were analyzed. Furthermore, time-resolved R_{ON} for different stressing voltages and

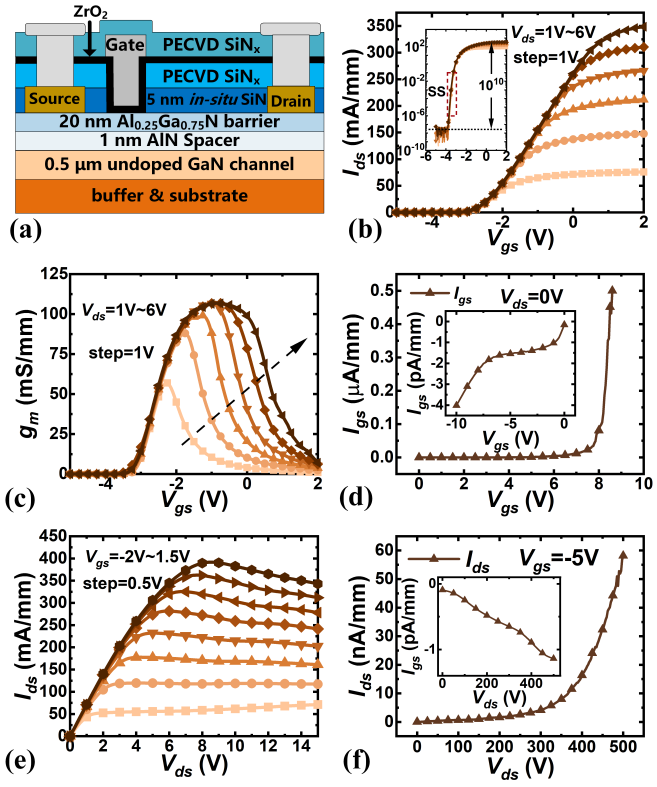

Fig. 1. (a) Cross-sectional schematic of GaN MOSHEMT. (b) Transfer (inset: logarithmic plots). (c) Transconductance, (d) forward gate leakage current (inset: reverse gate leakage current), (e) output characteristics, and (f) OFF-state I_{ds} (inset: OFF-state I_{ds}) of GaN MOSHEMT.

temperatures was investigated. Finally, the degradation of drain current was also revealed by drain current transient (DCT) spectroscopy. The small V_{th} shift and low dynamic R_{ON} in MOSHEMT showed ZrO_2 is a promising high-k dielectric for power switching electronics.

II. Device Fabrication and Method

Fig. 1(a) showed the schematic cross section of the fabricated GaN MOSHEMT structure with ZrO_2 as a dielectric. The AlGaN/GaN HEMT structure was grown on a 6-in n-type Si (111) substrate by metal–organic chemical vapor deposition (MOCVD). The epitaxial structures, from bottom to top, were as follows: a 0.3-μm AlN, a 1-μm step-graded AlGaN, a 2.5-μm carbon-doped GaN, a 0.5-μm unintentionally doped GaN channel layer, a 1-nm AlN spacer layer, a 20-nm $Al_{0.25}Ga_{0.75}N$ barrier layer, and a 5-nm in-situ SiN_x cap. Hall measurement conducted at room temperature revealed a 2-D electron gas (2DEG) density of 1.05×10^{13} cm^{-2} and an electron mobility of 1730 cm^2/V·s [16]. The source/drain ohmic metallization was formed before depositing 100-nm SiN_x passivation layer using plasma-enhanced chemical vapor deposition (PECVD). This PECVD SiN_x layer grown on in-situ SiN_x was used as an additional passivation layer to suppress current collapse [19]. Next, mesa isolation was performed through argon ion implantation. Using a low-power (20 W) SF_6-based inductively coupled plasma dry etch, the gate region was exposed by removing both the PECVD and the in-situ SiN_x. Tetrakis (ethylmethylamino) zirconium and H_2O vapor were used as precursors in the ALD process to

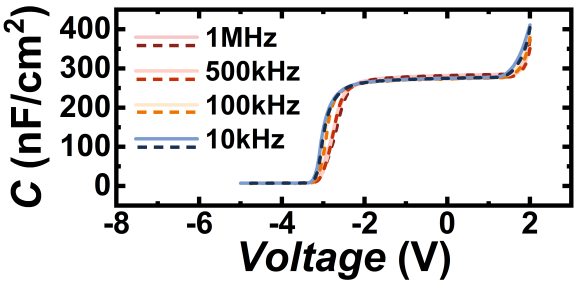

Fig. 2. Double sweep C–V characteristics of GaN MOSHEMTs at different frequencies. Dashed line represents the down-sweep measurements.

deposit a 28-nm ZrO_2 dielectric at 200 °C after cleaning the barrier surface with a diluted HCl solution (HCl:H_2O = 1:3). Subsequently, Ni/Au-based gate metal was formed and another 300-nm PECVD SiN_x was grown as a final passivation layer. The second passivation layer was used to passivate the ZrO_2 dielectric layer, decreasing the surface traps and enhancing the drain breakdown voltage. Finally, the regions in SiN_x at source/drain areas were etched prior to the deposition of the Al-based pad metal. The device in this article featured a gate length L_g, a gate–source distance L_{gs}, a gate–drain distance L_{gd}, and a gate width W_g of 2, 3, 20, and 200 μm, respectively.

III. Results and Discussion

Fig. 1(b) illustrated the transfer characteristics of GaN MOSHEMT with a ZrO_2 dielectric layer. The threshold voltage, defined at a drain current of 1 mA/mm, was extracted to be −3.0 V from the transfer curves. The ON/OFF current ratio of 10^{10} and subthreshold swing of 90 mV/decade were achieved for the MOSHEMTs [inset in Fig. 1(b)], indicating outstanding charge modulation of MOS gate structures. The device featured a peak transconductance of 106.75 mS/mm with V_{ds} = 6 V, as depicted in Fig. 1(c). Fig. 1(d) displayed the $I_{gs} - V_{gs}$ characteristic, where the leakage remained below 0.5 μA/mm until V_{gs} reaches 8.65 V, and the device exhibited a low gate leakage of 4 pA/mm at −10 V [inset in Fig. 1(d)]. Fig. 1(e) showed the output characteristics, where maximum drain current density of 390.2 mA/mm was obtained at V_{gs} = 1.5 V. Extracted R_{ON} of the device was 14 Ω·mm at V_{gs} = 1.5 V. Fig. 1(f) showed the OFF-state breakdown characteristics. The highest drain breakdown voltage of the device exceeds 500 V, as defined at the leakage current of 10 μA/mm. The OFF-state I_{gs} leakage current was four orders of magnitude lower than the I_{ds} leakage current at V_{ds} = 500 V, confirming the excellent current blocking capability of the MOS gate [inset in Fig. 1(f)].

Fig. 2 showed the double sweep capacitance–voltage (C–V) curves measured on a MOSCAP (MOS capacitor) with a diameter of 200 μm at various frequencies ranging from 50 kHz to 1 MHz. As increasing voltage bias, the C–V curves exhibited two distinct rising steps. The gate voltage at the first rising step corresponded to the 2DEG formation, and the second rising step was associated with the spill-over of electrons from the 2DEG channel to the barrier surface. In addition, the C–V curves exhibited a sharp transition from the deep depletion to accumulation and a small hysteresis of 50 mV, indicating high quality of the ZrO_2 dielectric film and low trap density at the interface between ZrO_2 and AlGaN barrier layer.

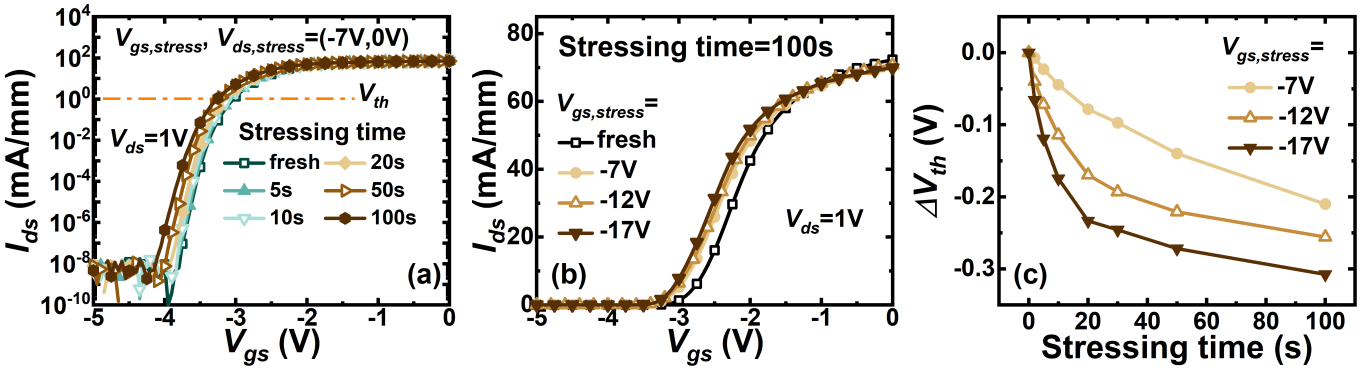

Fig. 3. (a) NBTI measurements with different stressing durations for $V_{gs,stress} = -7$ V. (b) Transfer curves with different reverse gate bias for stressing time 100 s. (c) Variation of V_{th} as a function of stressing time.

TABLE I
COMPARISON OF NEGATIVE V_{th} SHIFT AMPLITUDE BETWEEN THIS WORK AND OTHER GAN MOSHEMTS

Ref.	Dielectric	$\lvert V_{gs,stress}-V_{th}\rvert$	$\lvert\Delta V_{th}\rvert$
This work	28-nm ZrO_2	14 V	0.31 V
[11]	20-nm Al_2O_3	8 V	1.00 V
[27]	47-nm *in-situ* SiN_x	15 V	2.03 V
[26]	30-nm Al_2O_3	6 V	0.20 V
[28]	30-nm *in situ* SiN_x	6 V	0.20 V

Fig. 3 depicted the negative bias-induced threshold-voltage instability (NBTI) measurement results with different stressing durations for a fixed OFF-state voltage. As shown in Fig. 3(a), an OFF-state stressing of −7 V ($V_{gs,stress} = -7$ V) induced a negative shift in the threshold voltage of the device. A small ΔV_{th} of −0.21 V was observed as the stressing time was extended to 100 s. Fig. 3(b) illustrated the results of transfer curves upon different OFF-state stressing bias voltages for 100 s. When the device was subjected to a higher gate stressing voltage of −12 V, a larger negative shift of −0.26 V was noticed. Fig. 3(c) summarized the variation of V_{th} as a function of stressing time. After the device was subjected to a harsh stress condition ($V_{gs,stress} = -17$ V) for 100 s, a −0.31-V shift in V_{th} was measured. In previous literatures, positive V_{th} shift has been extensively observed and attributed to electron trapping in traps at barrier/insulator interface or in oxide layer [7], [20], [21], [22]. Only a few studies reported negative V_{th} shift in GaN MOS or MIS structures [23], [24], [25], [26], [27]. Table I illustrated the comparison of negative shift in V_{th} between this work and GaN MISHEMTs with some other representative dielectrics. A gate-first devices showed a V_{th} shift of −2.03 V after stressing at an OFF-state bias of −30 V [27]. Devices with other dielectrics (including 30-nm Al_2O_3 [26] and 30-nm in-situ SiN_x [28]) achieved the V_{th} shift of 0.2 V with moderate OFF-state stressing ($\lvert V_{gs,stress} - V_{th}\rvert < 10$ V). In this work, a 28-nm ZrO_2 dielectric helped achieve a small ΔV_{th} of −0.31 V for a relatively larger OFF-state stressing $\lvert V_{gs,stress} - V_{th}\rvert = 14$ V. These results indicated that this device has good threshold voltage stability with a relatively large gate OFF-state stress.

The negative shift of V_{th} was attributed to the emission of electrons from traps in the gate dielectric and/or at the insulator/AlGaN interface [23]. When zero bias was applied

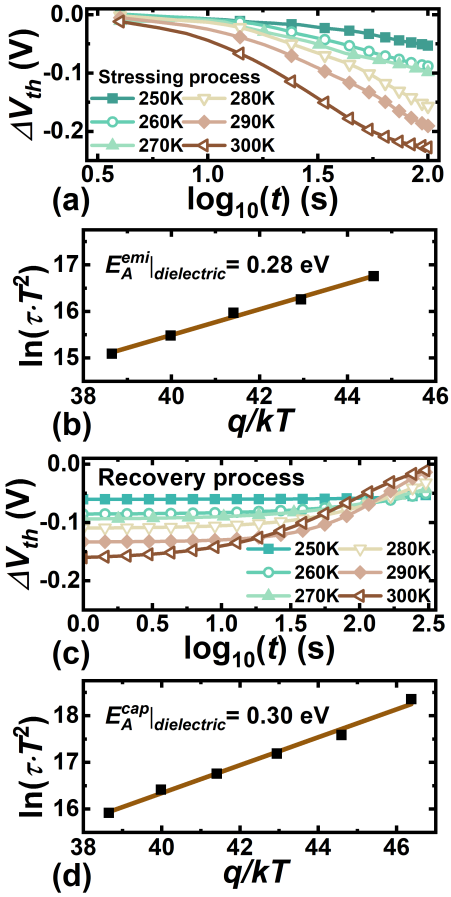

Fig. 4. (a) Measured ΔV_{th} transient spectroscopy for stressing process [$V_{gs,stress}$, $V_{ds,stress}$ = (−7 V, 0 V)] and (c) corresponding recovery process from 250 to 300 K. Arrhenius plot of (b) stressing and (d) recovery process.

to the device, trap states below the Fermi level were filled with electrons. These electrons depleted the 2DEG in the channel, which restrained the drain current of the device during the ON-state. However, when an OFF-state stressing voltage ($V_{gs,stress} < V_{th}$) was applied to the device, the electrons were emitted from trap states with energies above the Fermi level. The emission of electrons led to a negative V_{th} shift. The magnitude of $V_{gs,stress}$ and the duration of stressing also modulated the extent of V_{th} shift. With a longer stressing time and a larger $V_{gs,stress}$, a relatively larger V_{th} shift would be observed

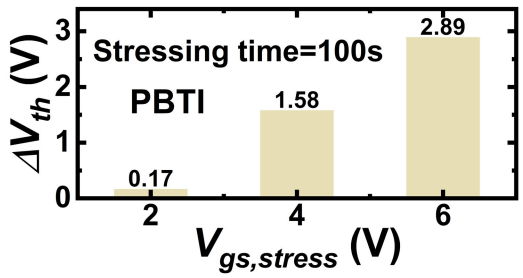

Fig. 5. Variation in V_{th} during PBTI experiments with different positive bias stress conditions.

[Fig. 3(c)]. In a separate deep-level transient spectroscopy (DLTS) measurement on a MOSCAP, the transient capacitance also displayed the emission process of traps, confirming the occurrence of electron emission when the device was subjected to an OFF-state stressing.

The ΔV_{th} transient spectrum was employed to extract activation energy of trap states related to the negative shift of V_{th}, as shown in Fig. 4. Fig. 4(a) illustrated the time-resolved stressing process of V_{th} at different temperatures. A moderate stress condition ($V_{gs,stress} = -7$ V) was selected to minimize the effects of transverse electric fields. During the stressing process, the device was periodically turned on to extract V_{th}. Each I_{ds}–V_{gs} measurements lasted for 30 μs with the drain voltage being fixed at 1 V. When applying the OFF-state stressing voltage of -7 V, the value of V_{th} became more negative. Meanwhile, the shifting amplitude of V_{th} was decreased as the temperature was reduced. ΔV_{th} transient followed a stretched exponential trend [$\sim\exp(-t/\tau)^{\beta}$] and the time constant (τ) of ΔV_{th} transient could be determined [23]. The coefficient β quantified the degree of deviation between the stretched exponential function and the ideal behavior. When the temperature decreased, a larger time constant was observed. After extracting time constants at different temperatures, the activation energy of traps can be obtained through the construction of the Arrhenius plot. The Arrhenius law takes the following form [29]:

$$\ln\left(\frac{T^2}{e_n}\right) = \frac{E_a}{k_B T} - \ln(\sigma_n \gamma) \tag{1}$$

where e_n is the emission rate, σ_n is the apparent cross section, γ_n is a material-dependent constant, T is the temperature, E_a is the activation energy, and k_B is the Boltzmann constant. As shown in Fig. 4(b), an emission activation energy $E_A^{\text{emi}}|_{\text{dielectric}}$ of 0.28 eV was extracted by fitting the Arrhenius plots [29]. During the recovery process, V_{th} would gradually recover to the initial state [Fig. 4(c)]. After a natural recovery for 300 s, the threshold voltage of the device almost completely restored at 300 K. As temperature decreased, it took a longer recovery time for the device to return to the initial value of V_{th}. The device scarcely recovered during the recovery process for 300 s at 250 K. The recovery of the device was caused by the recapture of electrons by unfilled traps. Similarly, a capture activation energy $E_A^{\text{cap}}|_{\text{dielectric}}$ of 0.30 eV was extracted for the traps in the gate region, as shown in Fig. 4(d).

Fig. 5 showed ΔV_{th} as a function of positive $V_{gs,stress}$ for a stressing time of 100 s in positive bias-induced threshold voltage instability (PBTI) experiment. When the device was subjected to a $V_{gs,stress}$ of 2 V for 100 s, a minor positive shift of 0.17 V was observed. With the increase of $V_{gs,stress}$, the offset of the threshold voltage rapidly reached 1.58 V. When a higher overdrive voltage was employed, the threshold voltage shifted to -0.1 V ($\Delta V_{th} = 2.9$ V) for a stressing time of 100 s. As further increasing $V_{gs,stress}$ or the stressing time, the threshold voltage of the device would even exceed 0 V. Unlike zero bias (initial state) and negative $V_{gs,stress}$ [Fig. 6(a) and (b)], the positive shift of V_{th} was related to electron capture from traps at the gate dielectric and/or insulator/AlGaN interface, when the device was subjected to a low positive gate stressing voltage ($V_{gs,stress} < 2$ V), as shown in Fig. 6(c). When the positive gate stressing voltage exceeded the spill-over voltage ($V_{gs,stress} > 2$ V), the electrons from the 2DEG flowed through the AlGaN barrier to the ZrO_2/AlGaN interface, forming a second channel and resulting in a large threshold voltage shift [Fig. 6(d)].

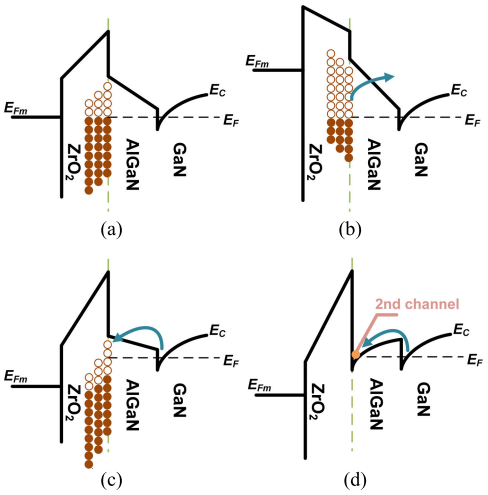

Fig. 6. Band diagram of the ZrO_2/AlGaN/GaN MIS structure with (a) initial state, (b) negative $V_{gs,stress}$, (c) positive $V_{gs,stress}$, and (d) overdrive $V_{gs,stress}$.

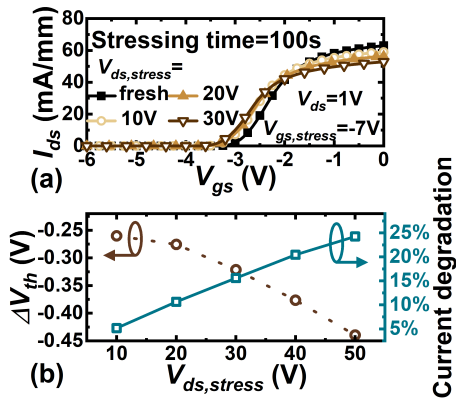

Fig. 7. (a) Transfer characteristics of the GaN MOSHEMT after various $V_{ds,stress}$ values for 100 s. (b) Variation of V_{th} and I_{ds} as a function of $V_{ds,stress}$ from the transfer curve of (a).

Fig. 7 showed the results of drain voltage-induced threshold voltage instabilities in GaN MOSHEMT with a ZrO_2 dielectric layer. Fig. 7(a) displayed the transfer curve of device, which was subjected to different $V_{ds,stress}$, with $V_{gs,stress}$ fixed at -7 V and a stressing time of 100 s. A simultaneous negative shift of V_{th} and reduction of drain current (at $V_{gs} = 0$ V) were observed. With the same $V_{gs,stress}$, a greater extent of V_{th} shift and a lower drain current (at $V_{gs} = 0$ V) were obtained as $V_{ds,stress}$ was strengthened. Fig. 7(b) illustrated ΔV_{th} and current ratio as a function of $V_{ds,stress}$. Compared with the results in the case of $V_{ds,stress} = 0$ V, a drain stressing voltage

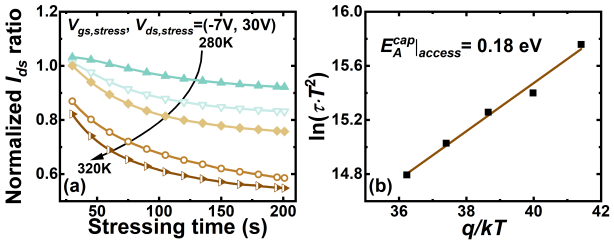

Fig. 8. (a) Normalized DCT spectroscopy with stressing process [$V_{gs,stress}$, $V_{ds,stress}$ = (−7 V, 30 V)] from 280 to 320 K. (b) Extracted activation energy in the access region of the device.

of 10 V for 100 s resulted in a V_{th} shift to the value of −0.26 V. The amount of V_{th} shift was further enlarged as biasing a higher $V_{ds,stress}$. When $V_{ds,stress}$ was enhanced to 50 V, ΔV_{th} was extracted to −0.45 V for 100 s. Additionally, the decrease of drain current extracted at V_{gs} = 0 V and V_{ds} = 1 V was summarized. The current degradation ratio was defined to $(1 - I_{ds}/I_{ds,fresh})$ at V_{gs} = 0 V, where $I_{ds,fresh}$ represents the drain current measured in the absence of stress. When the device was exposed to a $V_{ds,stress}$ of 50 V for 100 s, a current degradation ratio of 25% was observed.

The observed negative V_{th} shift was attributed to the emission of electrons from traps in the gate area, with an extracted $E_A^{emi}|_{dielectric}$ of 0.28 eV. When a drain voltage stress was applied, the release of electrons from traps was accelerated. ΔV_{th} was enhanced as the drain voltage increases [Fig. 7(b)]. In addition, a reduction in drain current was observed when the device was exposed to a large $V_{ds,stress}$ voltage [Fig. 7(a)]. This decrease in current was due to the capture of electrons by traps in the access region.

Temperature-related DCT spectroscopy was employed to explore trap properties related to the decreased I_{ds}. Fig. 8(a) displayed the normalized I_{ds} as a function of stressing time with different temperatures. The device was biased at the stressing condition of ($V_{gs,stress}$, $V_{ds,stress}$) = (−7 V, 30 V) for an extended period of 200 s and a relatively short sampling time of 3 ms was selected. When the device was switched to ON-state, I_{ds} was measured in the saturation region of output curves (V_{gs} = −1 V and V_{ds} = 5 V). The normalized I_{ds} was defined as ($I_{ds,dynamic}/I_{ds,static}$), where $I_{ds,static}$ was measured in the nonstressed fresh state [($V_{gs,stress}$, $V_{ds,stress}$) = (0 V, 0 V)]. With extending the stressing time, the normalized I_{ds} decreased due to the electrons was captured by trap states in the access region. The decrease of I_{ds} was thermally accelerated, and electrons were more likely to be injected into access region at a relatively higher temperature. Fig. 8(b) showed an Arrhenius plot of time constants during stressing process, and a capture activation energy $E_A^{cap}|_{access}$ of 0.18 eV for trap states related to the access region was extracted. This energy was in consistence with previously reported activation energy of SiN_x thin films [30], [31].

Fig. 9(a) showed the dynamic R_{ON} ratio with OFF-state drain stressing bias ranging from 10 to 50 V. The dynamic R_{ON} ratio was defined as ($R_{ON,d}/R_{ON,s}$), where $R_{ON,s}$ was measured in the nonstressed fresh state [($V_{gs,stress}$, $V_{ds,stress}$) = (0 V, 0 V)]. R_{ON} was extracted in the linear region of output curve, and the measurement voltage of the device was V_{gs} = −0.5 V and V_{ds} = 1 V. When merely an OFF-state stressing bias of −7 V was applied to the device, R_{ON} remained almost unchanged, indicating gate stressing voltage only would not affect R_{ON}. In the case of ($V_{gs,stress}$, $V_{ds,stress}$) = (−7 V, 10 V), the dynamic R_{ON} remained as low as 1.09 for a stressing time

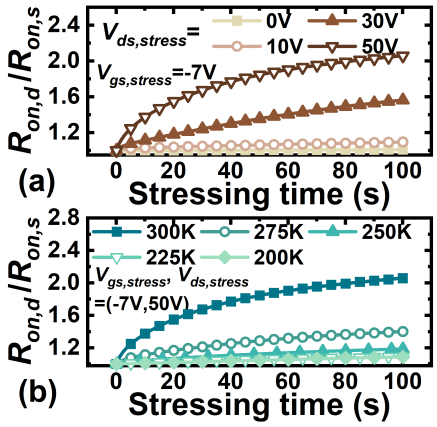

Fig. 9. (a) Variation of R_{ON} as a function of stressing time with various $V_{ds,stress}$ values. (b) Variation of R_{ON} with different temperatures at ($V_{gs,stress}$, $V_{ds,stress}$) = (−7 V, 50 V).

of 100 s. When the drain stressing voltage was increased to 30 V, a significant increase in R_{ON} was observed. The dynamic R_{ON} ratio deteriorated to 2.05 with a larger $V_{ds,stress}$ of 50 V for 100 s. In recent literatures, dynamic R_{ON} ratio of a recessed MISHEMT was increased to 1.6 at $V_{ds,stress}$ = 10 V for 60 s [32]. A MOSHEMT with a 4-nm-thick ZrO_2 dielectric layer exhibited a normalized dynamic R_{ON} of 5 for a $V_{ds,stress}$ = 50 V and duty cycle of 10% [33]. A recessed MISHEMT with a relatively thick LPCVD Si_3N_4 mask effectively suppressed dynamic R_{ON} to 1.2 ($V_{ds,stress}$ = 60 V) [13]. In this work, a low dynamic R_{ON} ratio of 2.05 has been observed when the device was exposed to a relatively large OFF-state drain stressing ($V_{ds,stress}$ = 50 V) and a long stressing time (100 s). The results demonstrated that thin and high-quality in-situ SiN_x layers represent a promising solution to achieve a low dynamic R_{ON} ratio.

Fig. 9(b) showed the dynamic R_{ON} as a function of stressing time with different temperatures. At 275 K, the degradation of the dynamic R_{ON} ratio was restrained to 1.39. The dynamic R_{ON} ratio further decreased as the device temperature was lowered. When the temperature was decreased to 225 K, the R_{ON} ratio reached 1.1 for a stressing time of 100 s. The variation of R_{ON} was related to the capture of electrons in the access region (in-situ SiN_x) of the device. The decrease of temperature inhibited the capture capability of traps and suppressed the increase of dynamic R_{ON}. The capture of electrons was accelerated with a higher temperature and a larger $V_{gs,stress}$, and thus, an increase in R_{ON} would be observed. This phenomenon was consistent with capture process revealed in GaN MISHEMT with an in-situ SiN_x dielectric layer [7].

IV. Conclusion

In conclusion, the OFF-state stress-induced threshold voltage instability and dynamic R_{ON} of GaN MOS-HEMTs with ZrO_2 gate dielectric were investigated. The negative V_{th} shift during NBTI experiments was recorded and was attributed to electron emission in the gate area. The threshold voltage was shifted by −0.31 V when an OFF-state stressing ($|V_{gs,stress} - V_{th}|$) of 14 V was applied for 100 s. Temperature-dependent threshold voltage transient spectroscopy revealed an emission activation energy $E_A^{emi}|_{dielectric}$ of 0.28 eV and a capture activation energy $E_A^{cap}|_{dielectric}$ of 0.30 eV related to threshold voltage shift. The V_{th} shift during PBTI experiments was also discussed. A much larger positive shift in V_{th} was observed when the device was

biased to overdrive voltage. In addition to the shift of threshold voltage, the decrease of drain current was found when the device was exposed to an OFF-state drain stressing. This degradation in drain current was attributed to electron trapping at the access region, which contributed to the increase of R_{ON}. The time-resolved R_{ON} displayed the R_{ON} increased with stressing time under higher drain stressing condition. DCT measurement also revealed an activation energy $E_A^{cap}|_{access}$ of 0.18 eV in connection with the R_{ON} degradation. These results indicate that GaN MOSHEMT with ZrO_2 gate dielectric is a promising technology for high-power switching applications.

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