Enhancing ON- and OFF-State Performance of Quasi-Vertical GaN Trench MOSFETs on Sapphire With Reduced Interface Charges and a Thick Bottom Dielectric

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***Abstract*— In this letter, we report the enhancement of ON- and OFF-state performance in vertical GaN trench MOSFETs through fabrication process optimization. The ON-state device performance was effectively improved by reducing MOS channel interface charges with a piranha cleaning process prior to the gate dielectric deposition. For the OFF-state, the breakdown voltage (V_{BR}) of the device was greatly enhanced via suppressing the electric field in the gate dielectric near the bottom of the gate trench with a thick bottom dielectric process. As a result, high-performance quasi-vertical GaN trench MOSFETs grown on sapphire substrates with a 4-μm-thick drift layer are demonstrated, exhibiting a low specific ON-resistance of 0.95 m$\Omega\cdot$cm^2, a high maximum drain current of 3.4 kA/cm^2, a large threshold voltage of 6.1 V (defined at I_D of 1 A/cm^2), and a high V_{BR} of 485 V.**

***Index Terms*— Gallium nitride, vertical trench MOSFET, interface charge, thick bottom dielectric, breakdown voltage.**

I. Introduction

VERTICAL GaN-based transistors have shown enormous potential for efficient power switching applications due to their high voltage and high current handling capability. Progress has been made on developing vertical GaN transistors, including vertical GaN trench MOSFETs [1]–[7], the current aperture vertical electron transistors (CAVETs) [7]–[12] and vertical GaN fin MOSFETs [13]–[15]. Considering the high threshold voltage (V_{th}) above 3 V preventing false turn-on and simple fabrication process (without regrowth step), vertical GaN trench MOSFET is a competitive candidate suitable for volume manufacturing. Lowering the channel resistance-dependent R_{ON} is key to minimize the power loss. The existence of high-density positive channel interface charges [1]–[7] can lead to a reduced V_{th} [4] and poor channel mobility [16], [17]. Therefore, a proper cleaning process is necessary to improve channel property for better ON-state behavior. Piranha cleaning was found effective to improve the dielectric/GaN interface in planar GaN MOS capacitors on c-plane GaN surface [18], [19]. For the OFF-state performance, the reported device breakdown voltage (V_{BR}) is far below the theoretical value of the non-punch-through GaN p-n junctions, which is mainly caused by the immature gate-to-drain breakdown due to the high peak electric field crowding at the trench bottom corner [1]–[4], [6], [7], [20], [21]. As such, suppressing the electric field at the gate trench corner is vital to enhance the device breakdown voltage. One effective solution was introducing a thick SiO_2 layer in the gate trench as the field oxide, as demonstrated in vertical GaN fin MOSFETs [13]–[15], similar to the thick bottom dielectric (TBD) reported in Si [22], [23] and SiC [24], [25] vertical MOSFETs. Effects of the TBD on the ON- and OFF-state performance in *inversion-channel* GaN trench MOSFETs have not been investigated.

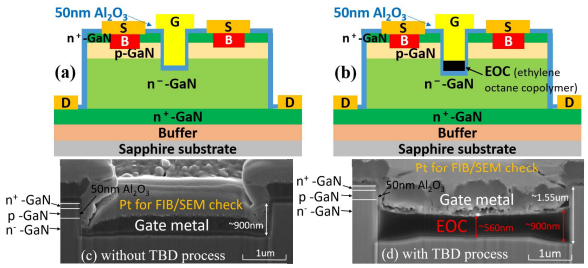

Fig. 1. Cross-sectional schematics of fabricated quasi-vertical GaN trench MOSFETs (a) without a thick bottom dielectric (TBD) process and (b) with a TBD process. "S", "D", "G", and "B" refers to "Source", "Drain", "Gate", and "Body", respectively. Cross-sectional SEM images of the gate trench region of devices (c) without TBD and (d) with TBD.

In this work, we report significant enhancement of ON- and OFF-state performance of vertical GaN trench MOSFETs with reduced interface charges and a thick bottom dielectric. The demonstrated quasi-vertical GaN trench MOSFETs exhibit not only a large V_{th} of 6.1 V, but also a low specific ON-resistance ($R_{ON,sp}$) of 0.95 m$\Omega\cdot$cm^2 and a high maximum drain current ($I_{D,max}$) of 3.4 kA/cm^2, and a V_{BR} of 485 V.

II. Device Design and Fabrication

The n^+-p-n^--n^+-GaN structures for the quasi-vertical trench MOSFETs were grown on sapphire substrates by Metal Organic Chemical Vapor Deposition (MOCVD) (Fig. 1).

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The epilayers, from bottom to top, consist of a 1-μm i-GaN buffer, a 1-μm n^+-GaN [Si: 5×10^{18} cm^{-3}], a 4-μm n^--GaN drift layer [Si: 3×10^{16} cm^{-3}], a 400-nm p-GaN body [Mg: 1.2×10^{19} cm^{-3}], and a 200-nm n^+-GaN layer [Si: 5×10^{18} cm^{-3}].

The vertical MOSFETs without TBD shared the same fabrication process as the work we have reported [4], except that two different channel cleaning processes were adopted before the gate dielectric (50-nm Al_2O_3) deposition: (I) buffered oxide etchant (BOE) for 2 min only; (II) piranha (H_2SO_4:H_2O_2 =10:1, at 120°C) for 10 min + BOE for 2 min. For the fabrication process of devices with TBD, compared with the ones without TBD: (1) a deeper trench of ~1.5 μm (~900 nm for device without TBD) was etched; (2) before gate metal deposition, a layer of ethylene octene copolymer (EOC, from *Everlight Chemical*, with a dielectric constant of 3.6, a breakdown field of 4.1 MV/cm, and a glass transition temperature of 230°C) was blanketly coated to fill the gate trench, cured at 150°C for 30 min on a hotplate and etched back by O_2 plasma, leaving around 500~600 nm EOC only in the gate trench to form the thick bottom dielectric. The cross-sectional schematic of the vertical MOSFETs without and with the TBD is shown in Fig. 1(a) and (b), respectively. After device fabrication, the corresponding gate stack of the device was characterized using scanning electron microscopy (SEM) as shown in Fig. 1(c) and (d). It can be observed that both devices exhibit near 90-degree vertical sidewalls of the gate trench, which has been reported vital for the carrier transport [6]. Moreover, for the device with TBD (Fig. 1(d)), the EOC near the gate trench sidewall was found thicker than that in the center region, which is in favor of reducing the electric field strength at the trench bottom corners.

The devices reported here feature a rectangular gate trench with a 4 μm × 100 μm area. The gate trench sidewalls were aligned to *m*-plane for better ON-state performance [6], [26]. The active area of the device for specific ON-resistance and current density normalization is regarded as (4 μm trench length + 4 μm drift region thickness) × (100 μm trench width + 4 μm drift region thickness) = 832 μm^2, taking the lateral current spreading length (4 μm) in the drift region into account [4], [6]–[8]. The total device area is 200 μm × 300 μm, including the gate, source and drain contact pads.

III. Device Results and Discussion

The device without additional piranha cleaning (without TBD) presents an ON/OFF current ratio (I_{ON}/I_{OFF}) of ~1×10^9, a gate current (I_G) of 5.7×10^{-4} A/cm^2 (at V_{GS} of 15 V), a V_{th} of 4.8 V (at I_D of 1 A/cm^2), a V_{th} hysteresis (from I_D-V_{GS} double sweep) of 1.3 V, a subthreshold slope (*SS*) of 281 mV/dec. In addition, a $I_{D,max}$ of 2.61 kA/cm^2 and a $R_{ON,sp}$ of 1.03 mΩ·cm^2 are also demonstrated at V_{GS} of 15 V (Fig. 2(a) and (b)). The device made from the same epi with additional piranha cleaning (without TBD) shows a similar I_{ON}/I_{OFF} of ~1×10^9, a similar I_G of 5.6×10^{-4} A/cm^2 (at V_{GS} of 15 V), an increased V_{th} of 6.2 V (at I_D of 1 A/cm^2), a reduced V_{th} hysteresis of 0.8 V, a smaller *SS* of 228 mV/dec, a remarkably enhanced $I_{D,max}$ of 3.56 kA/cm^2 and a reduced $R_{ON,sp}$ of 0.85 m$\Omega \cdot$ cm^2, as shown in Fig. 2 (c) and (d).

The increase of V_{th} (from 4.8 V to 6.2 V) indicates a reduction of fixed interface charges, from ~3.7×10^{12} cm^{-2} to ~2.5×10^{12} cm^{-2} with the employment of additional piranha cleaning, based on the extracted effective acceptor concentration (N_A) of ~1.6×10^{18} cm^{-3} in the p-GaN layer for both devices [4]. The reduced *SS* (281 mV/dec to 228 mV/dec) and V_{th} hysteresis (ΔV_{th}, 1.3 V to 0.8 V) indicate the decreased interface trap states density. The calculated interface trap density ($N_{it} = \Delta V_{th} \times C_{ox}/q$) based on the measured ΔV_{th} with and without piranha cleaning are 6.2×10^{11} cm^{-2} and 1.0×10^{12} cm^{-2}. In Fig. 2 (b) and (d), the device with additional piranha cleaning shows a reduced DC and gate pulsed *I-V* dispersion, also suggesting a reduced interface trap density. The extracted electron mobility of the inversion channel [4] (considering the drift layer resistance of ~0.33 m$\Omega \cdot$ cm^2 and contact resistance of ~0.15 m$\Omega \cdot$ cm^2) is found enhanced from ~30 cm^2/V-s to ~57 cm^2/V-s, which can be attributed to the reduced interface (fixed and/or trapped) charges [16], [17]. The ON-state performance of GaN vertical MOSFETs can be effectively improved by reducing interface charges in the gate stack, through the additional piranha cleaning process [18], [19].

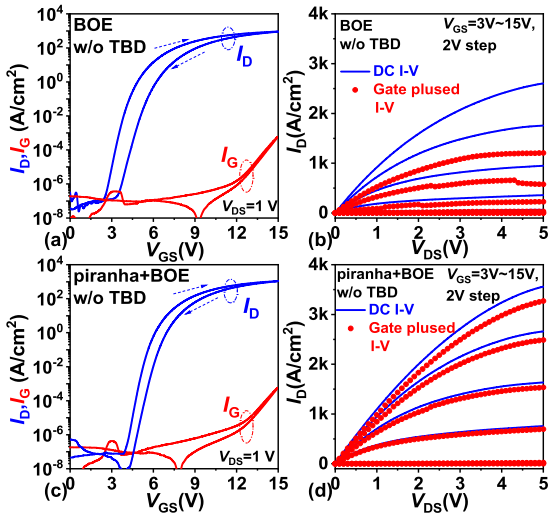

Fig. 2. (a) Transfer and (b) output (DC & pulsed I-V) characteristics of vertical MOSFET (without TBD) without additional piranha cleaning; (c) transfer and (d) output (DC & pulsed I-V) characteristics of vertical MOSFET (without TBD) with additional piranha cleaning. For gate pulsed *I-V* measurement in both (b) and (d), quiescent gate bias is −20 V, the pulse width is 500 μs, and the pulse period is 1 s.

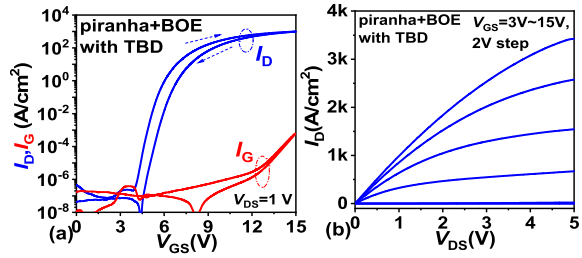

Fig. 3. (a) Transfer and (b) output (DC) characteristics of a vertical MOSFET with TBD process (with additional piranha cleaning).

The transfer and output characteristics of the device using the same fabrication process with the added TBD are shown in Fig. 3, which exhibits a similar I_{ON}/I_{OFF} of ~1×10^9, a I_G of 5.9×10^{-4} A/cm^2 (at V_{GS} of 15 V), a V_{th} of 6.1 V (at I_D of 1 A/cm^2), a V_{th} hysteresis of 0.8 V, a *SS* of 230 mV/dec, a $I_{D,max}$ of 3.42 kA/cm^2, and a $R_{ON,sp}$ of 0.95 m$\Omega \cdot$ cm^2. It should be noted that although most of the ON-state parameters including the I_{ON}/I_{OFF}, I_G (at V_{GS} of 15 V), V_{th}, V_{th} hysteresis, and *SS* are nearly identical in devices with and without TBD, the $R_{ON,sp}$ in the device with TBD is somewhat (~12%) higher (thereby slightly lower $I_{D,max}$) than the one without TBD, which possibly results from the relatively higher accumulation resistance in the trench region underneath the

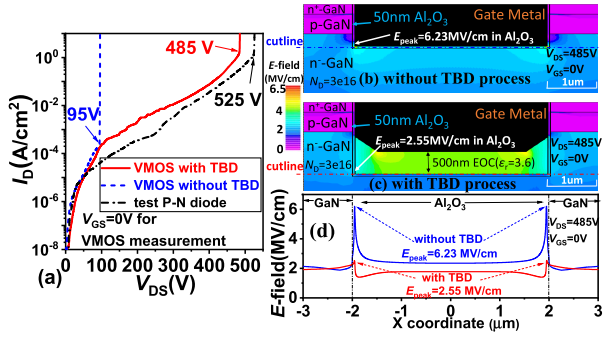

Fig. 4. (a) OFF-state leakage of vertical MOSFETs (with additional piranha cleaning) with & without TBD process and test p-n diode. TCAD simulation results of electric field distribution of VMOSFETs at V_{DS} = 485 V, V_{GS} = 0 V (b) without and (c) with a thick bottom dielectric (TBD); (d) electric field distribution along the cutlines at the gate trench bottom.

channel due to a lower carrier concentration in the sidewall and bottom accumulation layer covered by the EOC [22], [23].

Fig. 4(a) compares the OFF-state leakage currents in the vertical MOSFETs (with additional piranha cleaning) with and without the TBD and a p-n$^-$ diode test structure on the same sample. The device without TBD shows a small V_{BR} of 95 V due to early dielectric failure at the gate-to-drain MOS junction. The possible reason for the low breakdown voltage could be due to the non-smooth trench bottom surface and damages resulted from the ICP etching for trench formation and/or yet-to-be improved Al_2O_3 quality. In contrast, the V_{BR} of the device with TBD is greatly enhanced by more than five folds to 485 V, which is close to the V_{BR} (~525 V) of the p-n diode test structure on the same sample, suggesting an effectively reduced peak electric field in the dielectric. Devices under two cleaning processes (with and without additional piranha cleaning) but without TBD show nearly identical OFF-state performance.

Fig. 4(b), (c) and (d) present the TCAD simulation results of the electric field distribution in gate trench region of vertical MOSFETs without and with the TBD process biased at a V_{DS} of 485 V and V_{GS} of 0 V. It is found that the peak electric field (E_{peak}) in the Al_2O_3 at the trench bottom corner is suppressed from 6.23 to 2.55 MV/cm using the TBD process, as shown in Fig. 4(d), suggesting the effectiveness of the TBD for electric field management. Fig. 5 (a) shows TCAD simulation results of E_{peak} versus V_{DS} of devices with varied TBD thickness. Devices with thicker TBD show a reduced E_{peak}, resulting in the enhanced V_{BR}. Fig. 5(b) illustrates the simulation results of $R_{ON,sp}$, V_{BR}, and Baliga's figure of merit (BFOM = $(V_{BR})^2/R_{ON,sp}$) versus the TBD thickness, showing a trade-off between $R_{ON,sp}$ and V_{BR} (thicker TBD results in enhanced V_{BR} with a cost of higher $R_{ON,sp}$). Introducing thicker TBD can effectively increase the BFOM. However, with the continuous increase of TBD thickness, the enhancement of BFOM tends to saturate.

TABLE I summarizes the key device parameters of samples with different fabrication processes. A proper channel cleaning process can effectively improve the ON-state performance and the TBD process can greatly enhance the OFF-state V_{BR} with minimal sacrifice in $R_{ON,sp}$ and $I_{D,max}$. Fig. 6 benchmarks the $R_{ON,sp}$ versus V_{BR} of the quasi-vertical GaN trench MOSFETs under piranha + BOE treatment with TBD in this work with other reported state-of-the-art GaN vertical transistors on bulk GaN substrates and foreign substrates. Our vertical MOSFETs grown on sapphire substrates show a good BFOM

TABLE I
SUMMARY OF KEY DEVICE PARAMETERS OF SAMPLES WITH DIFFERENT FABRICATION PROCESSES

Sample	#1	#2	#3
channel cleaning	BOE	piranha+BOE	piranha+BOE
TBD process	without	without	with
V_{th} (V) @1 A/cm^2	4.8	6.2	6.1
$I_{D,max}$ (A/cm^2)	2609	3564	3421
$R_{ON,sp}$ (mΩ·cm^2)	1.03	0.85	0.95
Peak trans-conductance(g_m) (S/cm^2) @V_{DS}=5V	420	587	538
V_{th} hysteresis (V)	1.3	0.8	0.8
SS (mV/dec)	281	228	230
V_{BR} (V)	93	95	485
BFOM (MW/cm^2)	8.4	10.6	248

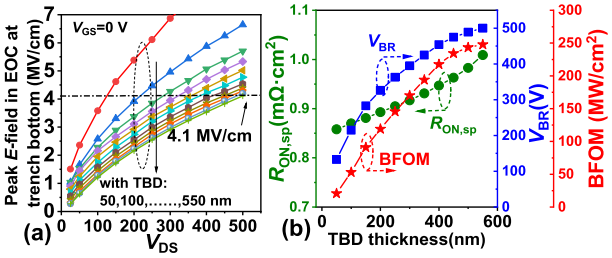

Fig. 5. TCAD simulation results of (a) E_{peak} versus V_{DS} of devices with varied TBD thickness and (b) $R_{ON,sp}$, V_{BR}, and BFOM versus TBD thickness. V_{BR} is defined by the biased V_{DS} when the E_{peak} in EOC at the trench bottom reaches 4.1 MV/cm (breakdown field of EOC).

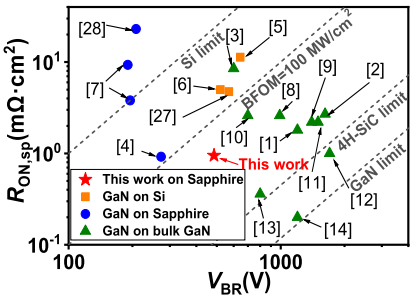

Fig. 6. $R_{ON,sp}$ versus V_{BR} benchmarking of the device with TBD in this work against reported state-of-the-art vertical GaN transistors.

of 248 MW/cm^2, which is superior to most of the reported vertical transistors on foreign substrates [4]–[7], [27], [28]. The V_{BR} of our vertical MOSFETs with TBD can be further improved by (1) optimizing gate trench formation process to achieve a smoother gate trench surface; (2) lowering the Si doping concentration and/or increasing the thickness of the drift layer; (3) introducing proper field plates near the mesa sidewalls [1], [9], [29], [30]. The $R_{ON,sp}$ can be further reduced by increasing the doping and thickness of the bottom n$^+$-GaN layer [31], [32].

IV. CONCLUSION

In summary, the ON-state performance of GaN vertical trench MOSFETs was effectively improved by reducing interface charges in the gate stack through a proper MOS channel cleaning process (piranha + BOE). In addition, a thick bottom dielectric process has been demonstrated, resulting in a greatly enhanced device OFF-state breakdown voltage with minimal sacrifice in $R_{ON,sp}$ and $I_{D,max}$. Overall high-performance quasi-vertical GaN trench MOSFETs on sapphire are achieved, exhibiting an ultralow $R_{ON,sp}$ of 0.95 mΩ · cm^2, a high $I_{D,max}$ of 3.4 kA/cm^2, a large V_{th} of 6.1 V, and a high V_{BR} of 485 V.

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