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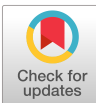

GaN quasi-vertical trench MOSFETs grown on Si substrate with ON-current exceeding 1 A

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This work reports GaN quasi-vertical trench MOSFETs grown on 6-inch Si substrates. The device with single-trench design shows a specific ON-resistance of 0.84 mΩ·cm^2, a maximum drain current density of 5.0 kA cm^{-2}, and a breakdown voltage of 320 V, after fine-tuning of the channel doping and employment of a thick bottom dielectric process. The large-area (~0.54 mm^2) GaN-on-Si trench MOSFET with multiple-finger design shows an ON-current of 1.1 A, an ON-resistance of 4.0 Ω and a breakdown voltage of 205 V. © 2022 The Japan Society of Applied Physics

Vertical GaN transistors are attracting extensive attention in high voltage [with breakdown voltage (V_{BR}) > 1 kV] applications.[1] Because of the vertical topology, a higher V_{BR} can be effectuated by introducing a thicker drift layer without increasing the device area.[1] In the past decade, high-performance GaN vertical transistors, including current aperture vertical electron transistors,[2–7] fin power FETs,[8–10] and trench MOSFETs [11–19] have been demonstrated. Compared with other types of vertical transistors, GaN trench MOSFETs have the advantages of a simpler fabrication process and larger V_{th}.[1] High-performance GaN trench MOSFETs with V_{BR} over 1 kV have been successfully demonstrated based on bulk GaN substrates.[11,12] However, the high cost and limited size of low-defect-density GaN substrates have limited the scaling of volume production. As a more cost-effective platform, GaN-on-Si has been explored for GaN vertical devices. Recently, quasi- and fully-vertical GaN trench MOSFETs with large V_{th} have been reported on Si substrates.[14–17] The reported GaN-on-Si trench MOSFETs showed relevantly high specific ON-resistance ($R_{ON,sp} > 4$ mΩ·cm^2).[14–17] In addition, the demonstrated devices employing single-trench design provided a limited maximum ON-current (<10 mA).[14–17]

In this letter, we report GaN-based quasi-vertical trench gate MOSFETs on cost-effective Si substrate with ON-current exceeding 1 A. The best device with single-trench design shows a low $R_{ON,sp}$ of 0.84 mΩ·cm^2, a high maximum drain current density ($I_{D,max}$) of 5.0 kA cm^{-2}, a high V_{th} of 5.3 V (at $I_D = 1$ A cm^{-2}) and a V_{BR} of 320 V, after fine-tuning of the channel doping and adoption of a thick bottom dielectric process. The fabricated large-area (~0.54 mm^2) device with a multiple-finger design presents a maximum drain current of 1.1 A, an ON-resistance of 4.0 Ω, a high V_{th} of 6.5 V (from linear extrapolation), and a V_{BR} of 205 V.

The epitaxial layers for device fabrication were grown on 6-inch Si substrates by metal-organic chemical vapor deposition (MOCVD), from bottom to top, consisting of a 1.3 μm AlN/AlGaN based buffer layer, a 1 μm n$^+$-GaN [Si: 5×10^{18} cm^{-3}], a 2 μm n$^-$-GaN [Si: 2×10^{16} cm^{-3}] drift layer, a 400 nm p-GaN layer (Mg-doped), and a 200 nm n$^+$-GaN [Si: 5×10^{18} cm^{-3}] layer, as presented in Fig. 1(a). Sample A, B, and C have the same epi structures except for the p-GaN channel doping (p-GaN channel doping: sample A > sample B > sample C). The estimated threading dislocation densities (TDD) are 4.12×, 5.76×, and 5.21 × 10^8 cm^{-2} for samples A, B, and C, respectively. The values were calculated using empirical equations[20] with measured FWHM values of the X-ray omega rocking curves for (002) and (102) planes from X-ray diffraction (XRD) measurements. The same device fabrication process was applied for all the samples [Fig. 1(b)]. The device fabrication started with Cl_2/BCl_3-based dry-etching of the gate trench, followed by mesa and p-GaN body contact etching. Subsequently, an 800 °C rapid thermal annealing (RTA) was carried out in a nitrogen ambient for p-GaN activation. A 50 nm Al_2O_3 gate dielectric was deposited by atomic layer deposition (ALD). Samples were cleaned by piranha and buffered oxide etchant (BOE) before the gate dielectric deposition to improve the Al_2O_3/GaN interface.[19,21] Metal contacts of the body (Ni/Au metal stacks) and source/drain (Ti/Al/Ni/Au metal stacks) were evaporated and defined. Subsequently, ethylene octene copolymer (EOC) was used to fill the gate trench and etched back before the gate metal deposition, forming the thick bottom dielectric (TBD) for enhanced breakdown voltage.[19] The process ended with the gate metal (Ti/Al) deposition. To achieve a superior device ON-state performance, the trench sidewalls of all samples were aligned to the *m*-plane.[16,22] Figure 1(c) shows a cross-sectional scanning electron microscopy (SEM) image of the gate region. The thicker EOC near the trench sidewall is beneficial to relax the electric field crowding at the trench corners.[19]

Channel doping level tuning and device design optimization (introducing the thick bottom dielectric) were performed on a single-trench device with a rectangular trench area of 4 μm × 100 μm [Fig. 1(b)]. The active area used for device key metrics normalization is (4 μm + 2 μm) × (100 μm + 2 μm) = 612 μm^2, taking the gate trench area and the 45-degree lateral current spreading in the drift layer into consideration.[2,3,14–17] The total device area is 0.06 mm^2, including all the contact pads. Figure 2 illustrates the representative transfer, output, and OFF-state I–V curves of a single-trench device on sample C (with the lowest channel doping among the three samples) with TBD, which shows the lowest $R_{ON,sp}$, the highest $I_{D,max}$, and a large V_{th}. As shown in Fig. 2(a), the device presents a positive V_{th} of 5.3 V (at $I_D =$ 1 A cm^{-2}) and a V_{th} hysteresis of 0.5 V. The gate leakage is 6.9×10^{-4} A cm^{-2} at $V_{GS} = 15$ V. In addition, a high $I_{D,max}$ (at $V_{GS} = 15$ V and $V_{DS} = 10$ V) of 5.0 kA cm^{-2} and a low $R_{ON,sp}$ (at $V_{GS} = 15$ V and $V_{DS} = 1$ V) of 0.84 mΩ·cm^2

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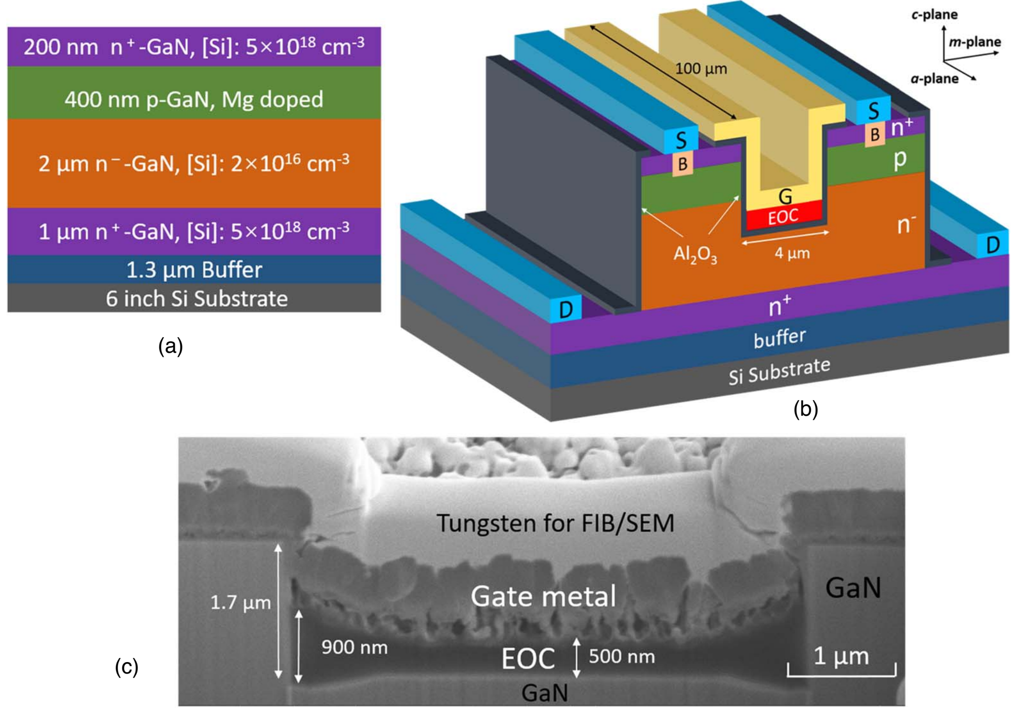

Fig. 1. (Color online) (a) Epilayers for device fabrication. (b) Device schematic presentation of GaN trench MOSFETs with single-trench design. (c) Cross-sectional SEM image of the device gate area.

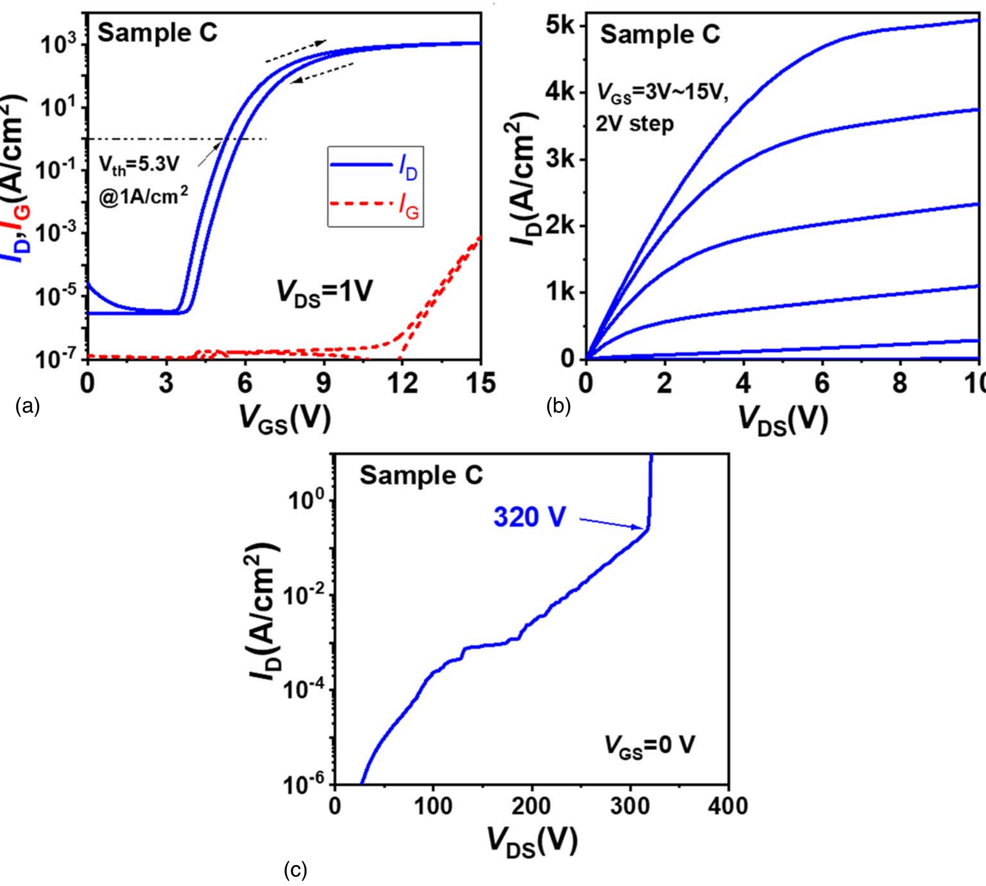

Fig. 2. (Color online) (a) Transfer, (b) output, and (c) OFF-state *I–V* curves of a single-trench device on sample C.

(82.3 mΩ·cm^2 when using total device area including pad area for $R_{ON,sp}$ normalization) are also demonstrated [Fig. 2(b)]. The V_{BR} (hard breakdown) is 320 V (measured at $V_{GS} = 0$ V), as shown in Fig. 2(c).

The good ON-state performance of sample C results from the fine-tuning of channel doping. Figure 3 presents a comparison of the representative transfer, output, transconductance (g_m), and OFF-state characteristics of the

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single-trench devices (all with TBD) from samples A, B, and C with varied channel doping (sample A > sample B > sample C). From samples A, B to C, the V_{th} (at $I_D = 1$ A cm^{-2}) decreases from 6.8 V, 6.1 V to 5.3 V. From the test structures with separated body and source contacts, the extracted effective acceptor concentration (N_A) of the p-GaN channel are 2.8×, 2.2×, and 1.3 × 10^{18} cm^{-3} for samples A, B and C, on the basis of the body bias effect.[18,23) On the other hand, from samples A, B, to C, the $R_{ON,sp}$ (at $V_{GS} = 15$ V and $V_{DS} = 1$ V) decreases from 1.53 mΩ·cm^2, 1.21 mΩ·cm^2 to 0.84 mΩ·cm^2 (149 mΩ·cm^2, 118 mΩ·cm^2 to 82.3 mΩ·cm^2 when using total device area for $R_{ON,sp}$ normalization), corresponding to a dramatic increase of the $I_{D,max}$ (at $V_{GS} = 15$ V and $V_{DS} = 10$ V) from 1.9 kA cm^{-2}, 2.9 kA cm^{-2} to 5.0 kA cm^{-2}, respectively [Fig. 3(b)]. The extracted channel mobility[18,24) (considering the drift layer resistance of ~0.18 mΩ·cm^2 and contact resistance of ~0.21 mΩ·cm^2) is found to increase from 15.1 cm^2 V^{-1} s^{-1}, 20.3 cm^2 V^{-1} s^{-1} to 28.9 cm^2 V^{-1} s^{-1} from sample A, B, to C, which could be explained by the reduced impurity scattering with lower channel doping.[18,25) From samples A, B, to C, the peak g_m ($V_{DS} = 10$ V) increases from 395 S cm^{-2}, 480 S cm^{-2}, to 735 S cm^{-2} [Fig.3 (c)], indicating the enhanced gate modulation with reduced channel doping. For the OFF-state performance [Fig. 3(d)], samples A, B, and C show similar V_{BR} (hard breakdown) of 325 V, 318 V and 320 V, respectively, measured at $V_{GS} = 0$ V. Benefiting from the lower channel doping, sample C shows a low $R_{ON,sp}$ of 0.84 mΩ·cm^2 and a high $I_{D,max}$ of 5.0 kA cm^{-2}, while maintaining a high V_{th} of 5.3 V, sufficient to avoid false turn-on.

Introducing the thick bottom dielectric (TBD) process can help to improve device OFF-state performance. The device schematics of trench MOSFETs with and without TBD are presented in Figs. 4(a) and 4(b). Figure 4(c) compares the OFF-state *I–V* curves of vertical MOSFETs with and without the TBD process and the trial p-n diode on sample C. After introducing the TBD process, the V_{BR} of trench MOSFETs is greatly increased from 90 V to 320 V (hard breakdown in gate region), close to the V_{BR} (~360 V, hard breakdown) of the test p-n diode on the same sample. From the TCAD simulation, the introduction of the TBD process can reduce the peak electric field of the Al_2O_3 gate dielectric at the gate trench corner region from 4.52 to 2.03 MV cm^{-1}, at $V_{DS} = 320$ V and $V_{GS} = 0$ V. The TCAD simulation results confirm the effectiveness of the TBD process in relaxing electric field strength in the trench corner region.[19,26) For the ON-state performance, the device on sample C without TBD presents a V_{th} (at $I_D = 1$ A cm^{-2}) of 5.2 V, a $R_{ON,sp}$ of 0.77 mΩ·cm^2 and a $I_{D,max}$ of 5.6 kA cm^{-2}. Introducing the TBD process can effectively enhance V_{BR} and keep nearly identical V_{th} with a slight sacrifice in $R_{ON,sp}$ (~9% higher) and $I_{D,max}$ (~11% lower).[19,26)

The top-view layout of the large-area trench MOSFET with multiple-finger design (4 μm × 500 μm for each gate trench; 20 trenches in total) is illustrated in Fig. 5(a). The cell pitch is 28 μm and the total device area is 720 μm × 750 μm = 0.54 mm^2, including all the contact pads. The

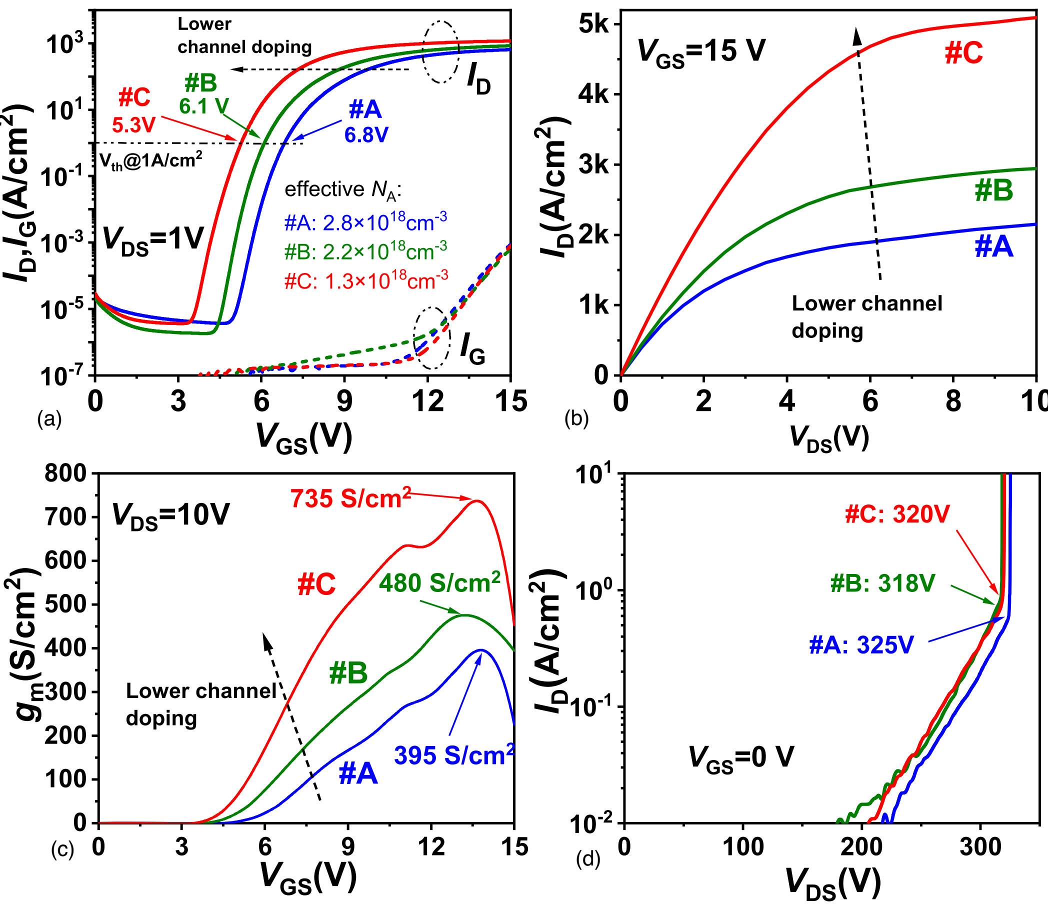

Fig. 3. (Color online) (a) Transfer, (b) output, (c) trans-conductance (g_m), and (d) OFF-state characteristics of single-trench devices on samples A, B, and C with varied channel doping.

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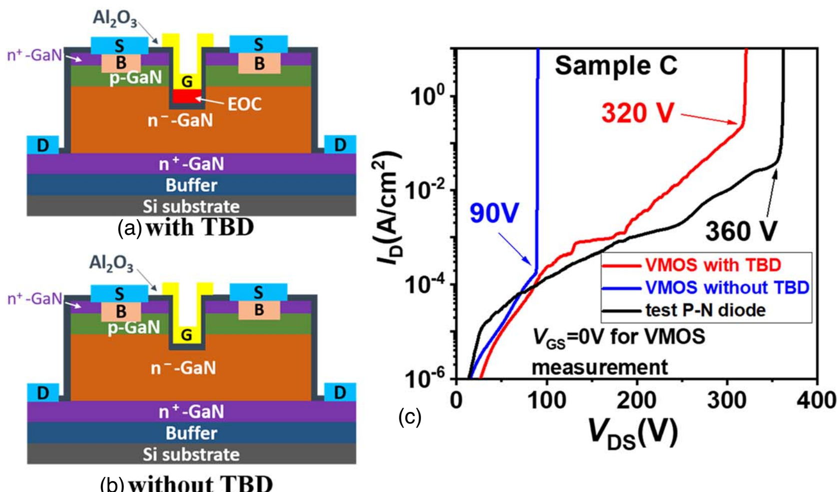

Fig. 4. (Color online) Device schematics of trench MOSFETs (a) with TBD and (b) without TBD. (c) OFF-state I–V curves of trench MOSFETs with and without TBD and the trial p-n diode on sample C.

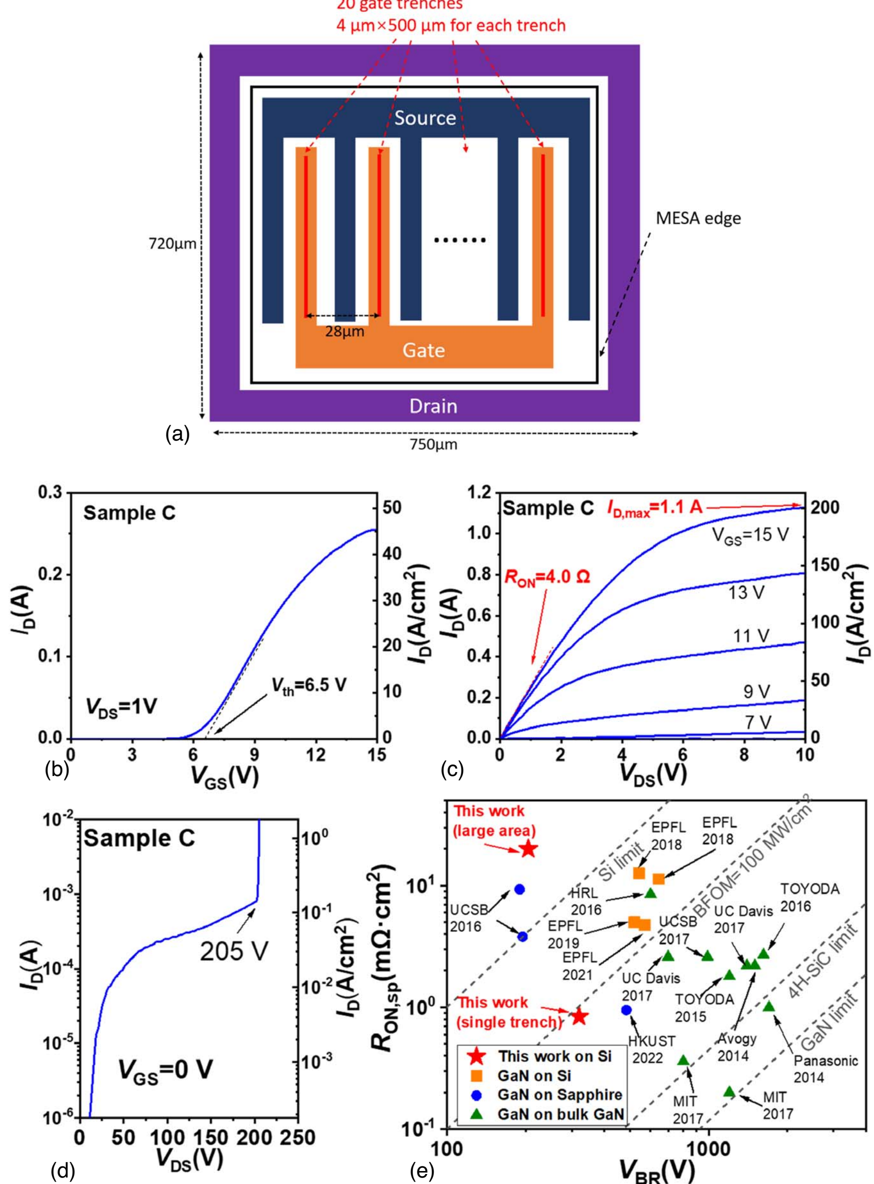

Fig. 5. (Color online) (a) Top-view layout of the large-area trench MOSFET with multiple-finger design. (b) Transfer, (c) output, and (d) OFF-state I–V curves of the large-area vertical MOSFET on sample C. (e) $R_{ON,sp}$ versus V_{BR} benchmarking of the GaN-on-Si trench MOSFETs in this work with other reported GaN vertical transistors.

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large-area device used the same fabrication procedure (with TBD) as the single-trench device described. Figures 5(b) and 5(c) show the transfer and output I–V curves of a large-area device on sample C with multiple-finger design, presenting a positive V_{th} of 6.5 V (extracted by linear extrapolation), a R_{ON} of 4.0 Ω ($V_{GS} = 15$ V) and a maximum I_{ON} of 1.1 A ($V_{GS} = 15$ V, $V_{DS} = 10$ V). To our best knowledge, this is the first demonstration of GaN vertical transistors grown on Si substrates with I_{ON} exceeding 1 A. Normalized to the total device area of 0.54 mm^2, the large-area device shows a $R_{ON,sp}$ of 21.6 mΩ·cm^2 and a $I_{D,max}$ of 0.2 kA cm^{-2}. Compared with the single-trench device (normalized by active area), the large-area device (normalized by total device area) presents a higher $R_{ON,sp}$ and a lower $I_{D,max}$, which can be attributed to: (1) the current crowding effect[27] in quasi-vertical device design; (2) yet-to-be-increased channel density (could be increased by employing hexagonal layout and decreasing the cell pitch).[11,12,28] Figure 5(d) presents the OFF-state performance of this large-area device, presenting a V_{BR} (hard breakdown) of 205 V. Compared with the single-trench device, the large-area device presents a lower V_{BR}, which can be explained by the increased number of dislocations (under the MOS area)[29] and the non-uniformity issue of the TBD and gate dielectric in the large-area device.

Figure 5(e) presents the $R_{ON,sp}$ versus V_{BR} benchmarking of the GaN-on-Si trench MOSFETs in this work with other reported GaN vertical transistors. Our GaN-on-Si trench MOSFETs employing single-trench design present a Baliga's figure of merit (BFOM = $(V_{BR})^2/R_{ON,p}$) of 122 MW cm^{-2}, which is higher than other reported GaN-on-Si vertical transistors (using the same active area definition method for a fair comparison).[14–17] For the large-area device, a lower $R_{ON,sp}$ and a higher $I_{D,max}$ can be effectuated by: (1) introducing a thicker bottom n^+-GaN layer with higher Si doping to reduce the influence of current crowding in the quasi-vertical design;[27] (2) using fully-vertical GaN-on-Si technique[17] to eliminate the current crowding; (3) employing hexagonal layout and decreasing the cell pitch to increase the channel density.[11,12,28] Lower leakage current and higher V_{BR} can be achieved by: (1) introducing a thicker drift layer with lower Si doping;[11–13] (2) optimizing the edge-terminal near the mesa region;[11,12,30] (3) optimizing gate trench etching, gate dielectric deposition and thick bottom dielectric processes to achieve a more stable gate MOS stack; (4) optimizing GaN-on-Si buffers to reduce the dislocation density.[31] Stable gate MOS stack for avoiding drain-to-gate hard breakdown, combined with high-quality epilayers with low dislocation density and advanced edge-termination techniques[32–34] are critical in achieving avalanche capability in GaN-on-Si vertical trench MOSFETs.

In summary, this letter reports the first demonstration of GaN-on-Si quasi-vertical trench MOSFETs with ON-current exceeding 1 A. Fine-tuning of the channel doping and employment of a TBD process led to the best device with a single-trench design showing a low $R_{ON,sp}$ of 0.84 mΩ·cm^2, a high $I_{D,max}$ of 5.0 kA cm^{-2}, a high V_{th} of 5.3 V (at $I_D = 1$ A cm^{-2}) and a V_{BR} of 320 V. The fabricated large-area (∼0.54 mm^2) device with multiple-finger design presents a maximum ON-current of 1.1 A, an ON-resistance of 4.0 Ω, a high V_{th} of 6.5 V (extracted by linear extrapolation), and a V_{BR} of 205 V. Those results support the potential of GaN vertical MOSFETs on Si for high-power applications.

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