Applied Physics Letters

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Cite as: Appl. Phys. Lett. **120**, 242104 (2022); https://doi.org/10.1063/5.0088251
Submitted: 15 February 2022 • Accepted: 03 June 2022 • Published Online: 14 June 2022

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Applied Physics Letters ARTICLE scitation.org/journal/apl

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Submitted: 15 February 2022 · Accepted: 3 June 2022 ·
Published Online: 14 June 2022

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Note: This paper is part of the APL Special Collection on Wide- and Ultrawide-Bandgap Electronic Semiconductor Devices.
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ABSTRACT

Vertical GaN trench MOSFETs have shown enormous potential for efficient power switching applications. Low ON-resistance (R_{ON}) to minimize power loss, high output current (I_{ON}) to maximize driving capability, and large threshold voltage (V_{th}) to avoid false turn-on are highly desirable. This work reports vertical GaN trench MOSFETs with step-graded channel doping. Conventional devices with uniform channel doping were involved for comparison. The experimental results show that step-graded channel doping can achieve an improved trade-off between I_{ON}, R_{ON}, and V_{th} than uniform channel doping.

GaN, a wide-bandgap semiconductor material widely used for LEDs, is expected to play an important role in the emerging field of power electronics.[1] AlGaN/GaN based lateral GaN power transistors have demonstrated great promise for low and medium voltage ($\leq$650 V) power switching applications over the past decade.[2–4] Commercial products of conventional normally-ON transistors are widely available. The much newer vertical GaN-based transistors have shown enormous potential for efficient power switching applications in recent years, due to their high voltage and high current handling capability.[1] To minimize power loss and maximize driving capability of the device, low ON-resistance (R_{ON}) in conjunction with high output current (I_{ON}) is always highly desired. At the same time, a large threshold voltage (V_{th}) is necessary to avoid false turn-on in switching applications.

Despite the remarkable progress made in vertical GaN trench MOSFETs,[5–11] the ON-state performance including the specific ON-resistance ($R_{ON,sp}$) and maximum drain current ($I_{D,max}$) is not on par with the current aperture vertical electron transistors (CAVETs)[11–16] and vertical fin MOSFETs[17–19] counterparts, mainly because of the large channel resistance of the inversion channel layer in trench MOSFETs. With shortcomings such as a complicated fabrication process (channel regrowth or precise dry etch required), the small V_{th} (typically ~1–2 V) of the CAVETs and vertical FinFETs may hinder their adoption for high-voltage switching applications. To take advantage of the simple device fabrication process and resulting large V_{th} of GaN trench MOSFETs, lowering the channel resistance-dominated R_{ON} is key to minimizing power loss. Even though the ON-state performance of vertical trench MOSFETs was improved by optimizing the gate trench formation process,[9,20–24] only a few studies report the impacts of material parameters, especially channel doping, on device performance. Strong impacts of the p-GaN doping level on balancing the device ON-state performance have been reported in vertical MOSFETs with the conventional uniform channel design.[7] The non-uniform (asymmetric) channel doping design, an effective way for improving device performance demonstrated in Si MOSFETs,[25,26] has never been reported in vertical GaN MOSFETs.

This work reports an investigation of the step-graded channel doping design in quasi-vertical GaN MOSFETs grown on sapphire substrates. From the experimental results, through tuning the thickness distribution of the high doping channel layer and low doping channel layer, trade-off among $I_{D,max}$, $R_{ON,sp}$, and V_{th} can be obtained. A thicker high doping channel can lead to an increased V_{th}, with a cost of an increased $R_{ON,sp}$ and a reduced $I_{D,max}$. Compared with the conventional design with uniform channel doping, the step-graded channel doping design offers an improved trade-off among $I_{D,max}$, $R_{ON,sp}$, and V_{th} in vertical GaN MOSFETs.

The n^+–p–n^-–n^+ epitaxial structures for the quasi-vertical GaN trench MOSFETs were grown on 2-in. sapphire substrates by metal

organic chemical vapor deposition (MOCVD) [Fig. 1(a)]. The epi-layers, from bottom to top, consist of a 1-μm i-GaN buffer layer, a 1-μm n^+-GaN (Si: 5×10^{18} cm^{-3}) layer, a 2.5-μm n^--GaN drift layer (Si: 5×10^{16} cm^{-3}), a 400-nm p-type GaN body layer (Mg-doped), and a 200-nm n^+-GaN layer (Si: 5×10^{18} cm^{-3}). Seven samples (denoted as samples A, B, C, D, E, F, and G) were grown with the same structure and growth conditions except for the doping profile of the Mg-doped p-GaN layer. Samples A, B, and C have the uniformly doped p-type GaN layer. As shown in Fig. 1(b), the Mg concentrations in the p-type GaN layer for samples A, B, and C were 2.3×10^{19} cm^{-3} (denoted as high doping, p^+-GaN), 1.8×10^{19} cm^{-3} (denoted as medium doping, p-GaN), and 1.2×10^{19} cm^{-3} (denoted as low doping, p^--GaN), respectively. As shown in Fig. 1(c), samples D, E, F, and G have two-step graded-doped p-GaN layer, from bottom to top, consisting of a one p^--GaN layer (Mg: 1.2×10^{19} cm^{-3}) and a one p^+-GaN layer (Mg: 2.3×10^{19} cm^{-3}) with varied thickness distribution: sample D with 350-nm p^--GaN and 50-nm p^+-GaN; sample E with 300-nm p^--GaN and 100-nm p^+-GaN; sample F with 250-nm p^--GaN and 150-nm p^+-GaN; sample G with 200-nm p^--GaN and 200-nm p^+-GaN. The relative Mg concentrations in the p-GaN were calibrated by the secondary-ion mass spectrometry (SIMS) depth-profiling measurements.

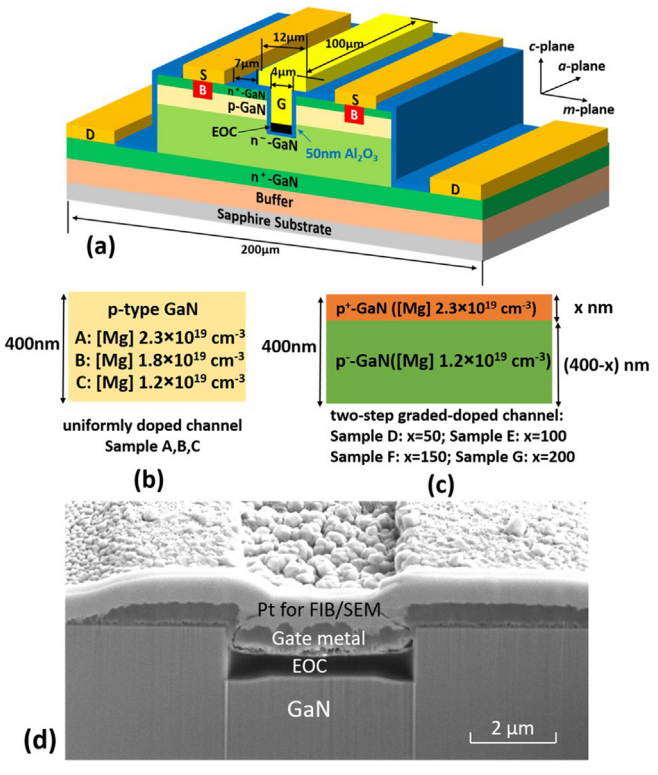

FIG. 1. (a) 3D cross-sectional schematic of fabricated quasi-vertical GaN trench MOSFETs. "S," "D," "G," and "B" refer to "source," "drain," "gate," and "body," respectively. Ethylene octene copolymer (EOC) at the gate trench is used as bottom dielectric to manage the electric field. p-type GaN epi information of (b) uniformly doped channel (samples A, B, and C); (c) step-graded channel (samples D, E, F, and G). (d) Cross-sectional SEM image of the gate trench region of a fabricated device.

Figure 1(a) illustrates the 3D cross-sectional schematic of the fabricated quasi-vertical GaN trench MOSFETs. All seven samples shared the same fabrication process.[10] The device fabrication started with gate trench formation using Cl_2/BCl_3-based inductively coupled plasma (ICP) dry etching with a Ni metal mask, followed by hot tetramethylammonium hydroxide (TMAH) wet etching (at 80 °C for 2 h) to repair the dry etching induced damage in the gate trench. The etching depth of the gate trench is around 1.5 μm. The process continued with mesa formation and exposure of the bottom n^+-GaN layer for drain Ohmic contacts using ICP dry etching. After the p-GaN body contact was opened through ICP dry etching, the buried p-GaN body was then activated via rapid thermal annealing (RTA) at 800 °C for 10 min in a N_2 ambient. Then, samples were cleaned by piranha (H_2SO_4:H_2O_2 = 10:1, at 120 °C for 10 min) + buffered oxide etchant (BOE) (for 2 min) to improve the GaN/Al_2O_3 interface,[10] and a 50-nm Al_2O_3 gate dielectric was subsequently deposited by atomic layer deposition (ALD). After opening the contact holes (removing the gate oxide in the body, source/drain contact regions), the Ni/Au metal stack was deposited and annealed as the body contact, followed by evaporating Ti/Al/Ni/Au metal stack as the source and drain Ohmic contact. Then, a layer of ethylene octene copolymer (EOC, from Everlight Chemical, with a dielectric constant of 3.6, a breakdown field of 4.1 MV/cm, and a glass transition temperature of 230 °C) was blanketly coated to fill the gate trench, cured at 150 °C for 30 min on a hotplate and etched back by O_2 plasma, leaving around 500 nm EOC in the gate trench as the thick bottom dielectric to manage the electric field in the gate trench for enhanced breakdown voltage.[10] The fabrication process ended with sputtering of a Ti/Al metal stack as the gate metal. All the devices reported here feature a rectangular gate trench with an area of 4×100 μm^2. The gate trench sidewalls were aligned to the *m*-plane for better ON-state performance.[9,21] After device fabrication, the gate stack of the device was characterized using scanning electron microscopy (SEM), as shown in Fig. 1(d). The active area of the devices used for specific ON-resistance and current density normalization is (4 μm trench length + 2.5 μm drift region thickness) × (100 μm trench width + 2.5 μm drift region thickness) = 666.25 μm^2, considering the lateral current spreading length (2.5 μm) in the drift region, which is a commonly used method to define the active area in vertical trench MOSFETs with a single trench.[8,9,11,12] The total device area is 200×300 μm^2, including the gate, source, and drain contact pads.

As a baseline study, we first investigated the effects of channel doping concentration in devices with a uniformly doped channel (samples A, B, and C). Figure 2 shows the representative transfer (I_D, $|I_G|$ vs V_{GS})

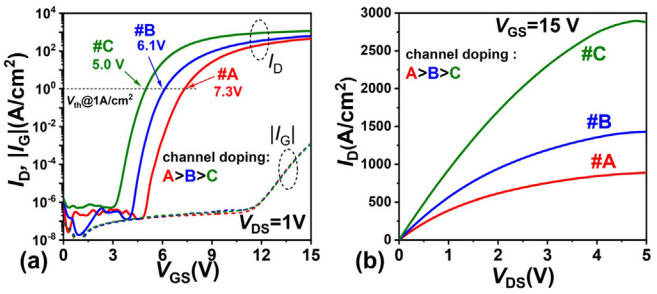

FIG. 2. (a) I_D, $|I_G|$–V_{GS} (at V_{DS} = 1 V) and (b) I_D–V_{DS} (at V_{GS} = 15 V) curves of samples A, B, and C (uniformly doped channel with different channel doping concentrations).

TABLE I. Summary of key device parameters (average value ± standard deviation, measured from at least ten devices on each sample) of samples with different channel doping profiles. $I_{D,max}$ at $V_{GS} = 15$ V and $V_{DS} = 5$ V; $R_{ON,sp}$ at $V_{GS} = 15$ V and $V_{DS} = 0.1$ V.

Sample No.	Channel doping profile	V_{th} (V) @1 A/cm^2	$I_{D,max}$ (A/cm^2)	$R_{ON,sp}$ (mΩ cm^2)	SS (mV/dec)	V_{BR} (V)
A	Uniform doping (high) 400-nm p$^+$-GaN ([Mg]: 2.3×10^{19} cm^{-3})	7.28 ± 0.19	872 ± 124	2.08 ± 0.24	291 ± 29	243 ± 23
B	Uniform doping (medium) 400-nm p-GaN ([Mg]: 1.8×10^{19} cm^{-3})	5.94 ± 0.13	1360 ± 185	1.54 ± 0.14	272 ± 17	238 ± 27
C	Uniform doping (low) 400-nm p$^-$-GaN ([Mg]: 1.2×10^{19} cm^{-3})	5.02 ± 0.16	2933 ± 212	1.02 ± 0.16	279 ± 21	234 ± 19
D	Two-step graded doping 350-nm p$^-$-GaN ([Mg]: 1.2×10^{19} cm^{-3}) + 50-nm p$^+$-GaN ([Mg]: 2.3×10^{19} cm^{-3})	5.49 ± 0.14	2632 ± 207	1.12 ± 0.19	275 ± 15	239 ± 21
E	Two-step graded doping 300-nm p$^-$-GaN ([Mg]: 1.2×10^{19} cm^{-3}) + 100-nm p$^+$-GaN ([Mg]: 2.3×10^{19} cm^{-3})	6.03 ± 0.22	2173 ± 232	1.24 ± 0.17	281 ± 21	243 ± 17
F	Two-step graded doping 250-nm p$^-$-GaN ([Mg]: 1.2×10^{19} cm^{-3}) + 150-nm p$^+$-GaN ([Mg]: 2.3×10^{19} cm^{-3})	6.35 ± 0.18	1985 ± 196	1.39 ± 0.13	287 ± 25	231 ± 25
G	Two-step graded doping 200-nm p$^-$-GaN ([Mg]: 1.2×10^{19} cm^{-3}) + 200-nm p$^+$-GaN ([Mg]: 2.3×10^{19} cm^{-3})	6.62 ± 0.21	1725 ± 187	1.49 ± 0.21	285 ± 19	241 ± 22

curves [Fig. 2(a)] and output (I_D vs V_{DS}) curves [Fig. 2(b)] of devices on samples A, B, and C. All samples show a similarly high ON/OFF current ratio of ~10^9 and a similar gate current (I_G) of ~1×10^{-3} A/cm^2 at $V_{GS} = 15$ V. From samples A, B to C, V_{th} (defined at $I_D = 1$ A/cm^2) decreases from 7.3, 6.1 to 5.0 V, following the channel doping reduction as expected. On the contrary, from samples A, B to C, $R_{ON,sp}$ decreases from 2.01, 1.52 to 1.01 mΩ cm^2 (181, 137 to 90.9 mΩ cm^2 when using total device area for $R_{ON,sp}$ normalization), corresponding to a dramatic increase in the $I_{DS,max}$ from 895, 1425 to 2893 A/cm^2. Under the same overdrive gate voltage ($V_{GS,max}$–V_{th} of sample A), I_D (at $V_{DS} = 5$ V) also increases and R_{ON} decreases from samples A, B to C [details shown in Fig. S2(a) of the supplementary material], indicating that the increase in $I_{D,max}$ and the reduction of $R_{ON,sp}$ at the same maximum gate bias ($V_{GS,max} = 15$ V) from samples A to C is a result of both increased electron carrier concentration (due to higher overdrive gate voltage) and enhanced effective channel mobility. Since the devices on the three samples shared the same process and epilayer structure except for channel doping concentration, the reduction in $R_{ON,sp}$ mainly results from the decrease in the inversion channel resistance with the decreased channel doping. The extracted electron mobility of the inversion channel[7] (considering the drift layer resistance of ~0.16 mΩ cm^2 and contact resistance of ~0.18 mΩ cm^2) is found enhanced from 10.3, 14.2 to 24.1 cm^2/V s from samples A, B to C, which can be attributed to the reduced impurity scattering with lower channel doping.[7,27] For the OFF-state performance, samples A, B, C show a similar breakdown voltage (V_{BR}) (hard breakdown) of around 240 V. All the average values (measured from at least ten devices on each sample) of device key parameters are summarized in Table I. We found that there is a strong impact of p-GaN doping concentration on the $R_{ON,sp}$, $I_{D,max}$, and V_{th} of vertical GaN trench MOSFETs with uniformly doped channel. Increasing the p-GaN body doping concentration leads to an increased V_{th}, with a cost of a decreased $I_{D,max}$ and an increased $R_{ON,sp}$.

Next, we present the device performance of samples D–G with step-graded channel of decreasing ratio of the low- and highly doped p-GaN (total channel thickness kept at 400 nm). Figure 3 shows the representative transfer curves and output curves (at $V_{GS} = 15$ V) of devices on samples D, E, F, and G. All samples show similar high ON/OFF current ratio of ~10^9 and a similar gate current (I_G) of ~1×10^{-3} A/cm^2 at $V_{GS} = 15$ V. From samples D to G, V_{th} increases from 5.6, 6.0, 6.5 to 6.8 V, while $R_{ON,sp}$ increases from 1.14, 1.22, 1.38 to 1.47 mΩ cm^2 (103, 110, 124 to 132 mΩ cm^2 when using total device area for $R_{ON,sp}$ normalization), corresponding to a reduction of $I_{DS,max}$ from 2709, 2144, 1899 to 1729 A/cm^2. Under the same overdrive gate voltage, the same trend as in the uniformly doped samples was observed [Fig. S2(b) of supplementary material] for the samples with step-graded channel doping. All the average values (measured from at least ten devices on each sample) of the device key parameters for samples with step-graded channel are also summarized in Table I. The average V_{BR} (hard breakdown) for samples D, E, F, and G is in the range of 230–250 V. Breakdown behavior for samples A–G is nearly identical. It is found that all samples show similar average values of subthreshold slope (SS), ranging from 270 to 300 mV/dec.

Figure 4(a) summarizes the experimental average values of $R_{ON,sp}$ and $I_{D,max}$ and V_{th} vs the highly doped channel (p$^+$-GaN) layer thickness. Samples A and C are also included for comparison since doping profile can be treated as "0-nm p$^-$-GaN + 400-nm p$^+$-GaN" in sample A and as "400-nm p$^-$-GaN + 0-nm p$^+$-GaN" in sample C. It can be observed that with the decreasing p$^+$-GaN layer thickness, a reduced V_{th}, a decreased $R_{ON,sp}$, and an enhanced $I_{D,max}$ can be observed. The experimental restuls of the two-step graded-doped

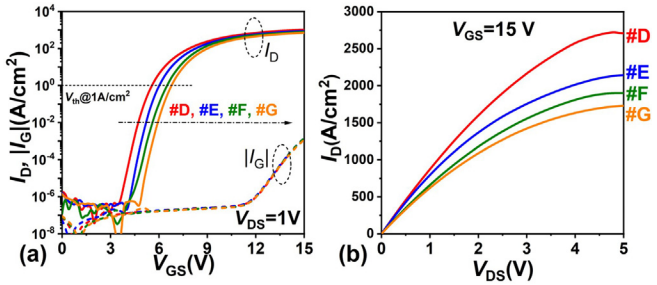

FIG. 3. (a) I_D, $|I_G|$–V_{GS} (at $V_{DS} = 1$ V) and (b) I_D–V_{DS} (at $V_{GS} = 15$ V) curves of samples D, E, F, and G (two-step graded-doped channel with different thickness distributions of high and low doping channels).

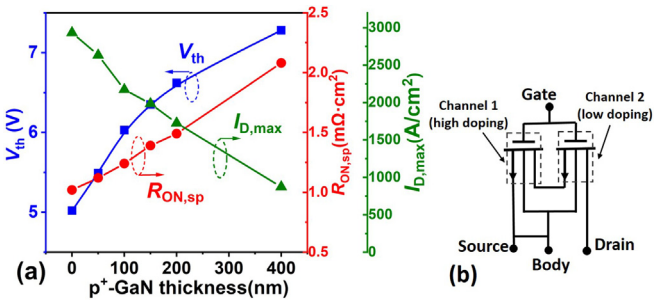

FIG. 4. (a) Experimental values of $R_{ON,sp}$, $I_{D,max}$, and V_{th} vs p^+-GaN layer thickness. Data points on p^+-GaN thickness = 0, 50, 100, 150, 200, and 400 nm correspond to samples C, D, E, F, G, and A, respectively. (b) Equivalent two-transistor sub-circuit model[25] for step-graded channel.

channel devices can be explained by a simplfied equivalent two-transistor sub-circuit model,[25] with the high- and low-doped channels connected in series and the gate and body regions tied together, as shown in Fig. 4(b). The total channel resistance consists of two series resistances, and each resistance value varies linearly with its channel length. Since we have observed a higher channel resistance (lower channel mobility) in the higly doped channel in the previous investigation of uniformly doped samples A, B, and C, with the decrease in high doping channel layer thickness (correspongding to the channel lenghth in the vertical MOSFET), the total channel resistance decreases, leading to the reduced $R_{ON,sp}$ and increased $I_{D,max}$. The V_{th} of the two-step doped channel is mainly determined by the highly doped portion of the channel, which is still in the OFF-state after turning-ON of the low-doped portion. What is more, due to the short channel effect, the V_{th} rolling-off is reasonable with the decrease in highly doped channel thickness (channel length) in the sub-mircometer level.[28]

Figure 5 summarizes the experimental results (using the average values) of $R_{ON,sp}$ vs V_{th} [Fig. 5(a)] and $I_{D,max}$ vs V_{th} [Fig. 5(b)] of all seven samples. Compared with the uniformly doped channel design, the two-step graded-doped design shows an improved trade-off among $I_{D,max}$, $R_{ON,sp}$, and V_{th} for vertical GaN MOSFETs. For example, in the uniformly doped channel design, from sample C to sample B, ~1 V positive shift of V_{th} can be obtained with the cost of significant sacrifice in $R_{ON,sp}$ (51% higher) and $I_{D,max}$ (54% lower). While in the step-graded channel design, from sample C to sample E, ~1 V positive shift of V_{th} can be obtained with much less sacrifice in $R_{ON,sp}$ (21% higher) and $I_{D,max}$ (26% lower). Technology computer-aided design (TCAD) simulation results of $R_{ON,sp}$ and $I_{D,max}$ vs V_{th} in devices with two-step graded-channel [with varied high and low doping channel thickness distributions, shown in Fig. 5(c)] are included in Figs. 5(a) and 5(b). In this TCAD simulation, relative parameters of the two-step channel were adjusted to fit between the experimental values obtained from sample A and sample C. The simulation results of the devices with two-step doped channel generally fit the trend of the experiental results. We also notice that there are some differences between the simulation and experimental results, especially for the V_{th} values (simlated values are higher than the experimental ones). This is possibly because only fixed charges at the MOS interface without any trap states were taken into consideration in the TCAD model, which may influence the short-channel-effect related V_{th} rolling-off.[29,30]

In conclusion, we present an investigation of the step-graded p-doped channel design in quasi-vertical GaN MOSFETs. Devices with

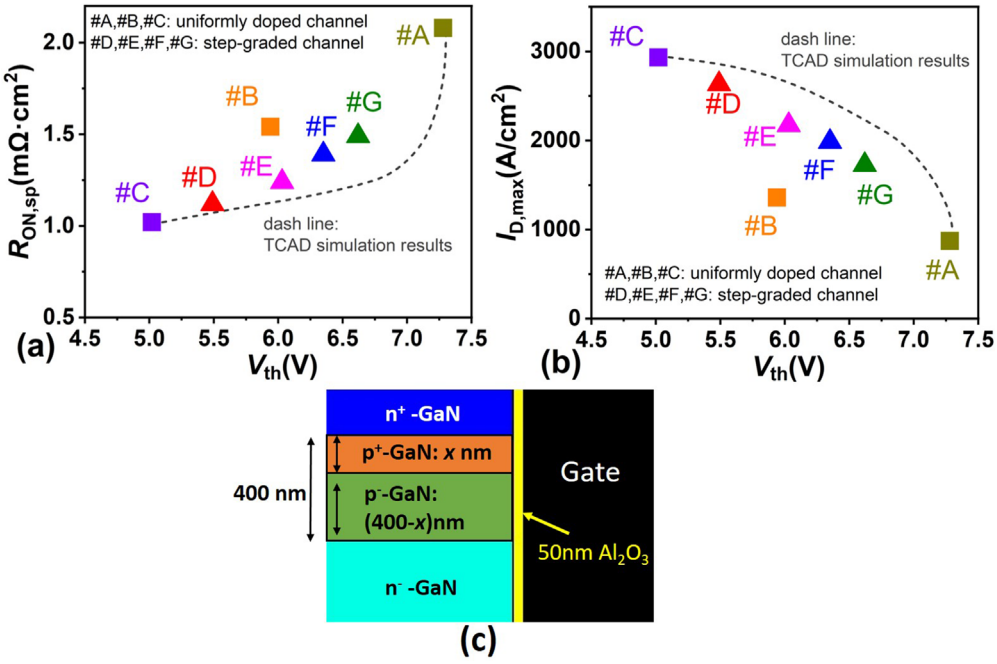

FIG. 5. Experimental results of (a) $R_{ON,sp}$ vs V_{th} and (b) $I_{D,max}$ vs V_{th} of all fabricated seven samples. (c) Simulation structures of device with two-step graded-doped channel. The simulation results are also included in (a) and (b).

conventional design (uniformly p-type doped channel) are also included for comparison. From the experimental results, through tuning the thickness ratio of the high- and low-doped channels, trade-off between $I_{D,max}$, $R_{ON,sp}$, and V_{th} can be clearly observed. Thicker highly doped channel can lead to an increased V_{th}, with a cost of higher $R_{ON,sp}$ and reduced $I_{D,max}$. Compared with the uniform channel doping design, the step-graded channel doping design shows an improved trade-off between the key device characteristics, $I_{D,max}$, $R_{ON,sp}$, and V_{th}, of quasi-vertical GaN MOSFETs. The potential of step-graded channel doping in channel engineering of GaN vertical power MOSFETs is illustrated.

See the supplementary material for MOCVD growth information, SIMS results, I_D–V_{DS} curves measured under the same overdrive gate voltage, inversion channel mobility extraction, representative I–V curves of device breakdown, and TCAD simulation details.

This work was supported by the Research Grants Council of Hong Kong under General Research Fund Grant No. 16215818 and the Innovation and Technology Fund of Hong Kong (No. MRP/039/21). The authors thank the staff of the Nanosystem Fabrication Facility (NFF) and the Material Characterization and Preparation Facility (MCPF) at HKUST for their technical support.

AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Renqiang Zhu: Conceptualization (equal); Data curation (lead); Investigation (lead); Methodology (lead); Writing – original draft (lead); Writing – review and editing (lead). **Huaxing Jiang:** Conceptualization (supporting); Writing – review and editing (supporting). **Chak Wah Tang:** Investigation (supporting); Methodology (supporting). **Kei May Lau:** Conceptualization (lead); Project administration (lead); Writing – review and editing (supporting).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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