Telecom InGaAs/InP Quantum Well Lasers Laterally Grown on Silicon-on-Insulator

Jie Li, Ying Xue, Liying Lin, Zengshan Xing, Kam Sing Wong, and Kei May Lau, *Fellow, IEEE*

***Abstract*— To achieve on-chip lasers for Si-photonics, monolithic integration using selective epitaxy is a favorable option due to the unique defect engineering and resultant bufferless structure. Among the intensively investigated selective epitaxy methods, lateral aspect ratio trapping generates III-V devices in the same plane as the Si layer enabling efficient coupling with Si waveguides. Here, we demonstrate telecom InGaAs/InP quantum well lasers selectively grown on commercial silicon-on-insulator substrates with an in-plane structure using a simple structural design and growth scheme without any regrowth steps. Leveraging on the lateral aspect ratio trapping technique, uniform quantum wells with high crystalline quality were obtained and shown by comprehensive material characterizations. Room temperature pulsed lasing was achieved on the fabricated micro-ring lasers with a low threshold of 20 μJ/cm^2. The results present a crucial step towards electrically pumped lasers at telecom band as well as fully integrated Si-photonics.**

***Index Terms*—Epitaxial growth, optical communication, quantum well lasers.**

I. Introduction

SI-PHOTONICS is a promising technology to ease the pressing issue of exploring data communications, due to its large bandwidth capability, cost-effective and scalable manufacturing [1]–[5]. In Si-photonics systems, Si is mainly used for passive components [6], and III-V materials with direct bandgap were introduced onto the Si platform to provide the crucial function of light-emitting [7]. On-chip lasers for Si-photonics need to be equipped with low threshold, high reliability, and can be efficiently coupled with Si-waveguides.

To realize monolithic III-V lasers on Si, many researchers have concentrated on blanket epitaxy of III-V thin films on Si and reported remarkable lasing results [8]–[10]. However, the strategy of efficient light coupling with Si-based passive components is yet to be demonstrated. Defect engineering to resolve the 8% lattice mismatch between InP and Si has been the primary research of hetero-epitaxy of InP and its lattice-matched alloys on Si which most telecom-band optoelectronic devices built on [11]–[13]. In blanket epitaxy, the thick "buffer" layers used for defect reduction result in a large height difference between the III-V gain region and the Si layer, leading to inefficiency and complexity in light coupling. In most integrated circuits, the area of active components is usually a small percentage of the die. To planarize the III-V gain and Si waveguide layers, selective epitaxy using aspect ratio trapping (ART) can be applied for eliminating the thick buffer.

Selective epitaxy methods such as vertical ART and nano-ridge engineering (NRE) generate III-V devices on a "bufferless" platform with vertical configuration. Optically pumped telecom lasers and electrical devices (such as photodetectors) have been demonstrated on this platform [14]–[16]. In these prior works, the limited material volume is insufficient for the demonstration of electrically pumped lasers, and the height difference between the III-V gain region and Si waveguides still limits the coupling efficiency. Furthermore, the defective III-V/Si interface in the current path could jeopardize the device performance. Alternatively, selective epitaxy methods such as template-assisted selective epitaxy (TASE) and lateral aspect ratio trapping (LART) generate devices in lateral configuration. Using these methods, III-V materials can be grown in the same plane as the Si layer, thereby eliminating the height difference between them. Also, the unique III-V on insulator feature will benefit the optical confinement of the lasers. The demonstrations based on the TASE technique focus on nano-scale devices which are extremely difficult to fabricate into electrically driven lasers. In contrast, using the LART technique, III-V membrane with large dimension and in-plane structure can be grown on silicon-on-insulator (SOI) which is promising for the realization of electrically pumped lasers and efficient coupling with Si waveguides simultaneously [17], [18]. Furthermore, the defective III-V/Si interface is a small portion of the laterally grown III-V volume and in-plane structure. GaAs lasers on SOI emitting at 860 nm

Manuscript received 4 March 2022; revised 17 May 2022; accepted 28 May 2022. Date of publication 10 June 2022; date of current version 16 August 2022. This work was supported in part by the Research Grants Council, University Grants Committee under Grants 16212115, 16245216, 16213420, and AoE/P-02/12, in part by the Innovation and Technology Fund under Grants ITS/273/16FP and ITS/201/19FP, and in part by the William Mong Institute of Nano Science and Technology under Grant WMINST19SC04. *(Jie Li, Ying Xue, and Liying Lin contributed equally to this work.) (Corresponding author: Kei May Lau.)*

Jie Li, Ying Xue, and Liying Lin are with the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Kowloon, Hong Kong (e-mail: jlifo@connect.ust.hk; yxueag@connect.ust.hk; llinao@connect.ust.hk).

Zengshan Xing and Kam Sing Wong are with the Department of Physics and William Mong Institute of Nano Science and Technology, Hong Kong University of Science and Technology, Kowloon, Hong Kong (e-mail: zxingaa@connect.ust.hk; phkswong@ust.hk).

Kei May Lau is with the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Kowloon, Hong Kong, and also with the Microelectronic Thrust, Hong Kong University of Science and Technology (GZ), Guangzhou, China (e-mail: eekmlau@ust.hk).

Color versions of one or more figures in this article are available at https://doi.org/10.1109/JLT.2022.3181723.

Digital Object Identifier 10.1109/JLT.2022.3181723

and InP lasers on SOI emitting at 920 nm have been demonstrated using TASE and LART technique, respectively [17], [19]. However, telecom lasers on SOI have yet to be reported using these methods with lateral configuration. Combining selective epitaxy, regrowth, and bonding techniques, telecom lasers on SOI were reported [20]–[26]. However, the multiple regrowth steps and the complex fabrication process used in this method add uncertainties to the integration and possibly affect the yield.

Here, we demonstrated telecom InGaAs/InP quantum well (QW) lasers on SOI by selective lateral epitaxy with a simple structural design. The whole laser structure can be grown in the same growth scheme [17] without any regrowth step involved. Fairly uniform QWs with clear interfaces were achieved and verified from comprehensive transmission electron microscopy (TEM) and micro-photoluminescence (μ-PL) characterization. Room temperature (RT) pulsed lasing of micro-ring lasers (MRLs) was achieved at the telecom band with a low threshold of 20 μJ/cm^2.

II. Lateral Quantum Well Grown on SOI

Built on our previously designed InP/SOI platform [17], we extended the lateral growth scheme for InGaAs/InP QW to achieve emission in telecom band. The whole structure was grown in an AIXTRON closed-couple-showerhead (CCS) metal-organic chemical vapor deposition (MOCVD) system. Trimethylindium (TMIn), trimethylgallium (TMGa) were used as group III precursors, and tertiary-butyl phosphine (TBP), tertiary-butyl arsine (TBA) were used as group V precursors, with H_2 as carrier gas. Fig. 1(a) depicts the procedure for the growth of InGaAs/InP QWs sandwiched by the InP claddings. Lateral oxide trenches with a 7 μm undercut were created on commercial SOI wafers using our optimized dry etching and wet etching steps which are detailed in [17], [18]. As a result, the 55° angle between {111} and {001} Si facets was exposed with the {111} facet as the growth front. Then InP nucleation layer, inner InP, 28 periods of QWs, and outer InP sections were grown in sequence as delineated in Fig. 1(b). We defined the InP cladding near the Si as inner InP, while those near the trench opening were defined as outer InP. Prior to the growth, 815 °C annealing for 15 min was performed to desorb the native oxide. TBA pre-flow was introduced into the chamber before nucleation to create As-terminated {111} Si facets to ease the InP nucleation. Then 400 °C low-temperature InP was grown as the nucleation layer with a V/III ratio of 1400, followed by the growth of 2.8 μm inner InP. The crystalline quality of lateral III-V highly depends on the growth of the InP nucleation layer. The optimal temperature of 400 °C, high V/III ratio of 1400, and growth speed associated with the temperature contribute to a uniform InP nucleation layer which facilitates the coalescence of high-temperature InP and high-quality epitaxial growth. Other details of the InP nucleation layer can be found in [17]. After that, QW consisting of 10 nm InGaAs well and 32 nm InP barrier was grown for 28 periods (see Fig. 1(c)). The 28 periods of QWs were designed for sufficient gain of the in-plane micro-lasers with a small footprint. Finally, a 2.8 μm outer section of InP

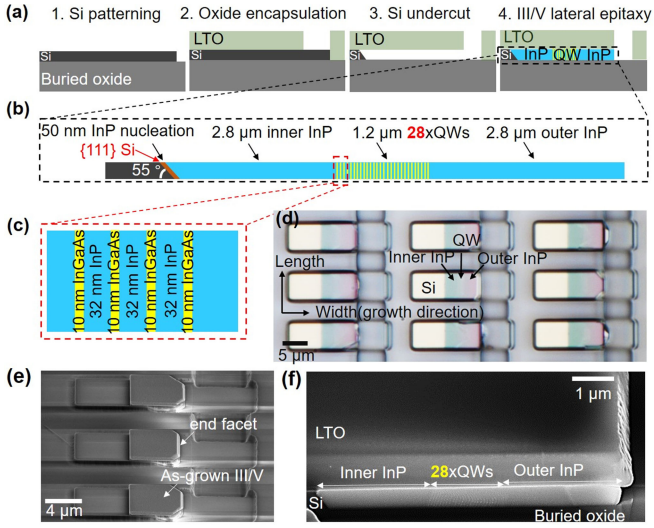

Fig. 1. (a) Schematic illustrating the procedure of lateral quantum well growth. (b) Schematic showing the designed growth structure and thickness of each layer. (c) Schematic showing the growth structure of InGaAs/InP quantum well. (d) Global-view microscope image of the as-grown lateral structure on SOI. (e) Tilted view SEM image of lateral quantum well grown on SOI after removing top oxide and Si. (f) Cross-sectional SEM image of lateral quantum well grown on SOI, with each layer labelled.

was grown according to the widest epitaxial width of 7 μm to add tolerance for E-beam lithography when defining MRLs. As the diameter of MRLs was designed to be around 4 μm to achieve lasing at the telecom band, the 7 μm total epitaxial width was designed to provide a sufficient material volume for fabrication distancing from the defective region near Si. All of the inner InP, QWs, and outer InP were grown under 620 °C. The as-grown III-V membranes present good uniformity and sufficient width for device demonstration as evidenced in the optical microscope image in Fig. 1(d).

The Scanning Electron Microscope (SEM) image in Fig. 1(e) presents a tilted view of the membranes after top oxide and Si removal, which reveals the flat top (001) facets and straight end facets of the as-grown membranes. The 28 periods of InGaAs/InP QWs located between the inner InP cladding and outer InP cladding can be identified in the cross-sectional SEM image in Fig. 1(f). The thickness of each layer in the as-grown structure fits well with the value we designed in the schematic.

III. Material Characterization

The optical properties of the as-grown QWs were studied by RT μ-PL measurements, as shown in Fig. 2. A 514 nm diode laser with a pumping power of 1.25 mW was used as the excitation source. In optimizing the growth structure, suitable QW volume, diffusion rate, and decomposition percentage of precursors under a certain growth temperature were experimented. We performed various growth time for the QW and tuned the parameters based on the RT μ-PL results as displayed in Fig. 2(a). A short growth time will cause insufficient decomposition of precursors

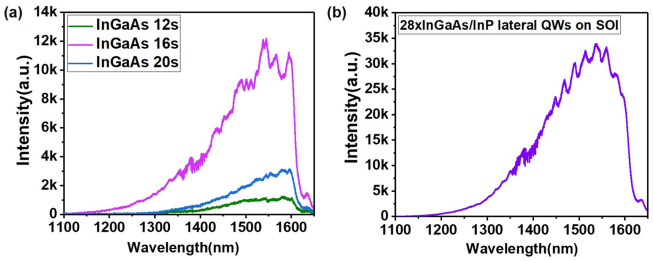

Fig. 2. (a) RT μ-PL characterization of QWs with different growth time. (b) RT μ-PL characterization of optimal as-grown 28 periods of QWs on SOI.

for the 7 μm deep trenches. A long growth time will lead to degradation of the carrier confinement and red-shift of emission wavelength due to the thick QW layer. Fig. 2(b) presents the RT μ-PL spectra of the as-grown 28 periods of InGaAs/InP QWs on SOI after optimization with a peak wavelength of 1550 nm. The full-width-at-half-maximum (FWHM) of the spectrum is related to the uniformity and quality of as-grown QWs. For lateral QWs, a slower growth rate was preferred to facilitate a uniform QW deposition. Note that we also observed equally spaced resonant peaks, suggesting light oscillation inside the lateral cavity [27].

The crystal quality of the as-grown structure was further investigated by observing cross-sectional TEM. As illustrated in Fig. 3(a), we prepared TEM lamella on one of the segments with 10 μm length, along the lateral growth direction. Fig. 3(b) displays the global-view TEM image of the specific segment with 28 periods of InGaAs/InP QWs, corresponding to the SEM image in Fig. 1(f). The laterally arranged QWs manifest excellent uniformity and high crystalline quality without any defect observed as evidenced in Fig. 3(c). The growth front of the lateral QWs consisted of (111) facets on the small upper and lower sides and (110) facets in most regions in the middle. The thickness difference between (110) and (111) facets shown in Fig. 3(e) is induced by growth preference on different facets for minimizing the total surface energy during the selective epitaxy [28]. We also observed the evolution of crystalline growth front by monitoring the development of facets from the first QW to the 28th QW. The InGaAs wells can be treated as growth markers to trace the growth front during different stages of growth. The QWs featuring atomic sharp interfaces with good uniformity can be confirmed by the zoomed-in TEM image in Fig. 3(d).

In addition to the uniform distribution of QWs, we also found defect filtering functionality of the QWs on the last grown InP. As compared with the inner InP cladding in Fig. 3(f), which contains some stacking faults (SFs) and threading dislocations (TDs), the outer InP cladding after the QW growth displays no defect as shown in Fig. 3(g). The result agrees well with the RT μ-PL characterization (Fig. 3(h)). After the QWs, the InP shows a reduction on FWHM by 17% from 43 meV to 36 meV. Similar to the superlattice filtering effect, the specific mechanism can be explained as: The growth preference on different growth facets results in slight inhomogeneities of indium

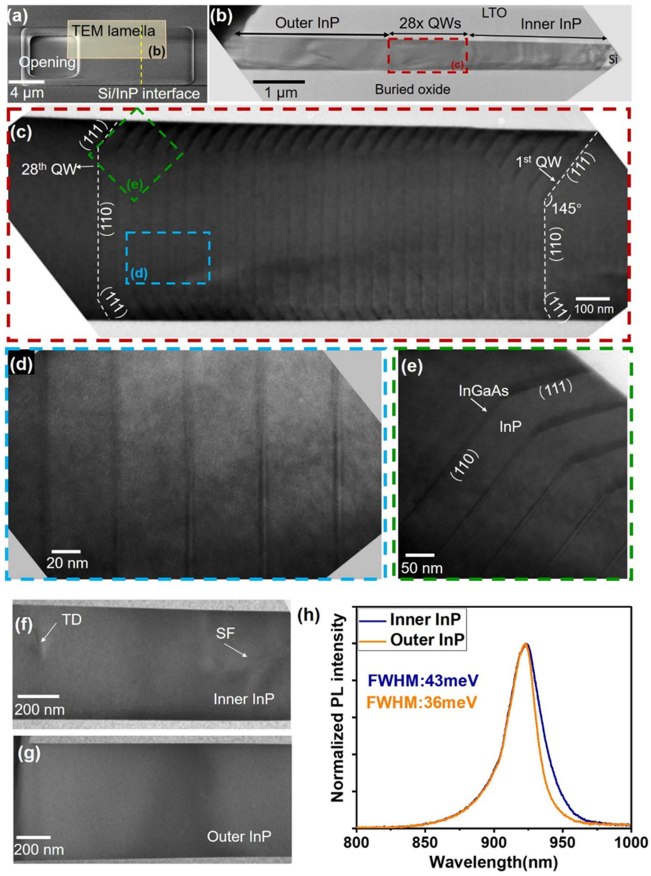

Fig. 3. (a) Tilted view SEM image of the segment for TEM characterization and schematic of TEM lamella along the lateral growth direction. (b) Global-view TEM image of lateral InGaAs/InP quantum wells grown on SOI. (c) Zoomed-in TEM image of 28 periods of InGaAs/InP quantum wells. (d) Zoomed-in TEM image of the uniform InGaAs/InP quantum wells on (110) facet. (e) Zoomed-in TEM image of quantum wells on (110) and (111) facet. (f) Zoomed-in TEM image of inner InP cladding. (g) Zoomed-in TEM image of outer InP cladding. (h) RT μ-PL comparison of inner InP and outer InP.

composition and strain field in QWs. As the period of QW layers increases, the stress accumulates gradually, so SFs and grain boundaries can be blocked at the hetero-interface [29]–[32]. As a result, the crystalline quality of InP was improved after growing QWs.

IV. Device Fabrication and Results

The as-grown sample was then fabricated into MRLs with the process steps depicted in Fig. 4(a). After removing the top low-temperature oxide (LTO), 200 nm oxide was deposited by plasma-enhanced chemical vapor deposition (PECVD) as a hard mask. Then the ring shapes were defined using E-beam lithography and a subsequent oxide etching step. Finally, the cavity was formed by transferring the ring shapes to the III-V layer using inductively coupled plasma (ICP) etching. Fig. 4(b) displays the MRL array on the SOI in a global view. We fabricated MRLs with the same outer diameter of 3.8 μm and different ring widths of 0.8, 1, and 1.2 μm. The good circularity of the MRLs was shown in the top-view SEM image of a MRL with 1 μm ring

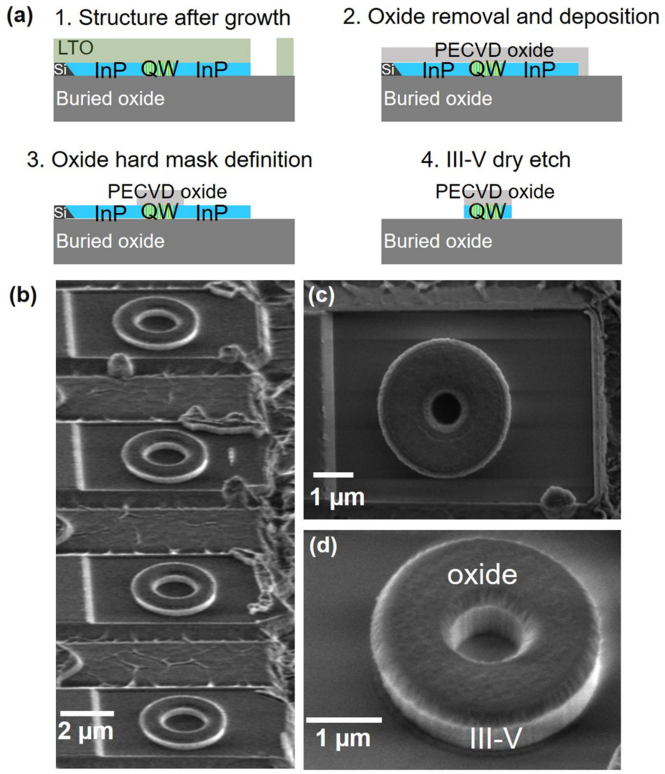

Fig. 4. (a) Fabrication process of the micro-ring lasers on SOI. (b) Tilted view SEM image of micro-ring laser array on SOI. (c) Top-view SEM image of a micro-ring laser with 1 μm ring width and 3.8 μm outer diameter. (d) Tilted view SEM image showing sidewall of the fabricated micro-ring laser.

width in Fig. 4(c). Fig. 4(d) displays the tilted-view SEM image showing the smooth sidewall of the MRL.

We characterized the lasers using a home-built PL setup that was described in reference 17. RT pulsed lasing was achieved for MRLs with all the designed dimensions. Fig. 5(a) presents a representative RT power-dependent PL spectra of the MRL in a log scale. Under low excitation levels, the spectra exhibit a broad spontaneous emission. With the progressively increasing pumping power, a sharp peak located at around 1580 nm gradually stuck out from the spontaneous emission and finally lased. The Light-light (*L-L*) curve of the MRL with a 1 μm ring width was plotted in Fig. 5(b). A low threshold of 20 μJ/cm^2 was measured for the MRL with 1 μm ring width. The lasers with different dimensions show similar lasing thresholds due to their comparable gain volume. In the future, we might be able to obtain a lower threshold and a higher slope efficiency by reducing the SFs density in the as-grown III-V crystals and improving the sidewall smoothness of the MRLs. The linewidth reduction plotted in Fig. 5(c) further certified the lasing of the MRL.

Compared with the telecom lasers grown by vertical ART [14]–[16], [28], our telecom lasers grown by LART feature an in-plane structure with Si which will facilitate efficient light coupling with Si waveguides. The optical confinement is also enhanced by the III-V-on-insulator structure enabled by LART. Compared with our previous report of pure InP lasers emitting at 920 nm [17], the demonstration of telecom lasers emitting in

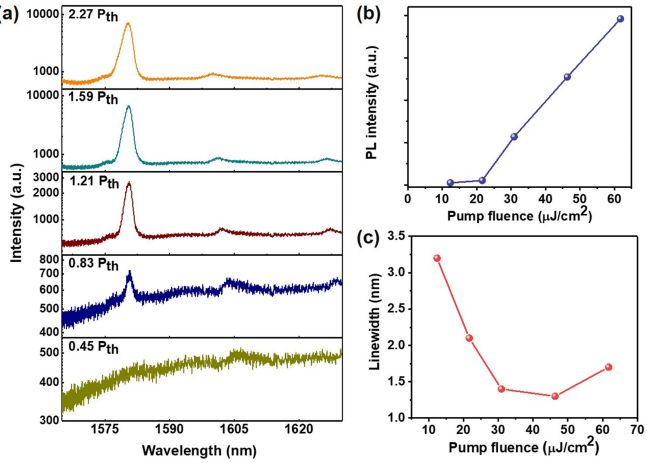

Fig. 5. (a) RT power-dependent PL spectra of a representative MRL with 1 μm ring width. (b) Light–light (*L–L*) curve of corresponding MRL. (c) Linewidth of corresponding MRL.

the 1.5 μm band on SOI signifies a step towards the practicality of on-chip lasers for Si-photonics.

V. Conclusion

In summary, based on our previously demonstrated InP-on-SOI platform [17], we incorporated 28 periods of InGaAs/InP QWs as the active region sandwiched in the InP crystals by the LART technique. Uniform QWs with high crystal quality were obtained as evidenced by the PL and TEM characterization. RT telecom band lasing was achieved with a low threshold of 20 μJ/cm^2 through fabricating MRLs on the as-grown in-plane structure. These promising results provide a possible solution of electrically pumped lasers at the telecom band, paving the way toward fully integrated Si-photonics.

Acknowledgment

The authors would like to thank the Material Characterization & Preparation Facility (MCPF) and the Nanosystem Fabrication Facility (NFF) of HKUST for technical support, and many helpful discussions with Zhao Yan, Yu Han, Jie Huang, Wei Luo, and Ka Ming Wong.

References

[1] Y. Han, Y. Xue, Z. Yan, and K. M. Lau, "Selectively grown III-V lasers for integrated Si-photonics," *J. Lightw. Technol.*, vol. 39, no. 4, pp. 940–948, Feb. 2021.
[2] B. Jalali and S. Fathpour, "Silicon photonics," *J. Lightw. Technol.*, vol. 24, no. 12, pp. 4600–4615, Dec. 2006.
[3] D. Thomson *et al.*, "Roadmap on silicon photonics," *J. Opt.*, vol. 18, no. 7, Jun. 2016, Art. no. 073003.
[4] Y. Matsui *et al.*, "Low-chirp isolator-free 65-GHz-bandwidth directly modulated lasers," *Nat. Photon.*, vol. 15, no. 1, pp. 59–63, 2021.
[5] K. Xu, "Silicon electro-optic micro-modulator fabricated in standard CMOS technology as components for all silicon monolithic integrated optoelectronic systems," *J. Micromechan. Microeng.*, vol. 31, no. 5, 2021, Art. no. 054001.
[6] R. Won, "Integrating silicon photonics," *Nature Photon.*, vol. 4, no. 8, pp. 498–499, Aug. 2010.
[7] D. Liang and J. E. Bowers, "Recent progress in lasers on silicon," *Nature Photon.*, vol. 4, no. 8, pp. 511–517, Nov. 2010.

[8] Y. Wan *et al.*, "1.3 μm submilliamp threshold quantum dot micro-lasers on Si," *Optica*, vol. 4, no. 8, pp. 940–944, Aug. 2017.
[9] W. Luo *et al.*, "MOCVD growth of inp-based 1.3 μm quantum dash lasers on (001) Si," *Appl. Phys. Lett.*, vol. 116, Apr. 2020, Art. no. 142106.
[10] Y. Xue *et al.*, "1.55 μm electrically pumped continuous wave lasing of quantum dash lasers grown on silicon," *Opt. Exp.*, vol. 28, no. 12, pp. 18172–18179, Jun. 2020.
[11] A. Krost, F. Heinrichsdorff, and D. Bimberg, "InP on si (111): Accommodation of lattice mismatch and structural properties," *Appl. Phys. Lett.*, vol. 64, no. 6, pp. 769–771, 1994.
[12] K. Samonji *et al.*, "Reduction of threading dislocation density in inp-on-Si heteroepitaxy with strained short-period superlattices," *Appl. Phys. Lett.*, vol. 69, no. 1, pp. 100–102, 1996.
[13] B. Shi and J. Klamkin, "Defect engineering for high quality InP epitaxially grown on on-axis (001) Si," *J. Appl. Phys.*, vol. 127, Jan. 2020, Art. no. 033102.
[14] Y. Han *et al.*, "Bufferless 1.5 μm III-V lasers grown on Si-photonics 220 nm silicon-on-insulator platforms," *Optica*, vol. 7, no. 2, pp. 148–153, Feb. 2020.
[15] Y. Han *et al.*, "Room-temperature InP/InGaAs nano-ridge lasers grown on Si and emitting at telecom bands," *Optica*, vol. 5, no. 8, pp. 918–923, Jul. 2018.
[16] Y. Xue *et al.*, "Bufferless III–V photodetectors directly grown on (001) silicon-on-insulators," *Opt. Lett.*, vol. 45, no. 7, pp. 1754–1757, Mar. 2020.
[17] Z. Yan *et al.*, "A monolithic InP/SOI platform for integrated photonics," *Light Sci. Appl.*, vol. 10, no. 1, pp. 1–10, Sep. 2021.
[18] Y. Xue *et al.*, "High-performance III-V photodetectors on a monolithic InP/SOI platform," *Optica*, vol. 8, no. 9, pp. 1204–1209, Sep. 2021.
[19] B. F. Mayer *et al.*, "Microcavity lasers on silicon by template-assisted selective epitaxy of microsubstrates," *IEEE Photon. Technol. Lett.*, vol. 31, no. 13, pp. 1021–1024, Jul. 2019.
[20] S. Matsuo *et al.*, "Directly modulated buried heterostructure DFB laser on SiO 2/Si substrate fabricated by regrowth of InP using bonded active layer," *Opt. Exp.*, vol. 22, no. 10, pp. 12139–12147, May 2014.
[21] C. Zhang, D. Liang, and J. E. Bowers, "MOCVD regrowth of InP on hybrid silicon substrate," *ECS Solid State Lett.*, vol. 2, no. 11, Nov. 2013, Art. no. Q82.
[22] T. Fujii *et al.*, "Multiwavelength membrane laser array using selective area growth on directly bonded InP on SiO 2/Si," *Optica*, vol. 7, no. 7, pp. 838–846, Jul. 2020.
[23] G. Crosnier *et al.*, "Hybrid indium phosphide-on-silicon nanolaser diode," *Nature Photon.*, vol. 11, no. 5, pp. 297–300, Apr. 2017.
[24] K. Tanabe, K. Watanabe, and Y. Arakawa, "III-V/Si hybrid photonic devices by direct fusion bonding," *Sci. Rep.*, vol. 2, no. 1, pp. 1–6, Apr. 2012.
[25] Y. T. Hu *et al.*, "III/V-on-Si MQW lasers by using a novel photonic integration method of regrowth on a bonding template," *Light Sci. Appl.*, vol. 8, no. 1, pp. 1–9, Oct. 2019.
[26] H. Duprez *et al.*, "1310 nm hybrid InP/InGaAsP on silicon distributed feedback laser with high side-mode suppression ratio," *Opt. Exp.*, vol. 23, no. 7, pp. 8489–8497, Mar. 2015.
[27] Y. Han *et al.*, "Micrometer-scale InP selectively grown on SOI for fully integrated Si-photonics," *Appl. Phys. Lett.*, vol. 117, Aug. 2020, Art. no. 052102.
[28] Y. Han *et al.*, "InGaAs/InP quantum wires grown on silicon with adjustable emission wavelength at telecom bands," *Nanotechnology*, vol. 29, Mar. 2018, Art. no. 225601.
[29] J. E. Ayers *et al.*, *Heteroepitaxy of Semiconductors: Theory, Growth, and Characterization*. Boca Raton, FL, USA: CRC, Sep. 2016.
[30] F. Ratto and F. Rosei, "Order and disorder in the heteroepitaxy of semiconductor nanostructures," *Mater. Sci. Eng: R: Rep.*, vol. 70, no. 3-6, pp. 243–264, Nov. 2010.
[31] P. Pirouz, F. Ernst, and T. T. Cheng, "Heteroepitaxy on (001) silicon: Growth mechanisms and defect formation," *MRS Online Proc. Library*, vol. 116, pp. 57–70, 1988.
[32] B. Shi *et al.*, "MOCVD grown low dislocation density gaas-on-V-groove patterned (001) si for 1.3 μm quantum dot laser applications," *Appl. Phys. Lett.*, vol. 114, Apr. 2019, Art. no. 172102.

Jie Li received the B.S. degree from the University of Electronic Science and Technology of China, Chengdu, China, in 2019. She is currently working toward the Ph.D. degree with the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong. Her research focuses on III-V selective epitaxy on silicon by metal-organic chemical vapor deposition.

Ying Xue received the B.S. degree from Shandong University, Jinan, China, in 2017, and the Ph.D. degree from the Hong Kong University of Science and Technology, Hong Kong, in 2022. She is currently a Postdoctoral Research Associate with the Hong Kong University of Science and Technology. Her research focuses on the integration of III-V optoelectronic devices with silicon photonics.

Liying Lin received the B.S. degree from Fudan University, Shanghai, China, in 2018. She is currently working toward the Ph.D. degree with the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong. Her research focuses on III-V lasers on silicon in silicon photonics.

Zengshan Xing received the B.S. degree in physics from Hainan Normal University, Hainan, China, and the master's degree in optical engineering from Jinan University, Guangdong, China. He is currently working toward the Ph.D. degree with the Hong Kong University of Science and Technology, Hong Kong. His research focuses on photo-physics in organic- and inorganic materials.

Kam Sing Wong received the B.S. degree from the King's College, University of London, London U.K., in 1983, and the Ph.D. degree from the Clarendon Laboratory, University of Oxford, Oxford, U.K. in 1987. He is currently a Professor with the Physics Department, Hong Kong University of Science and Technology, Hong Kong. His research interests include ultrafast laser spectroscopy, nonlinear optical properties of semiconductors and polymers, fabrication and applications of photonic crystals and plasmonic nanostructures, and photo-physics of organic and inorganic materials.

Kei May Lau (Fellow, IEEE) received the B.S. and M.S. degrees in physics from the University of Minnesota, Minneapolis, MN, USA, and the Ph.D. degree in electrical engineering from Rice University, Houston, TV, USA. She is currently a Chair Professor of electronic and computer engineering with the Hong Kong University of Science and Technology (HKUST). Before joining HKUST in 2000, she was with the ECE Faculty, University of Massachusetts/Amherst, Amherst, MA, USA. Her research focuses on the development of monolithic integration of semiconductor devices on industry-standard silicon substrates. Lau is a Fellow of the OSA and Hong Kong Academy of Engineering Sciences. She is also the recipient of the IET J J Thomson medal for Electronics, OSA Nick Holonyak Jr. Award, IEEE Photonics Society Aron Kressel Award, US National Science Foundation (NSF) Faculty Awards for Women (FAW) Scientists and Engineers, and Hong Kong Croucher Senior Research Fellowship. She was the Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES and *Electron Device Letters*, an Associate Editor for the *Journal of Crystal Growth* and *Applied Physics Letters*.