

Effects of p-GaN Body Doping Concentration on the ON-State Performance of Vertical GaN Trench MOSFETs

Renqiang Zhu[®], *Graduate Student Member, IEEE*, Huaxing Jiang[®], *Member, IEEE*, Chak Wah Tang[®], and Kei May Lau[®], *Life Fellow, IEEE*

Abstract—In this letter, we report the influence of p-GaN body doping concentration on the ON-state performance of vertical GaN trench MOSFETs. Decreasing the p-GaN body doping concentration leads to an enhanced maximum drain current ($I_{D,max}$), reduced specific ON-resistance ($R_{ON,sp}$), but also a decreased threshold voltage (V_{th}), suggesting that the p-GaN doping plays an important role in balancing the V_{th} , $R_{ON,sp}$ and $I_{D,max}$ in vertical GaN trench MOSFETs. Resulting from the tuning of Mg concentration in the p-GaN, we demonstrate high ON-performance including a high $I_{D,max}$ of 2.8 kA/cm², a low $R_{ON,sp}$ of 0.87 m $\Omega \cdot cm^2$, a large V_{th} of 4.8 V in a quasi-vertical GaN trench MOSFET on sapphire with a 2.5- μ m-thick drift layer, while maintaining a breakdown voltage of 273 V.

Index Terms—Gallium nitride, vertical trench MOSFET, channel doping, ON-state performance.

I. INTRODUCTION

LGAN/GAN based lateral GaN power transistors have demonstrated great promise for low and medium voltage (≤ 650 V) power switching applications over the past decade [1]–[5]. To enhance the voltage rating and current handling capability of GaN transistors, device structures with vertical current conduction path have attracted extensive research interest [6]–[20]. Current aperture vertical electron transistors (CAVETs) [14], [16], [17], vertical fin MOSFETs [19], [20], and inversion channel vertical trench MOSFETs [6], [7] with a high breakdown voltage over 1 kV have been achieved. On the other hand, low ON-resistance ($R_{\rm ON}$) to minimize the power loss, high output current ($I_{\rm ON}$) to maximize the driving capability, and large threshold voltage ($V_{\rm th}$) (>3 V) to avoid false turn-on are always highly desired device metrics in these devices.

However, among the above mentioned three types of vertical GaN transistors, the CAVETs and vertical FinFETs were mainly operated in accumulation-mode, usually resulting in a small V_{th} (typically ~1-2 V). Their fabrication processes were also relatively complicated (channel regrowth or precise dry etch required), which may slow down their pace for wide

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The authors are with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong (e-mail: hjiangab@connect.ust.hk; eekmlau@ust.hk).

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adoption in manufacturing. As for the vertical GaN trench MOSFETs, despite the remarkable progress made in recent years [6]–[12], the ON-state performance including the R_{ON} and $I_{D,max}$ are not on par with the CAVET [12]–[17] and their vertical fin MOSFET [18]–[20] counterparts, mainly because of the large channel resistance of the inversion channel layer in the trench MOSFETs. To take advantage of the simple device fabrication process and resulting large V_{th} of GaN trench MOSFETs, lowering the channel resistance-dominated R_{ON} is essential to minimize the total power loss of the device. Although the ON-state performance of vertical trench MOSFETs was improved by optimizing the gate trench formation process [11], [21]–[23], the impact of material parameters, especially the body doping, of the device epilayers, has seldom been reported.

In this work, we investigated the effects of p-GaN body doping concentration on the ON-state performance of vertical GaN trench MOSFETs. We found that decreased p-GaN body doping concentration results in enhanced $I_{D,max}$, reduced $R_{ON,sp}$, but a lower V_{th} . Resulting from the fine tuning of the Mg doping concentration in the channel layer, a high ON-performance quasi-vertical GaN trench MOSFET is demonstrated, exhibiting not only a large V_{th} of 4.8 V, but also an ultralow specific on-resistance ($R_{ON,sp}$) of 0.87 m $\Omega \cdot cm^2$ in conjunction with a high $I_{D,max}$ of 2.8 kA/cm².

II. DEVICE DESIGN AND FABRICATION

The n⁺-p-n⁻-n⁺-GaN structures for the quasi-vertical trench MOSFETs were grown on sapphire substrates by MOCVD (Fig. 1). The epilayers, from bottom to top, consist of a 1- μ m i-GaN buffer, a 1- μ m n⁺-GaN [Si: 5 × 10¹⁸ cm⁻³], a 2.5- μ m n⁻-GaN drift layer [Si: 5 × 10¹⁶ cm⁻³], a 400-nm p-GaN body (Mg-doped), and a 200-nm n⁺-GaN layer [Si: 5 × 10¹⁸ cm⁻³]. Five samples (denoted as sample A, B, C, D, and E) were grown with the same structure and growth conditions except for the Mg doping concentration in the p-GaN body. The Mg concentration was varied from 3.0 to 1.2 ×10¹⁹ cm⁻³, as confirmed by secondary-ion mass spectrometry (SIMS) depth-profiling measurements (Fig. 1(b)).

All the samples shared the same fabrication procedures. The device process started with Cl₂/BCl₃-based dry etching of the gate trench (~900 nm-deep) with a Ni hard mask, followed by hot tetramethylammonium hydroxide (TMAH) wet etching to remove the dry etching induced damage in the gate trenches [21], [24]. The gate trench sidewalls were aligned to the *m*-plane for better ON-state performance [11], [22]. Process continued with the mesa formation and exposure of bottom n^+ -GaN layer for drain Ohmic contacts. After the

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Fig. 1. (a) 3-D cross-sectional schematic of fabricated quasi-vertical GaN trench MOSFETs. (b) Secondary ion mass spectrometry (SIMS) depth-profiling results of Mg concentration in the p-GaN layer of different samples. (c) Cross-sectional SEM images of the gate trench region of a fabricated device.



Fig. 2. (a) Transfer and (b) output curves of sample E.

p-GaN body contact was opened, the buried p-GaN body was then activated via rapid thermal annealing at 800°C for 10 min in an N₂ ambient. Subsequently, a 50-nm Al₂O₃ gate dielectric was deposited by atomic layer deposition (ALD). After removing the gate oxide in the body, source/drain contact regions, the p-body contact with a Ni/Au metal stack was deposited and annealed, followed by the Ti/Al/Ni/Au metal stack for the source and drain Ohmic contact. Finally, a Ti/Al metal stack was sputtered as the gate contact. It was noted that the p-GaN body contact is non-ideal Ohmic contact with a turn-on voltage of around 3 V, due to the dry-etching induced damage to the p-GaN surface [25], [26].

Fig. 1(c) shows the cross-sectional SEM images of the gate region in a fabricated device. Near 90-degree vertical sidewalls of the gate trench can be observed, which has been reported vital for the carrier transport [11]. The devices reported here feature a rectangular gate trench with a 4 μ m×100 μ m area. The active area (*A*) of the device for specific ON-resistance and current density normalization is regarded as (4 μ m trench length +2.5 μ m drift region thickness) × (100 μ m trench width +2.5 μ m drift region thickness) = 666.25 μ m², taking the lateral current spreading length (2.5 μ m) in the drift region into account [10]–[13].

III. DEVICE RESULTS AND DISCUSSION

Fig. 2 plots the transfer and output characteristics of a device on sample E (lowest Mg concentration among the five samples) that shows the best overall ON-state performance with the lowest $R_{ON,SP}$, the highest $I_{D,max}$, and a large V_{th} .

TABLE I

SUMMARY OF Mg CONCENTRATION OF P-GaN FROM SIMS AND CORRESPONDING ON-STATE DEVICE PARAMETERS (AVERAGE VALUE MEASURED FROM TEN DEVICES ON EACH SAMPLE) FOR DIFFERENT SAMPLES

Sample	А	В	С	D	Е
Mg concentration of p-GaN (10 ¹⁹ cm ⁻³)	3.0	2.6	2.3	1.8	1.2
$V_{\rm th}$ (V) @1 A/cm ²	7.75	7.53	7.05	5.21	4.70
$I_{\rm D,max}$ (A/cm ²)	400	635	713	1261	2605
$R_{ m ON,sp}({ m m}\Omega{ m \cdot}{ m cm}^2)$	4.83	2.95	2.39	1.66	0.89
$V_{\rm th}$ hysteresis (V)	1.33	1.36	1.28	1.30	1.26
$\Delta V_{ m th} / \Delta V_{ m DS} ({ m mV/V})$	93	91	98	107	105



Fig. 3. (a) $I_{\rm D} - V_{\rm GS}$ (at $V_{\rm DS} = 1$ V) and (b) $I_{\rm D} - V_{\rm DS}$ (at $V_{\rm GS} = 15$ V) curves of the five samples with different Mg concentrations of p-GaN.



Fig. 4. $R_{ON,sp}$ breakdown of devices on the five samples with varied Mg concentration in p-GaN body. The percentages of $R_{ch,sp}$ to total $R_{ON,sp}$ on five samples are labeled.

At $V_{\rm DS} = 1$ V, an ultrahigh ON/OFF current ratio of $\sim 5 \times 10^{10}$, a large $V_{\rm th}$ of 4.8 V at $I_{\rm D}$ of 1 A/cm²(7.4 V from linear extrapolation), a reasonable subthreshold slope of 280 mV/dec, and a low gate current of 1.7×10^{-3} A/cm² at $V_{\rm GS}$ of 15 V are achieved in the device (Fig. 2(a)). The gate leakage can be further reduced by optimizing the dry etching and gate dielectric deposition conditions. In addition, a high $I_{\rm D,max}$ of 2.8 kA/cm² and a low $R_{\rm ON,sp}$ of 0.87 m $\Omega \cdot \rm cm^2$ are also demonstrated (Fig. 2(b)). The $V_{\rm th}$ measured at $V_{\rm DS} = 10$ V is negatively shifted to 3.9 V at $I_{\rm D}$ of 1 A/cm², resulting in a drain-bias-induced $V_{\rm th}$ shift ($\Delta V_{\rm th}/\Delta V_{\rm DS}$) of ~ 100 mV/V. The reason behind the drain-bias-induced $V_{\rm th}$ shift is under investigation.

Fig. 3 compares the representative $I_{\rm D}$ - $V_{\rm GS}$ (at $V_{\rm DS} = 1$ V) and $I_{\rm D}$ - $V_{\rm DS}$ (at $V_{\rm GS} = 15$ V) curves of the five samples, with key device parameters ($V_{\rm th}$, $I_{\rm D,max}$, $R_{\rm ON,sp}$, $V_{\rm th}$ hysteresis from $I_{\rm D}$ - $V_{\rm GS}$ double sweep, and drain-bias-induced $V_{\rm th}$ shift ($\Delta V_{\rm th}/\Delta V_{\rm DS}$)) summarized in TABLE I. From sample A to E, the average $R_{\rm ON,sp}$ decreases from 4.83 to 0.89 m Ω -cm², corresponding to the dramatic increase of the $I_{\rm D,max}$ from 400 to 2605 A/cm². Fig. 4 shows the contributions of the total $R_{\rm ON,sp}$ of the five samples, consisting of contact resistance ($R_{\rm contact,sp}$,



Fig. 5. Comparison of inversion channel mobility of devices on the five samples with varied Mg concentrations in p-GaN body.

including S/D contact layers and Ohmic contacts resistance), drift layer resistance ($R_{drift,sp}$) and channel resistance ($R_{ch,sp}$). The $R_{contacts,sp}$ is calculated based on the transmission line measurement (TLM) of the top and bottom n⁺-GaN layers on each sample. The $R_{drift,sp}$ is estimated based on Schottky diodes with the same drift layer. The $R_{ch,sp}$ is calculated by $R_{ch,sp} = R_{ON,sp} - R_{drift,sp} - R_{contact,sp}$. Since the five samples show nearly identical $R_{drift,sp} (\sim 0.16 \text{ m}\Omega \cdot \text{cm}^2)$ and $R_{contact,sp}$ ($\sim 0.18 \text{ m}\Omega \cdot \text{cm}^2$), the drastic drop in $R_{ON,sp}$ mainly resulted from the reduction of the $R_{ch,sp}$ with the decrease of Mg concentration in the p-GaN body can be inferred.

To further correlate the ON-state channel resistance with the body doping concentration, the electron mobility (μ_{ch}) of the inversion channel of each sample is extracted by fitting the equation [27]:

$$I_{\rm D} = \frac{V_{\rm DS}}{\frac{A}{\frac{W}{L}u_{\rm ch}C_{\rm ox}(V_{\rm GS} - V_{\rm th})} + R_{\rm drift,sp} + R_{\rm contact,sp}}, (V_{\rm GS} > V_{\rm th})}$$
(1)

with measured $I_{\rm D}$ - $V_{\rm GS}$ curves (Fig. 5) at $V_{\rm DS}$ of 0.1 V, considering the series resistance from the drift and contact layers. In (1), A is the active area of 666.25 μ m², W is the gate width of 208 μ m, L is the gate length of 0.4 μ m, and $C_{\rm ox}$ is the gate oxide capacitance per unit area. We observe an increasing trend of inversion channel mobility with the decrease of Mg concentration, from 4.7 cm²/V-s for sample A to 25.2 cm²/V-s for sample E. With a lower Mg concentration in the p-GaN body, the impurity scattering is reduced for the electrons in the inversion channel thus increasing the carrier mobility [28].

On the other hand, from sample A to E, the average $V_{\rm th}$ (defined at $I_{\rm D}$ of 1 A/cm²) decreases from 7.75 V to 4.70 V, following the decrease of acceptor concentration in the body as expected. Therefore, the reduction of $R_{\rm ON,sp}$ at the same maximum gate bias ($V_{\rm GS}$ =15 V) from sample A to E is a combined result of the enhanced inverted channel mobility together with the increased electron carrier concentration (due to higher overdrive gate voltage ($V_{\rm GS}$ - $V_{\rm th}$)). Nevertheless, further reduction of the Mg concentration may lead to too low a $V_{\rm th}$ that may undermine the device immunity to noise signals. Our work suggests that the body doping concentration of the p-GaN layer in the vertical trench MOSFETs is a key parameter to make tradeoffs among the $V_{\rm th}$, $R_{\rm ON,sp}$ and $I_{\rm D,max}$ in the device.

All five samples show a similar $V_{\rm th}$ hysteresis ($\Delta V_{\rm th}$) of ~1.3 V, corresponding to an interface trap density ($N_{\rm it} = \Delta V_{\rm th} \times C_{\rm ox}/q$) of ~ 1 × 10¹² cm⁻². The drain-bias-induced $V_{\rm th}$ shift ($\Delta V_{\rm th}/\Delta V_{\rm DS}$) of five samples



Fig. 6. Experimental V_{th} and calculated V_{th} with/without interface charge as a function of N_{A} .

ranges from ~ 90 to ~ 110 mV/V, as shown in TABLE I. To further investigate the gate stack properties, we have compared the measured $V_{\rm th}$ with theoretically predicted ones. The $V_{\rm th}$ can be calculated using the traditional $V_{\rm th}$ equation for MOSFET in the textbook [27]. Since the effective acceptor concentration (N_A) in p-GaN is different from the Mg doping concentration depending on the activation efficiency, we have extracted the $N_{\rm A}$ from test structures based on the body bias effect [27], [29], which is $3.6 \times$, $3.1 \times$, $2.8 \times$, $2.2 \times$, and $1.6 \times$ 10^{18} cm⁻³ for sample A to E, respectively. It can be observed that the experimental $V_{\rm th}$ value for each sample is far lower than the theoretical value assuming no interfacial charges $(Q_{\rm it})$, as shown in Fig. 6. The results suggest the existence of high-density positive interface charges in the gate stack, which may originate from residual impurities and/or dryetching-induced N-vacancies on the p-GaN sidewall [25], [26]. Accordingly, the interface charge density ($\sigma = Q_{it}/q$) for sample A to E is estimated to be $5.1 \times$, $4.6 \times$, $4.5 \times$, $4.6 \times$, and 3.7×10^{12} cm⁻², respectively.

For the OFF-state performance, a small breakdown voltage $(V_{\rm BR})$ of 60 V was initially observed in all the devices, due to an early dielectric failure at the gate-to-drain MOS junction. By employing a thick bottom dielectric in the gate trench to suppress the electric field [30], [31] without sacrificing the ON-state performance, the $V_{\rm BR}$ of the vertical MOSFET has been enhanced from 60 V to 273 V, close to the $V_{\rm BR}$ of the p-n junction of 285 V on the same epi-wafer. Details of the breakdown voltage enhancement will be reported elsewhere.

IV. CONCLUSION

This work reports a strong impact of p-GaN doping concentration on $R_{ON,sp}$, $I_{D,max}$, and V_{th} of vertical GaN trench MOSFETs. In a series of comparative experiments, we found that decreasing the p-GaN body doping concentration leads to an enhanced $I_{D,max}$, a lowered $R_{ON,sp}$, but also a reduced V_{th} . The p-GaN doping might be the most sensitive variable in balancing the key ON-state parameters ($R_{ON,sp}$, $I_{D,max}$, and V_{th}) in vertical GaN trench MOSFETs. From the fine tuning of Mg concentration in the p-GaN, high ON-state performance including a low $R_{ON,sp}$, a high $I_{D,max}$, a large V_{th} has been demonstrated in the quasi-vertical GaN trench MOSFET with a 2.5- μ m thick drift layer maintaining a reasonable V_{BR} .

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