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Thin-barrier heterostructures enabled normally-OFF GaN high electron mobility transistors

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Abstract

In this paper, we present our recent research on the demonstration of normally-OFF operation and high-performance device merits in GaN high electron mobility transistors (HEMTs), which are enabled by the employment of thin-barrier AlGaN/GaN heterostructures. Two types of thin-barrier HEMTs are investigated: one is with a metal–oxide–semiconductor (MOS) gate structure, and the other is with a p-GaN gate stack. The MOSHEMTs feature an as-grown thin-barrier heterostructure with a gate-recess-free fabrication process and a high-k ZrO_2 gate dielectric. Approaches including selective area barrier regrowth and selective area surface passivation are implemented to minimize the access resistance in the MOSHEMTs. For the p-GaN gate HEMTs, a T-shaped Schottky gate contact scheme is employed to realize superior gate stack reliability. Normally-OFF operation with a large threshold voltage $\geqslant$1.5 V, a high maximum drain current $\geqslant$450 mA mm^{-1}, a steep subthreshold slope $\leqslant$95 mV dec^{-1}, and negligible hysteresis are achieved in all the demonstrated device structures. Moreover, in analyzing the reported device results with the corresponding heterostructure design, we discuss the benefits and tradeoffs of thin-barrier MOSHEMTs and p-GaN gate HEMTs, respectively.

Keywords: thin barrier, normally-OFF, GaN high electron mobility transistor, p-GaN gate, high-k dielectrics, passivation

(Some figures may appear in color only in the online journal)

1. Introduction

Semiconductor power switches with a minimal ON-state power loss in conjunction with a strong OFF-state blocking capability are always desired in power electronic systems. Benefiting from the high electron density and mobility of 2D electron gas (2DEG) formed channel leading to a low ON-resistance (R_{ON}), and the large critical electric field in GaN material properties thereby a high OFF-state breakdown voltage (V_{BR}), AlGaN/GaN-based heterojunction field effect transistors have demonstrated great promise for energy-efficient power switching applications [1, 2]. However, the normally-ON characteristic resulting from the pre-existing 2DEG channel in conventional AlGaN/GaN high electron mobility transistors (HEMTs), typically with a ~20 nm AlGaN barrier thickness and a ~20% – 30% Al mole fraction, slowed down the pace towards rapid adoption of these devices in power systems [3]. In high-voltage high-current application scenarios, power switches with normally-OFF property are highly demanded to ensure fail-safe operation, in addition to simplifying the circuit design with a single-polarity power supply. As such, extensive research efforts have been devoted to achieve high-performance normally-OFF GaN HEMTs over the past two decades. For instance, Ikeda *et al* demonstrated the first normally-OFF GaN HEMTs on silicon substrates using a C-doped GaN channel [4], Saito *et al* and Oka *et al* achieved normally-OFF operation using a recessed gate structure [5, 6], Kanamura *et al* employed

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a n-GaN/i-GaN/n-GaN triple cap layer to obtain a positive V_{th} [7], and Medjdoub *et al* demonstrated a normally-OFF AlN/GaN HEMT with a low R_{ON} [8]. Alternatively, Cai *et al* demonstrated a normally-OFF HEMT with fluoride plasma treatment [9]. In the past decade, extensive attention has been paid to the metal–insulator–semiconductor structure with fully removed AlGaN barrier [10, 11] or ultrathin barrier [12]. Recently, some novel tri-gate structures have also been developed to achieve normally-OFF operation [13, 14]. Other approaches such as Schottky-contact p-GaN gate HEMTs and gate injection transistors were also demonstrated with large threshold voltages [15, 16].

The basic guideline to realize normally-OFF operation in AlGaN/GaN HEMTs is to prevent the 2DEG formation underneath the gate region no matter when the gate is floating or biased at 0 V. Several approaches were explored to deplete the 2DEG underneath the gate, including introducing negative charges (e.g. fluorine ions) [17, 18], employing p-(Al)GaN cap layer to form a p–n junction [16, 19, 20], or simply reducing the AlGaN barrier thickness (by gate recess or epitaxy) since the 2DEG density strongly depends on the thickness and Al composition of the AlGaN layer [5, 21–23]. However, thermal stability remains an unresolved issue to date in the first method. While, for the latter two approaches, the ultrathin AlGaN barrier needed to achieve a positive V_{th} can lead to device fabrication a liability. Moreover, the V_{th} of the device needs to be large enough to avoid false turn-on triggered by noise gate signals.

Early works on thin-barrier normally-OFF HEMTs deployed a Schottky gate (SG) contact, which had a very limited maximum gate bias (<3 V) [5, 24]. Later on, with the improvement of high-quality dielectric deposition techniques on GaN, metal–insulator (oxide)–semiconductor HEMT (MISHEMT/MOSHEMT) structures were applied in the thin-barrier normally-OFF devices to reduce the gate leakage current and increase the gate swing. In recent years, high-performance normally-OFF GaN MOSHEMTs with a low R_{ON} and high maximum drain current ($I_{DS,\,max}$) have been demonstrated employing a thin-barrier structure [12, 25, 26]. However, due to the insertion of a thick gate dielectric (SiO_2, SiN_x, or Al_2O_3) with a relatively low dielectric constant between the gate metal and thin barrier, the effectiveness of using a thin-barrier structure to suppress the 2DEG formation is undermined. Consequently, the reported V_{th} in the device is only slightly larger than 0 V or even a small negative value, leading to a quasi-normally-OFF device. Alternatively, the utilization of insulated gate structure allows thinning the barrier to its minimum thickness, i.e. complete removal of the barrier layer, resulting in a direct contact of gate dielectric and i-GaN channel layer thus forming a MOSFET structure [27, 28]. In this way, a relatively large V_{th} may be achieved. However, due to the strong scattering effect, the electron mobility in the i-GaN channel is much less than that in the 2DEG channel with a preserved heterojunction. Hence, the large V_{th} in devices with an i-GaN channel is usually at the cost of a compromised R_{ON}. Therefore, in this work, for the insulated gate HEMT structure, we mainly discuss about the development of MOSHEMTs with a functional thin-barrier layer to ensure high performance in the ON-state.

Up to now, p-GaN gate HEMTs with good V_{th} stability are the only type of truly normally-OFF GaN HEMTs being commercialized among all the aforementioned approaches. In p-GaN gate HEMTs, an AlGaN/GaN heterostructure with a relatively thin barrier is vital to ensure a positive V_{th}. Precise removal of the topmost p-GaN layer in the access regions poses a significant challenge since a slight overetch will lead to a significant increase in the access resistance thereby a high R_{ON}. Although the V_{th} of the p-GaN gate HEMTs can also be adjusted by the work function of gate metals [15, 29], the R_{ON} and $I_{DS,\,max}$ are also affected by the gate stack design. To achieve both a large V_{th} and a low R_{ON} in p-GaN gate HEMTs, a recess-and-regrowth method was proposed and high-performance devices were demonstrated [30]. However, the regrowth process increased the p-GaN gate HEMTs fabrication complexity and the device results strongly depended on the process conditions [31]. Over the past decade, great efforts have been devoted to minimizing the R_{ON} in p-GaN gate HEMTs while maintaining a large V_{th}. The gate reliability associated with the p-GaN cap and thin barrier in the device have also attracted extensive research interests.

In the work, we present our recent research results on the development of normally-OFF GaN HEMTs employing thin-barrier heterostructures, aiming at achieving a large V_{th} as well as a high $I_{DS,\,max}$ and a low R_{ON}. In addition, minimal hysteresis and high V_{BR} are also important device merits in the target. Based on the gate stack structure, our strategies to achieve normally-OFF operation in the thin-barrier devices can be divided into two categories as mentioned above: (a) MOSHEMTs and (b) p-GaN gate HEMTs. For the MOSHEMTs, a recess-free barrier process was developed to ensure low trapping effect in the gate stack and a small resistance in the access regions. A high-*k* ZrO_2 gate dielectric was employed to suppress the gate leakage without sacrificing the gate control over the channel to achieve a large V_{th}. For the p-GaN gate HEMTs, a T-shaped gate structure with reduced metal/p-GaN contact area was implemented with a properly designed barrier structure, achieving both a large V_{th} and a high $I_{DS,\,max}$, as well as a retained high-voltage blocking capability even after forward gate breakdown.

This paper is organized as follows. In section 2 we introduce the development of normally-OFF GaN MOSHEMTs with a recess-free barrier process and high-*k* ZrO_2 gate dielectric. Two different approaches to reduce the access resistance in the thin-barrier MOSHEMTs are presented. Section 3 describes the development of high-performance p-GaN gate HEMTs. The gate stack reliability of the device is characterized and analyzed. Benchmarking of MOSHEMTs and p-GaN gate HEMTs in this work with reported state-of-the-art devices with thin-barrier heterostructures is discussed in section 4. Finally, a brief summary will be given in section 5.

2. GaN MOSHEMTs with engineered thin-barrier and high-*k* ZrO_2 gate dielectric

In comparison with the GaN MOSFETs which have a fully recessed barrier underneath the gate, a preserved thin barrier in the MOSHEMT structure maintains full benefits of the 2DEG

with reduced Coulomb scattering and surface roughness scattering for the electron carriers at the heterointerface. On the other hand, to reduce the density of interface trap states in the gate stack, we chose the bottom-up method to form the thin barrier in the AlGaN/GaN heterostructure by epitaxy in the initial device design, instead of using the conventional top-down gate recess approach in which dry/wet-etching process steps inevitably cause damages to the barrier surface thus gate controllability issues.

As mentioned earlier, stacking insulators with a relatively low dielectric constant on top of the thin-barrier heterostructures to realize GaN MOSHEMTs commonly results in a small V_{th} in the device. To achieve a large positive V_{th}, we employed high-k ZrO_2 as the gate dielectric for better gate control [32]. The ZrO_2 was formed by atomic layer deposition and the deposition conditions were fine tuned to achieve a good uniformity of film thickness and an ultrahigh dielectric constant of 29. Therefore, even though a thick ZrO_2 was introduced to reduce the gate leakage current of the MOSHEMT, the negative shift of V_{th} induced by the gate dielectric is rather small, which is less than 1 V when comparing the SG HEMT and ZrO_2-insulated MOSHEMTs with the same AlGaN/GaN heterostructure.

2.1. Ultrathin-barrier GaN MOSHEMTs with selective area barrier regrowth

Utilizing an ultrathin-barrier heterostructure and selective area barrier regrowth, we have successfully demonstrated a GaN MOSHEMT with normally-OFF operation [33]. Figure 1(a) shows the cross-sectional schematic of the fabricated device. The epilayers were grown on a 6 inch n-type Si (111) substrate by metal-organic chemical vapor deposition, from bottom to top, consisting of a 1.2 μm step-graded AlGaN buffer, a 2.5 μm C-doped high-resistivity GaN buffer, a 0.5 μm unintentionally doped GaN channel layer, a 1 nm AlN spacer, and a 6 nm $Al_{0.2}GaN$ barrier. The topmost AlGaN/GaN heterostructure features an ultrathin AlGaN barrier of 6 nm and a low Al mole fraction of 20%. Such a thin barrier and low Al composition can hardly induce 2DEG at the heterointerface. Nearly no 2DEG formation in the heterostructure is in favor of normally-OFF operation for the gate stack, which, however, gives rise to large resistivity in the access regions thereby a large R_{ON}. To address this issue, an additional barrier layer of 20 nm AlGaN with 30% Al mole fraction was selectively grown outside the gate region. A thick SiN passivation by plasma-enhanced chemical vapor deposition (PECVD) was employed to further enhance the 2DEG concentration in the access regions. A 23 nm high-k ZrO_2 was deposited as the gate dielectric. More detailed description on the device fabrication process can be found in our previous report [33]. Figure 1(b) depicts the cross-sectional transmission electron microscopy (TEM) image taken near the ZrO_2/AlGaN interface of the gate stack. An atomically abrupt interface between the ZrO_2 and the $Al_{0.2}GaN$ barrier can be observed. To further evaluate the impact of AlGaN barrier structure on the 2DEG concentration/conductivity at the AlGaN/GaN heterointerface, current–voltage (I–V) measurements were performed on two ohmic pads 16 μm apart for both the as-grown heterostructure with a 6 nm AlGaN barrier and the heterostructure with an additional 20 nm regrown AlGaN barrier. The results are compared in figure 2. The current measured on the as-grown heterostructure is as low as ~5 nA mm^{-1}, while the value on the stacked $Al_{0.3}GaN/Al_{0.2}GaN/GaN$ heterostructure increased by approximately eight orders of magnitude to 650 mA mm^{-1}, suggesting high-density 2DEG formed at the AlGaN/GaN heterointerface in the access regions with the additional regrown barrier.

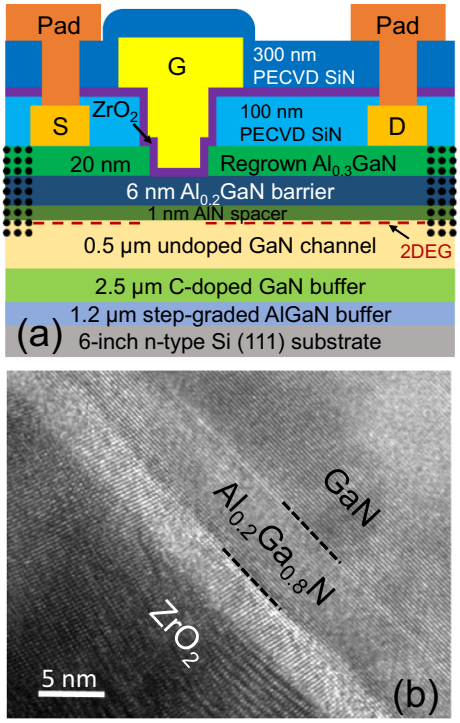

Figure 1. (a) Cross-sectional schematic of the fabricated GaN MOSHEMTs with an ultrathin AlGaN barrier underneath the gate and selective area barrier regrowth in the access regions. (b) Cross-sectional TEM image taken near the $ZrO_2/Al_{0.2}GaN$ interface of the gate stack. Copyright 2018 IEEE. Reprinted with permission from [33].

Figure 3 shows the representative transfer and output characteristics of the GaN MOSHEMTs with a gate length (L_G) of 1.5 μm, a gate–drain distance (L_{GD}) of 3 μm, a gate–source distance (L_{GS}) of 3 μm, and a gate width (W_G) of 10 μm. The device exhibits a large V_{th} of 2.3 V defined at I_D of 0.1 mA mm^{-1} or 3 V by linear extrapolation. In addition, a high ON/OFF current ratio of ~10^9 and a steep subthreshold slope (SS) of 95 mV dec^{-1} are also achieved in the device. The double-sweep I_D–V_G measurement reveals a negligible V_{th} hysteresis, suggesting a high-quality gate stack with little trapping effect at the ZrO_2/AlGaN interface and inside the ZrO_2, which is attributed to the recess-free process with minimized damage to the ultrathin AlGaN barrier surface. As a result of the efficient gate modulation facilitated by the high-k ZrO_2 gate dielectric and greatly enhanced 2DEG concentration in the access regions, the MOSHEMT exhibits a high $I_{DS,\,max}$ of 590 mA mm^{-1} at a V_{GS} bias of 8 V with a low accompanied R_{ON} of 9.2 Ω mm.

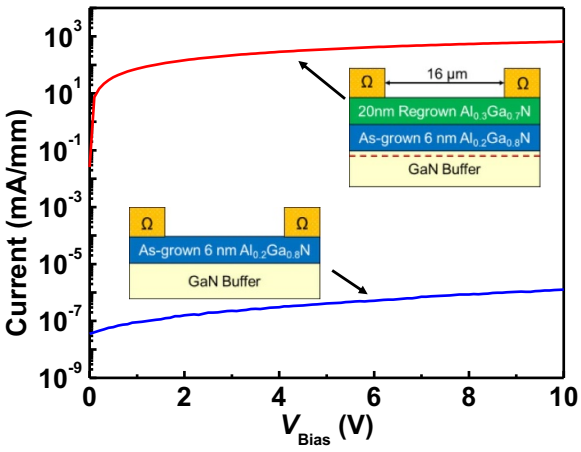

Figure 2. Comparison of currents measured between two ohmic pads with a 16 μm distance on the as-grown heterostructure and the one with an additional 20 nm regrown barrier.

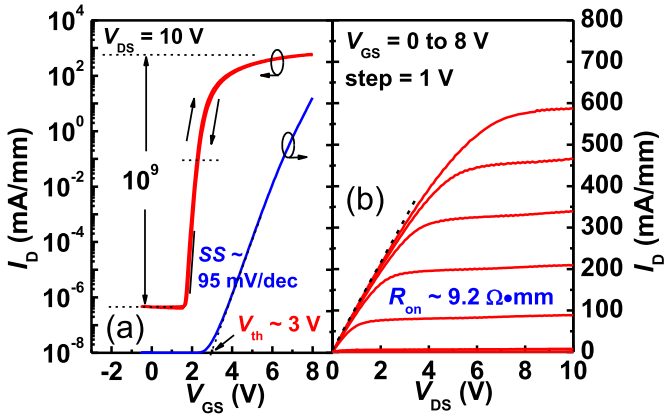

Figure 3. (a) Transfer (I_D–V_{GS} in semi-log and linear plots) and (b) output characteristics of the ultrathin-barrier GaN MOSHEMTs with dimensions of $L_G/W_G/L_{GS}/L_{GD}$ = 1.5/10/3/3 μm.

2.2. Thin-barrier GaN MOSHEMTs with selective area surface passivation

The selective area barrier regrowth approach to restore the 2DEG in the access regions for thin-barrier AlGaN/GaN heterostructures is effective yet somewhat complicated. The short growth time for tens of nanometer-thick regrown barrier presents some challenge to achieve a smooth regrown barrier surface. Alternatively, we developed another type of normally-OFF thin-barrier MOSHEMTs, in which no regrowth is needed and the 2DEG concentration in the access regions is enhanced by selective area passivation with a thick PECVD SiN_x.

Figure 4(a) shows the cross-sectional schematic of the fabricated thin-barrier GaN MOSHEMTs with selective area surface passivation. Compared with the heterostructure described in previous subsection, the epilayer structures are the same except that the AlGaN barrier in this design is slightly thicker (~10 nm), and the Al composition is also relatively higher (~30%). A thicker barrier with a higher Al mole fraction is

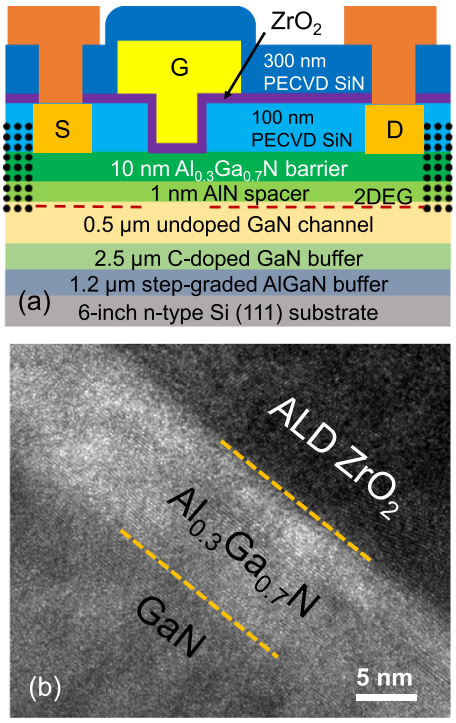

Figure 4. (a) Cross-sectional schematic of the fabricated thin-barrier GaN MOSHEMTs. (b) Cross-sectional TEM image of the $ZrO_2/Al_{0.3}GaN/GaN$ gate stack.

in favor of the 2DEG formation at the heterojunction. Nevertheless, the resulted 2DEG concentration is still relatively low (confirmed with I–V measurement), compared with the typical value (~0.8–1 $\times$ 10^{13} cm^{-3}) in conventional 20 nm-AlGaN/GaN heterostructures. The device also employed a 23 nm ALD ZrO_2 gate dielectric. Figure 4(b) shows the cross-sectional TEM image of the $ZrO_2/Al_{0.3}GaN/GaN$ gate stack, depicting a seamless contact between the gate dielectric and barrier layer with an atomically abrupt interface. Without additional barrier regrowth, the device fabrication process steps are greatly simplified, which are almost the same as those for conventional depletion-mode GaN MOSHEMTs [32, 34]. To maintain both normally-OFF operation in the gate stack and a low R_{ON}, the PECVD SiN passivation layer was selectively removed in the gate region via a combined low-power dry etching and a wet etching using buffered oxide etchant. In this way, 2DEG can be restored in the access region only and the channel underneath the gate remains depleted. The ohmic contact is formed with conventional alloyed Ti/Al/Ni/Au metal layers and the gate contact is a Ni/Au stack [35].

The transfer and output characteristics of the thin-barrier GaN MOSHEMTs with dimensions of $L_G/W_G/L_{GS}/L_{GD}$ = 1.5/10/3/3 μm are presented in figure 5. The device exhibits a large V_{th} of 1.5 V at I_D of 0.1 mA mm^{-1} and 2.4 V by linear extrapolation. The V_{th} of the thin-barrier MOSHEMTs is slightly smaller than that of the device described in previous subsection, due to the thicker AlGaN barrier and a higher Al composition. With effective suppression of the gate leakage current, a low OFF-state drain leakage

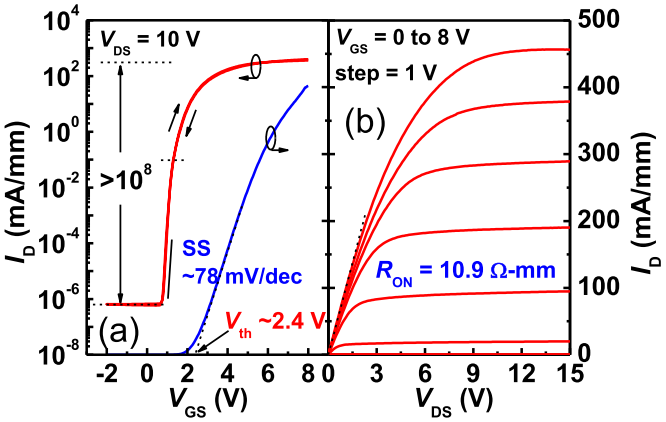

Figure 5. (a) Transfer (I_D–V_{GS} in semi-log and linear plots) and (b) output characteristics of the thin-barrier GaN MOSHEMTs with selective area passivation. Device dimensions: $L_G/W_G/L_{GS}/L_{GD}$ = 1.5/10/3/3 μm.

current below 10^{-6} mA mm^{-1} was achieved, leading to a high ON/OFF current ratio of over 10^8. The high-k gate dielectric enabled efficient gate modulation over the channel results in a steep SS of 78 mV dec^{-1}, which also suggests a low interface trap states density in the high-quality gate stack. The negligible V_{th} hysteresis in the double-swept transfer characteristics provides another evidence of a low trap states density in the gate stack. Although the GaN MOSHEMTs in this subsection have a larger gate-to-channel distance than that in previous subsection due to the larger barrier thickness, the smaller *SS* in the device suggests a better interface quality than that of the ultrathin-barrier GaN MOSHEMTs with selective area barrier regrowth. One possible reason is that the selective area barrier regrowth process requires the as-grown ultrathin AlGaN barrier to go through a high-temperature annealing process during the regrowth, which might modify the surface status and surface trap states could be introduced, weakening the gate controllability over the channel. On the other hand, although the initial 2DEG concentration is low in the as-grown 10 nm-$Al_{0.3}$GaN/GaN heterostructure, the density of electron carriers is significantly increased via the PECVD SiN passivation. As a result, the device exhibits a high $I_{DS,\,max}$ of 450 mA mm^{-1} and a low R_{ON} of 10.9 Ω mm. The recovery of 2DEG at the heterojunction by PECVD SiN passivation alone is not as effective as that with the regrown AlGaN barrier, which however is still sufficient to build up a normally-OFF GaN MOSHEMT as a proof of concept.

High-voltage OFF-state blocking capability is also demonstrated in the device. Figure 6 plots the three-terminal OFF-state leakage current versus the drain bias at V_{GS} of 0 V for the device with a 15 μm gate–drain distance. Benefitting from the effective leakage-blocking capability of the MOS gate stack, the device exhibits an ultralow drain leakage current (I_D) and gate leakage current of 2 nA mm^{-1} and 0.6 nA mm^{-1}, respectively, at V_{DS} of 200 V. Moreover, a high soft breakdown voltage of 920 V defined at I_D of 1 μA mm^{-1} is also achieved in the device, suggesting good management of peak electric field at the gate edge on the drain side employing a gate-connected field plate.

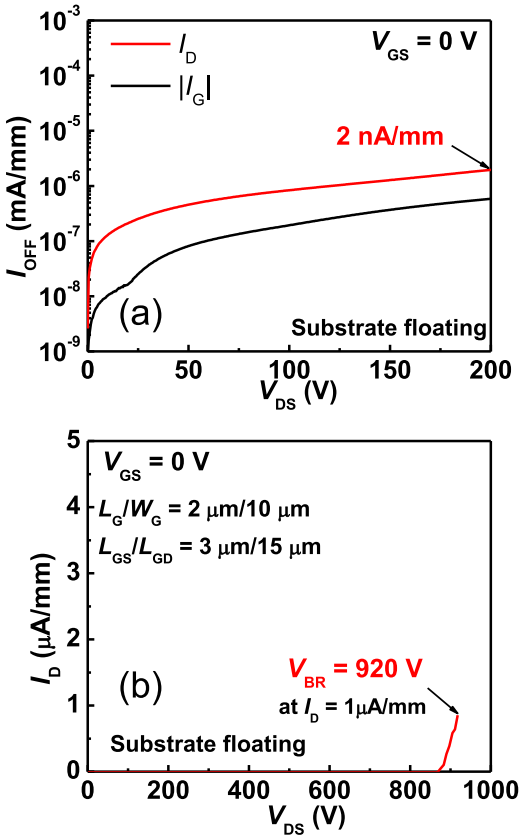

Figure 6. OFF-state leakage current versus drain bias of the thin-barrier MOSHEMTs (a) for V_{DS} within 200 V and (b) for V_{DS} up to 1000 V.

3. High-performance p-GaN gate HEMTs with reliable gate operation

Unlike the aforementioned GaN MOSHEMTs, which rely on the inherent resistivity of the thin-barrier heterostructure with no or low-concentration 2DEG formed to realize the normally-OFF operation, HEMTs with a p-GaN gate proactively deplete the 2DEG at the AlGaN/GaN heterointerface through the elevation of Fermi level by the p-GaN cap layer [20]. As such, there is one more degree of freedom to control the 2DEG concentration thereby the V_{th} in p-GaN gate HEMTs.

3.1. Schottky-contact p-GaN gate HEMTs with large V_{th} and high $I_{DS,\,max}$

Based on the type of gate metal and p-GaN contact, p-GaN gate HEMTs can have either a SG contact or an ohmic contact for the gate stack [36, 37]. When a p-GaN gate HEMT is under a forward gate bias, the p-GaN/AlGaN/GaN junction (p–i–n diode) is also forward biased. It is a common strategy to employ a reversely biased SG contact on p-GaN to suppress the gate leakage current in this type of devices.

We have fabricated p-GaN gate HEMTs with a Ni/Au SG contact [38]. The cross-sectional schematic of the fabricated devices is shown in figure 7(a). The AlGaN/GaN heterostructure features a 10 nm barrier layer with a 20% Al mole fraction. A 70 nm p-GaN cap layer with a Mg doping

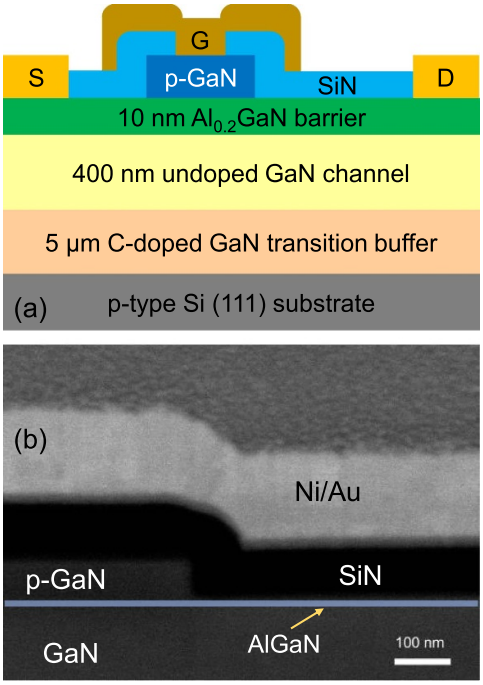

Figure 7. (a) Cross-sectional schematic of fabricated p-GaN gate HEMTs. (b) Cross-sectional SEM image of the gate stack near the p-GaN edge, with the thin AlGaN layer color-enhanced.

concentration of $\sim 5 \times 10^{19}$ cm^{-3} was adopted to fully deplete the 2DEG at the heterojunction. It should be noted that the 2DEG concentration is influenced by not only the thickness and Al composition of the AlGaN barrier, but also the thickness and hole concentration of the p-GaN cap layer. For the p-GaN gate HEMT fabrication process, the most critical step is the selective removal of p-GaN cap layer on top of the AlGaN barrier in the access regions, where either underetch or overetch is detrimental to the recovery of 2DEG thus the R_{ON}. We have developed a low-power plasma dry etching method to precisely remove the p-GaN layer and minimize the damage to the AlGaN barrier surface [38]. Additional PECVD SiN passivation is deployed to further enhance the 2DEG concentration. Figure 7(b) shows the cross-sectional scanning electron microscopy image of the gate stack near the p-GaN edge of fabricated p-GaN gate HEMTs, which shows a precise etch stop at the AlGaN barrier surface.

The transfer and output characteristics of p-GaN gate HEMTs with dimensions of $L_G/W_G/L_{GS}/L_{GD} = 4/10/3/3$ μm are presented in figure 8. A large V_{th} of 1.75 V defined at I_D of 0.1 mA mm^{-1} or 2.3 V by linear extrapolation is achieved in the device, accompanied by a high ON/OFF current ratio of over 10^8 and a nearly ideal SS of 68 mV dec^{-1}. Although the device employed a SG contact scheme, the hysteresis of the double-swept transfer curves is almost negligible, suggesting excellent interface quality of the Ni/p-GaN contact. Moreover, the device is capable to deliver a high $I_{DS,\,max}$ of 605 mA mm^{-1} at a large forward gate bias of 8 V, associated with a R_{ON} as low as 3.6 Ω mm. Such a high driving current and low ON-resistance are combined results of efficient gate modulation of the channel underneath the p-GaN and sufficient recovery of

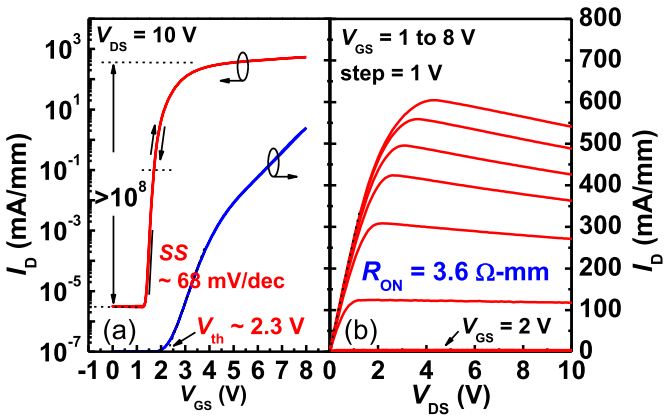

Figure 8. (a) Transfer (I_D–V_{GS} in semi-log and linear plots) and (b) output characteristics of the fabricated p-GaN gate HEMTs. Device dimensions of $L_G/W_G/L_{GS}/L_{GD} = 4/10/3/3$ μm.

2DEG in the access regions enabled by the low-damage precise p-GaN removal and effective SiN passivation.

The OFF-state leakage currents as a function of the drain bias for our p-GaN gate HEMTs with a gate–drain distance of 18.5 μm are plotted in figure 9. The OFF-state drain leakage current at V_{DS} of 200 V is about two orders higher than that of the aforementioned thin-barrier MOSHEMTs, due to a higher gate-to-drain leakage current and a drain-to-source leakage current, which may result from surface leakage current at the SiN/AlGaN interface via a 2D hopping conduction mechanism [39]. Nevertheless, the device still exhibits an ultrahigh three-terminal V_{BR} of 1600 V defined at I_D of 1 μA mm^{-1}, suggesting well managed electric fields in the device.

3.2. Schottky-contact p-GaN gate HEMTs with a stable gate operation

Since the gate metal/p-GaN Schottky junction is under reverse bias when a positive bias is applied to the gate, the forward gate leakage current and breakdown voltage is thus in principle determined by the reverse leakage current and breakdown voltage of the Schottky junction, respectively. In many reported p-GaN gate HEMTs, forward gate breakdown usually leads to the complete failure of gate control over the channel thus losing the high-voltage blocking capability on the drain terminal [40–42]. Such a device behavior can be ascribed to the failure of the p-GaN/AlGaN/GaN (p–i–n) junction losing its rectifying function upon the forward gate breakdown, which poses a great safety risk when we rely on these devices to control the high-voltage high-current power electronic systems. To address this issue, we strategically reduce the gate metal foot/p-GaN contact area to ensure the contact region is totally within the p-GaN on all sides rather than using a self-aligned metal/p-GaN contact scheme [43, 44], as illustrated in the schematic shown in figure 7(a). The shrinked foot of the gate metal with respect to the p-GaN, in conjunction with the gate-connected field plate suppressing the electric field at the p-GaN edge, limits the forward gate breakdown to occur only at the gate metal/p-GaN junction with the p-GaN/AlGaN/GaN heterojunction intact.

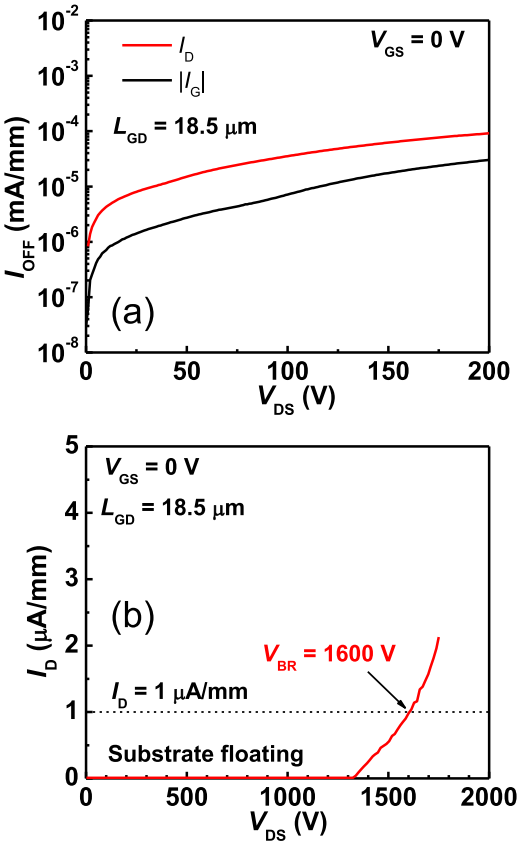

Figure 9. OFF-state leakage current versus drain bias of the p-GaN gate HEMTs (a) for V_{DS} within 200 V and (b) for V_{DS} up to 1800 V.

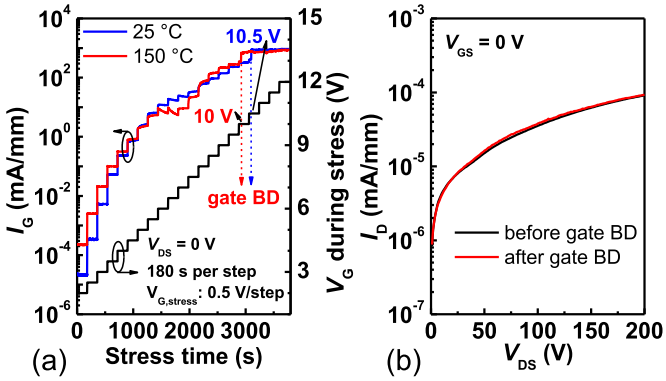

Figure 10. (a) Step stress forward gate breakdown of the p-GaN gate HEMT at 25 °C and 150 °C. (b) OFF-state drain leakage current before and after the step-stress forward gate breakdown.

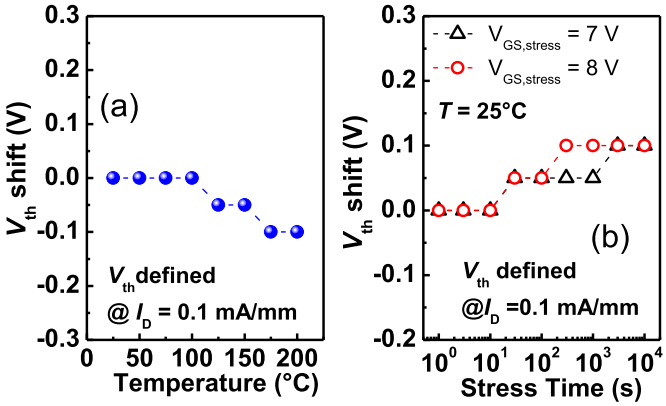

Figure 11. (a) Temperature-dependent V_{th} shift. (b) Time-dependent V_{th} shift induced by constant forward gate stress at 7 V and 8 V.

The step-stressed forward gate breakdown of the p-GaN gate HEMTs is shown in figure 10(a). The forward gate breakdown voltage at 25 °C and 150 °C is 10.5 and 10 V, respectively. The OFF-state drain leakage currents of the device before and after the step-stress forward gate breakdown are compared in figure 10(b). Our devices show persistent high-voltage OFF-state blocking capability after forward gate breakdown with an almost identically low leakage current as that of fresh devices. In order to achieve reliable device operation upon accidental gate failure induced by large overshoot of forward gate bias, the gate architecture needs to be carefully designed to manage the electric field at the p-GaN gate edge.

On the other hand, the V_{th} stability is also critical to the reliable device operation for Schottky-contact p-GaN gate HEMTs. Figure 11(a) shows the dependence of V_{th} shift on the measurement temperature for our p-GaN gate HEMTs. A negative V_{th} shift with the increase of temperature can be observed in the device, which results from the weakened gate control over the channel due to the increased carrier concentration in the bulk GaN under elevated temperature. Nevertheless, benefitting from the high-quality gate metal/p-GaN Schottky contact and the wide band gap nature of GaN material, the V_{th} shift is only ~ -0.1 V when the temperature increases to 200 °C. Another typical approach to evaluate the V_{th} stability in Schottky-contact p-GaN gate HEMTs is submitting the device to large constant forward gate stress for a long term to examine the time-dependent V_{th} shift accelerated by the high electric field in the gate stack [34, 45]. The room temperature time-dependent V_{th} shifts under a constant forward gate stress of 7 and 8 V for 10^4 s are plotted in figure 10(b). The devices exhibit a small positive shift in V_{th} with the increase of stress time and the V_{th} shift is limited to $\sim$0.1 V for a 10 000 s gate stress at both voltages. The positive shift of the threshold voltage suggests electron trapping in the depleted p-GaN region or inside the AlGaN barrier, as also observed by many other researchers [46]. Minimal V_{th} shifts have been achieved in the device under either high-temperature thermal stimulation or long-term large forward gate stress, suggesting excellent stability of the gate stack in our p-GaN gate HEMTs.

4. Comparison of various device structures and discussion

Different approaches to achieve normally-OFF operation based on thin-barrier heterostructures have been presented. The advantages and tradeoffs for each method vary significantly. Figure 12 benchmarks the V_{th} versus $I_{DS,\,max}$ of devices in this work with reported state-of-the-art normally-OFF GaN MOSHEMTs and p-GaN gate HEMTs that employed a thin-barrier heterostructure [26, 29, 37, 47–56]. The V_{th} is

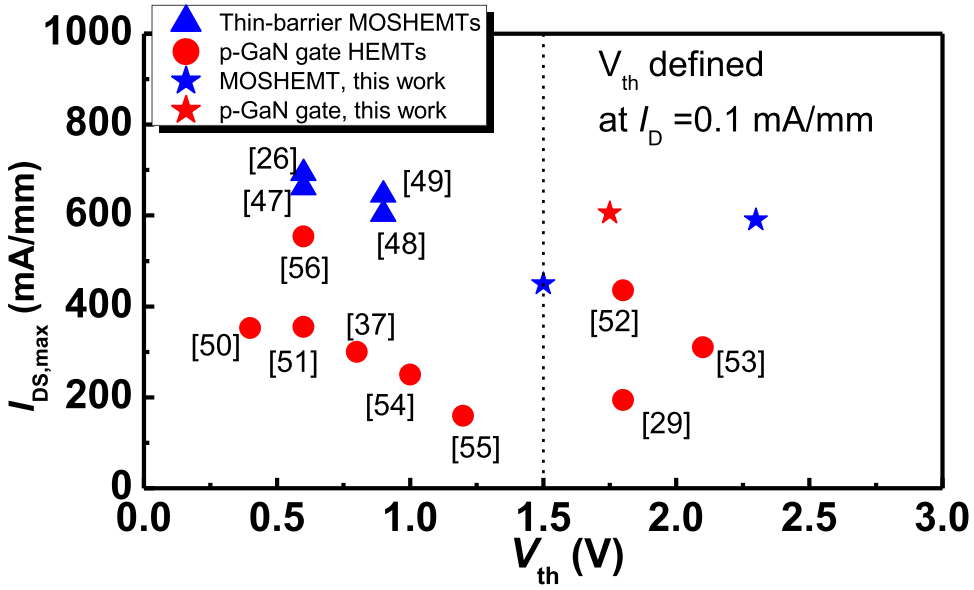

Figure 12. Benchmarking of $I_{DS,\,max}$ versus V_{th} of devices in this work with reported state-of-the-art normally-OFF GaN MOSHEMTs and p-GaN gate HEMTs employing thin-barrier heterostructures.

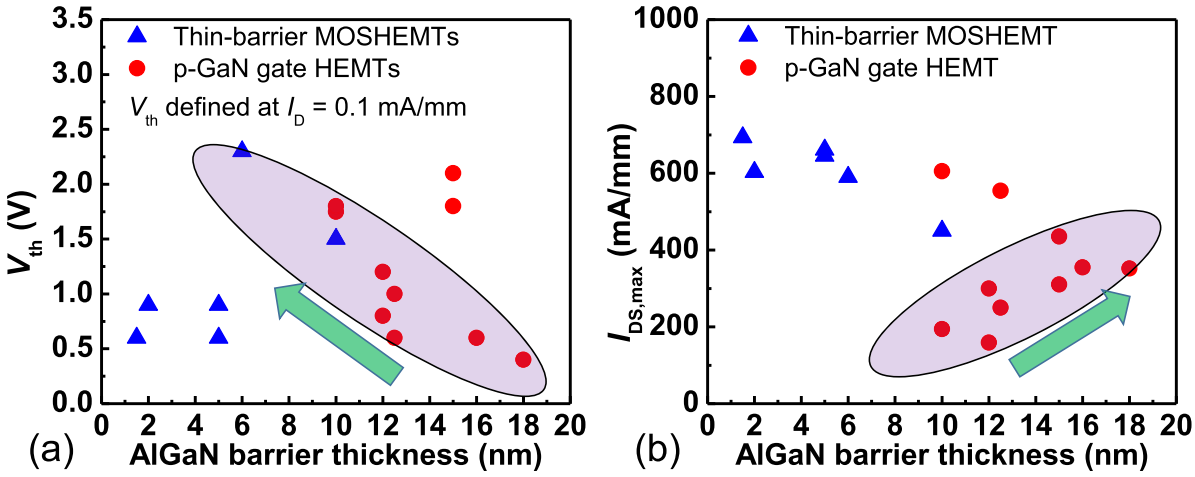

Figure 13. (a) Extracted V_{th} and (b) $I_{DS,\,max}$ as a function of the barrier thickness of the AlGaN/GaN heterostructures employed in the reported normally-OFF GaN MOSHEMTs and p-GaN gate HEMTs.

extracted from transfer curves and defined as the V_G when the I_D reaches 0.1 mA mm^{-1}. The reason we choose to use the drain current constant instead of the linear extrapolation method to define the V_{th} is that the small drain current constant of 0.1 mA mm^{-1} gives a better reflection of the 2DEG concentration under the given V_{GS} that the channel is about to turn on. Nevertheless, the V_{th} by linear extrapolation is still a useful parameter to provide a rough idea on the device operation boundaries, despite that the value could be far deviated from the drain current defined one due to a large SS. It can be observed that our devices show not only a large V_{th} but also a concurrently high $I_{DS,\,max}$.

To further correlate the device performance of V_{th} and $I_{DS,\,max}$ with the heterostructure and gate structure design in the normally-OFF GaN HEMTs, we have plotted the V_{th} and $I_{DS,\,max}$ as a function of the barrier thickness of AlGaN/GaN heterostructures of devices (references in figure 12) with MOS and p-GaN gate stacks, respectively, as shown in figure 13. Clear trends can be observed for p-GaN gate HEMTs that the V_{th} typically decreases and the $I_{DS,\,max}$ increases with the increase of AlGaN barrier thickness. This phenomenon is intuitive since the thicker the AlGaN barrier, the higher the 2DEG concentration (till saturation) at the heterojunction, and the smaller a gate bias needed to turn on the channel. P-GaN gate HEMTs with effective acceptor concentration of the p-GaN cap offer additional manipulation of the V_{th} and $I_{DS,\,max}$ combination. In contrast, no obvious trends with the barrier thickness are observed for the reported thin-barrier GaN MOSHEMTs. The V_{th} varies significantly in devices from one research group to another, even though with a similar barrier thickness. The large deviation of reported GaN MOSHEMTs from the trends we have seen in p-GaN gate HEMTs is mainly due to the complexity of the interface properties of the MOS gate stack, which can vary dramatically resulting from many

factors such as the AlGaN barrier surface status before gate dielectric deposition, interface charge polarity and density, and the dielectric properties.

As such, achieving a large positive V_{th} in thin-barrier MOSHEMTs with stable reproducible results across institutions confronts many more challenges than that for p-GaN gate HEMTs, in which the interfaces of the gate stack are mainly influenced by the as-grown epilayers of the starting wafer. Nevertheless, the MOSHEMT structure is capable to provide a large gate swing with a low gate leakage current, a desirable characteristic yet to be achieved in p-GaN gate HEMTs. The thin-barrier MOSHEMTs may become as consistent as the p-GaN gate HEMTs, provided that the issues in the MOS gate stack are well addressed. On the other hand, despite the commercialization of p-GaN gate HEMTs, the device potential are still yet to be demonstrated to its theoretical limits, compared with their depletion-mode counterparts. More research efforts are to be devoted to the p-GaN gate HEMTs to take full advantages of the material promise.

5. Conclusions

In this work, we have presented our recent research results on normally-OFF GaN HEMTs with MOS and p-GaN gate structures, both of which are enabled by the utilization of thin-barrier AlGaN/GaN heterostructures. Both a large V_{th} and a high $I_{DS,\,max}$ have been achieved in our devices. Moreover, a high breakdown voltage is demonstrated in the recess-free thin-barrier MOSHEMTs with a simple fabrication process and the p-GaN gate HEMTs. The p-GaN gate HEMTs have also exhibited superior reliable gate operation with persistent OFF-state high-voltage blocking capability after forward gate breakdown and minimal V_{th} shifts upon high-temperature thermal stimulation and long-term gate stress. We have also compared the device performance in thin-barrier MOSHEMTs and p-GaN gate HEMTs. The correlation of ON-state parameters in terms of V_{th} and $I_{DS,\,max}$ with the barrier thickness of AlGaN/GaN heterostructures are discussed. This work is able to provide some general guidelines of device design for further advancement of normally-OFF GaN HEMTs employing thin-barrier heterostructures.

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References

[1] Chen K J, Häberlen O, Lidow A, Tsai C L, Ueda T, Uemoto Y and Wu Y 2017 GaN-on-Si power technology: devices and applications *IEEE Trans. Electron Devices* **64** 779–95
[2] Ma J, Erine C, Zhu M, Luca N, Xiang P, Cheng K and Matioli E 2019 1200 V multi-channel power devices with 2.8 Ω mm ON-resistance *2019 IEEE Int. Electron Devices Meeting (IEDM)* pp 4.1.1–4.1.4
[3] Jones E A, Wang F F and Costinett D 2016 Review of commercial GaN power devices and GaN-based converter design challenges *IEEE J. Emerging Sel. Top. Power Electron.* **4** 707–19
[4] Ikeda N, Li J and Yoshida S 2004 Normally-off operation power AlGaN/GaN HFET *2004 Proc. of the 16th Int. Symp. on Power Semiconductor Devices and ICs* pp 369–72
[5] Saito W, Takada Y, Kuraguchi M, Tsuda K and Omura I 2006 Recessed-gate structure approach toward normally off high-voltage AlGaN/GaN HEMT for power electronics applications *IEEE Trans. Electron Devices* **53** 356–62
[6] Oka T and Nozawa T 2008 AlGaN/GaN recessed MIS-gate HFET with high-threshold-voltage normally-off operation for power electronics applications *IEEE Electron Device Lett.* **29** 668–70
[7] Kanamura M, Ohki T, Kikkawa T, Imanishi K, Imada T, Yamada A and Hara N 2010 Enhancement-mode GaN MIS-HEMTs with n-GaN/i-AlN/n-GaN triple cap layer and high-*k* gate dielectrics *IEEE Electron Device Lett.* **31** 189–91
[8] Medjdoub F, Derluyn J, Cheng K, Leys M, Degroote S, Marcon D, Visalli D, Hove M V, Germain M and Borghs G 2010 Low on-resistance high-breakdown normally off AlN/GaN/AlGaN DHFET on Si substrate *IEEE Electron Device Lett.* **31** 111–3
[9] Cai Y, Zhou Y, Chen K J and Lau K M 2005 High-performance enhancement-mode AlGaN/GaN HEMTs using fluoride-based plasma treatment *IEEE Electron Device Lett.* **26** 435–7
[10] Wang Y, Wang M, Xie B, Wen C P, Wang J, Hao Y, Wu W, Chen K J and Shen B 2013 High-performance normally-off Al_2O_3/GaN MOSFET using a wet etching-based gate recess technique *IEEE Electron Device Lett.* **34** 1370–2
[11] Hahn H, Benkhelifa F, Ambacher O, Brunner F, Noculak A, Kalisch H and Vescan A 2015 Threshold voltage engineering in GaN-based HFETs: a systematic study with the threshold voltage reaching more than 2 V *IEEE Trans. Electron Devices* **62** 538–45
[12] Huang S *et al* 2016 High uniformity normally-OFF GaN MIS-HEMTs fabricated on ultra-thin-barrier AlGaN/GaN heterostructure *IEEE Electron Device Lett.* **37** 1617–20
[13] Ma J, Erine C, Xiang P, Cheng K and Matioli E 2018 Multi-channel tri-gate normally-on/off AlGaN/GaN MOSHEMTs on Si substrate with high breakdown voltage and low ON-resistance *Appl. Phys. Lett.* **113** 242102
[14] Zhu M, Ma J, Nela L, Erine C and Matioli E 2019 High-voltage normally-off recessed tri-gate GaN power MOSFETs with low on-resistance *IEEE Electron Device Lett.* **40** 1289–92
[15] Hwang I *et al* 2013 p-GaN gate HEMTs with tungsten gate metal for high threshold voltage and low gate current *IEEE Electron Device Lett.* **34** 202–4
[16] Uemoto Y, Hikita M, Ueno H, Matsuo H, Ishida H, Yanagihara M, Ueda T, Tanaka T and Ueda D 2007 Gate injection transistor (GIT): a normally-off AlGaN/GaN power transistor using conductivity modulation *IEEE Trans. Electron Devices* **54** 3393–9
[17] Cai Y, Zhou Y, Lau K M and Chen K J 2006 Control of threshold voltage of AlGaN/GaN HEMTs by fluoride-based

plasma treatment: from depletion mode to enhancement mode *IEEE Trans. Electron Devices* **53** 2207–15
[18] Wang Y H, Liang Y C, Samudra G S, Huang H, Huang B J, Huang S H, Chang T F, Huang C F, Kuo W H and Lo G Q 2015 6.5 V high threshold voltage AlGaN/GaN power metal–insulator–semiconductor high electron mobility transistor using multilayer fluorinated gate stack *IEEE Electron Device Lett.* **36** 381–3
[19] Hu X, Simin G, Yang J, Khan M A, Gaska R and Shur M S 2000 Enhancement mode AlGaN/GaN HFET with selectively grown pn junction gate *Electron. Lett.* **36** 753–4
[20] Greco G, Iucolano F and Roccaforte F 2017 Review of technology for normally-off HEMTs with p-GaN gate *Mater. Sci. Semicond. Process.* **78** 96–106
[21] Brown R, Macfarlane D, Al-Khalidi A, Xu L, Ternent G, Haiping Z, Thayne I and Wasige E 2014 A sub-critical barrier thickness normally-off AlGaN/GaN MOS-HEMT *IEEE Electron Device Lett.* **35** 906–8
[22] Ibbetson J P, Fini P T, Ness K D, DenBaars S P, Speck J S and Mishra U K 2000 Polarization effects, surface states, and the source of electrons in AlGaN/GaN heterostructure field effect transistors *Appl. Phys. Lett.* **77** 250–2
[23] Ambacher O *et al* 2000 Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures *J. Appl. Phys.* **87** 334–44
[24] Endoh A, Yamashita Y, Ikeda K, Higashiwaki M, Hikosaka K, Matsui T, Hiyamizu S and Mimura T 2004 Non-recessed-gate enhancement-mode AlGaN/GaN high electron mobility transistors with high RF performance *Japan. J. Appl. Phys.* **43** 2255–8
[25] Huang S *et al* 2014 High-temperature low-damage gate recess technique and ozone-assisted ALD-grown Al_2O_3 gate dielectric for high-performance normally-off GaN MIS-HEMTs *2014 IEEE Int. Electron Devices Meeting* pp 17.4.1–4.4
[26] Zhou Q, Chen B, Jin Y, Huang S, Wei K, Liu X, Bao X, Mou J and Zhang B 2015 High-performance enhancement-mode Al2O3/AlGaN/GaN-on-Si MISFETs with 626 MW cm^{-2} figure of merit *IEEE Trans. Electron Devices* **62** 776–81
[27] Xu Z *et al* 2014 Demonstration of normally-off recess-gated AlGaN/GaN MOSFET using GaN cap layer as recess mask *IEEE Electron Device Lett.* **35** 1197–9
[28] Hua M, Zhang Z, Wei J, Lei J, Tang G, Fu K, Cai Y, Zhang B and Chen K J 2016 Integration of LPCVD-SiN*x* gate dielectric with recessed-gate E-mode GaN MIS-FETs: toward high performance, high stability and long TDDB lifetime *2016 IEEE Int. Electron Devices Meeting (IEDM)* pp 10.4.1–4.4
[29] Lee F, Su L Y, Wang C H, Wu Y R and Huang J 2015 Impact of gate metal on the performance of p-GaN/AlGaN/GaN high electron mobility transistors *IEEE Electron Device Lett.* **36** 232–4
[30] Okita H, Hikita M, Nishio A, Sato T, Matsunaga K, Matsuo H, Mannoh M and Uemoto Y 2016 Through recessed and regrowth gate technology for realizing process stability of GaN-GITs *2016 28th Int. Symp. on Power Semiconductor Devices and ICs (ISPSD)* pp 23–26
[31] Zhong Y, Su S, Zhou Y, Gao H, Chen X, He J, Zhan X, Sun Q and Yang H 2019 Effect of thermal cleaning prior to p-GaN gate regrowth for normally off high-electron-mobility transistors *ACS Appl. Mater. Interfaces* **11** 21982–7
[32] Jiang H, Liu C, Ng K W, Tang C W and Lau K M 2018 High-performance AlGaN/GaN/Si Power MOSHEMTs with ZrO_2 gate dielectric *IEEE Trans. Electron Devices* **65** 5337–42
[33] Jiang H, Tang C W and Lau K M 2018 Enhancement-mode GaN MOS-HEMTs with recess-free barrier engineering and high-*k* ZrO_2 gate dielectric *IEEE Electron Device Lett.* **39** 405–8
[34] Jiang H, Liu C, Chen Y, Lu X, Tang C W and Lau K M 2017 Investigation of *in situ* SiN as gate dielectric and surface passivation for GaN MISHEMTs *IEEE Trans. Electron Devices* **64** 832–9
[35] Jiang H, Lu X, Liu C, Li Q and Lau K M 2016 Off-state drain leakage reduction by post metallization annealing for Al_2O_3/GaN/AlGaN/GaN MOSHEMTs on Si *Phys. Status Solidi* a **213** 868–72
[36] Ishida M, Ueda T, Tanaka T and Ueda D 2013 GaN on Si technologies for power switching devices *IEEE Trans. Electron Devices* **60** 3053–9
[37] Hilt O, Zhytnytska R, Böcker J, Bahat-Treidel E, Brunner F, Knauer A, Dieckerhoff S and Würfl J 2015 70 mΩ/600 V normally-off GaN transistors on SiC and Si substrates *2015 IEEE 27th Int. Symp. on Power Semiconductor Devices & IC's (ISPSD)* pp 237–40
[38] Jiang H, Zhu R, Lyu Q and Lau K M 2019 High-voltage p-GaN HEMTs with OFF-state blocking capability after gate breakdown *IEEE Electron Device Lett.* **40** 530–3
[39] Liu Z H, Ng G I, Zhou H, Arulkumaran S and Maung Y K T 2011 Reduced surface leakage current and trapping effects in AlGaN/GaN high electron mobility transistors on silicon with SiN/Al_2O_3 passivation *Appl. Phys. Lett.* **98** 113506
[40] Meneghini M *et al* 2017 Reliability and failure analysis in power GaN-HEMTs: an overview *2017 IEEE Int. Reliability Physics Symp. (IRPS)* pp 3B-2.1–8
[41] Ťapajna M, Hilt O, Bahat-Treidel E, Würfl J and Kuzmík J 2016 Gate reliability investigation in normally-off p-type-GaN Cap/AlGaN/GaN HEMTs under forward bias stress *IEEE Electron Device Lett.* **37** 385–8
[42] Rossetto I, Meneghini M, Hilt O, Bahat-Treidel E, Santi C D, Dalcanale S, Wuerfl J, Zanoni E and Meneghesso G 2016 Time-dependent failure of GaN-on-Si power HEMTs with p-GaN gate *IEEE Trans. Electron Devices* **63** 2334–9
[43] Wu T L, Marcon D, You S, Posthuma N, Bakeroot B, Stoffels S, Hove M V, Groeseneken G and Decoutere S 2015 Forward bias gate breakdown mechanism in enhancement-mode p-GaN Gate AlGaN/GaN high-electron mobility transistors *IEEE Electron Device Lett.* **36** 1001–3
[44] Kim J *et al* 2013 High threshold voltage p-GaN gate power devices on 200 mm Si *2013: 25th Int. Symp. on Power Semiconductor Devices & IC's (ISPSD)* pp 315–8
[45] Sayadi L, Iannaccone G, Sicre S, Häberlen O and Curatola G 2018 Threshold voltage instability in p-GaN gate AlGaN/GaN HFETs *IEEE Trans. Electron Devices* **65** 2454–60
[46] Tallarico A N, Stoffels S, Posthuma N, Magnone P, Marcon D, Decoutere S, Sangiorgi E and Fiegna C 2018 PBTI in GaN-HEMTs with p-type gate: role of the aluminum content on ΔV_{TH} and underlying degradation mechanisms *IEEE Trans. Electron Devices* **65** 38–44
[47] Huang S *et al* 2018 Ultrathin-barrier AlGaN/GaN heterostructure: a recess-free technology for manufacturing high-performance GaN-on-Si power devices *IEEE Trans. Electron Devices* **65** 207–14
[48] Liu S *et al* 2017 Gate-recessed normally-OFF GaN MOSHEMT with improved channel mobility and dynamic performance using AlN/Si_3N_4 as passivation and post gate-recess channel protection layers *IEEE Electron Device Lett.* **38** 1075–8
[49] Zhang J *et al* 2018 High-mobility normally OFF Al_2O_3/AlGaN/GaN MISFET with damage-free recessed-gate structure *IEEE Electron Device Lett.* **39** 1720–3
[50] Hao R *et al* 2017 Breakdown enhancement and current collapse suppression by high-resistivity GaN cap layer in

normally-off AlGaN/GaN HEMTs *IEEE Electron Device Lett.* **38** 1567–70

[51] Zhou Y, Zhong Y, Gao H, Dai S, He J, Feng M, Zhao Y, Sun Q, Dingsun A and Yang H 2017 p-GaN gate enhancement-mode HEMT through a high tolerance self-terminated etching process *IEEE J. Electron Devices Soc.* **5** 340–6

[52] Zhong Y *et al* 2019 Normally-off HEMTs with regrown p-GaN gate and low-pressure chemical vapor deposition SiN_x passivation by using an AlN pre-layer *IEEE Electron Device Lett.* **40** 1495–8

[53] Wang C, Hua M, Yang S, Zhang L and K J C 2020 E-mode p–n junction/AlGaN/GaN HEMTs with enhanced gate reliability *2020 32nd Int. Symp. on Power Semiconductor Devices and ICs (ISPSD)* pp 14–7

[54] Li X, Hove M V, Zhao M, Geens K, Lempinen V P, Sormunen J, Groeseneken G and Decoutere S 2017 200 V enhancement-mode p-GaN HEMTs fabricated on 200 mm GaN-on-SOI with trench isolation for monolithic integration *IEEE Electron Device Lett.* **38** 918–21

[55] Liu X, Chiu H, Liu C, Kao H, Chiu C, Wang H, Ben J, He W and Huang C 2020 Normally-off p-GaN Gated AlGaN/GaN HEMTs using plasma oxidation technique in access region *IEEE J. Electron Devices Soc.* **8** 229–34

[56] Lükens G, Hahn H, Kalisch H and Vescan A 2018 Self-aligned process for selectively etched p-GaN-gated AlGaN/GaN-on-Si HFETs *IEEE Trans. Electron Devices* **65** 3732–8