Selectively Grown III-V Lasers for Integrated Si-Photonics

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(Invited Paper)

***Abstract*—Epitaxially integrating III-V lasers with Si-photonics is the key for compact, efficient, and scalable photonic integrated circuits (PICs). Here we present an investigation of a path forward in integrating III-V functionalities on industry-standard silicon-on-insulator (SOI) platforms using selective area hetero-epitaxy. Based on our recently developed methods of selectively growing device quality InP on (001)-oriented SOI wafers, we demonstrated InP stripes and segments, with dimensions varying from a few hundred nanometers to a few micrometers. The flexible epitaxy of InP on SOI together with the unique "bufferless" trait will enable efficient light interfacing with Si-based photonic devices using either evanescent or butt coupling schemes. We simulated the possibility of employing the micrometer-scale InP on insulator to realize electrically driven lasers and found that the metal induced optical loss is negligible when the InP dimension exceeds 4.0 μm. The potential of utilizing this selective area growth method to realize fully integrated Si-photonics is illustrated.**

***Index Terms*—Integrated photonics, III-V lasers, Si-photonics, selective area growth.**

I. Introduction

SI-PHOTONICS is the key technology to mitigate the interconnect bottleneck in current data-communication systems [1], [2], and has received increasing interest in other various applications such as high performance computing, quantum communication, microwave engineering, sensing, etc [3]–[7]. The extensive research of Si-photonics is driven by the superior wave-guiding property of the Si/SiN/SiO_2 material system and the cost-effective and high-throughput manufacturing infrastructure well established by the microelectronics foundries. However, the indirect energy band nature of Si forbids efficient light emission and incorporation of Si/Ge has not been fruitful. III-V materials for coherent photon generation have been developed for decades and deployed in telecommunication systems. To include light sources in Si photonics, heterogeneous integration of III-V lasers on Si using wafer/die bonding or transfer printing techniques preserves the high quality of the source materials and guarantees an intimate interfacing of the III-V light sources and the Si-waveguides [8]–[12]. Nevertheless, fully integrated Si-based PICs and future co-integration with microelectronics calls for a low-cost, wafer-scale, and monolithic integration approach via direct hetero-epitaxy [13]–[16]. Two different schemes have been developed to directly grow III-V lasers on industry-standard Si wafers. In the first approach, III-V lasers are integrated onto planar Si substrates using blanket hetero-epitaxy [17]–[18]. Several micrometer thick buffers with elaborate defect filtering layers are typically employed to reduce the density of threading dislocations, and quantum dots are usually selected as active gain medium to further improve the device reliability. This approach was extensively investigated over the last decade and has produced electrically driven lasers with impressive lifetimes [19]. However, the thick buffer layers used in this method present obstacles towards monolithic integration with Si-based photonic devices [20]. In the second approach, III-V lasers are selectively grown on pre-patterned Si/SOI wafers [21]–[23]. Crystalline defects induced by lattice mismatch are generally confined at the limited III-V/Si interface, and dislocation-free III-V materials can be produced away from the hetero-interfaces [24]–[26]. Additionally, the intimate placement of the III-V alloys and Si can facilitate efficient light coupling [27]. This method also receives considerable research effort in the last decade and has spawned different selective growth techniques including aspect ratio trapping (ART), nanoridge engineering (NRE) and template assisted selective epitaxy (TASE) [28]–[31]. A complete suite of III-V alloys, including GaAs, InP, InGaAs, GaSb, and InAs were selectively grown on Si [32]–[37], and III-V lasers with emission wavelengths over the entire telecom bands were epitaxially integrated on Si/SOI wafers [38]–[41]. However, all these light sources operate under optical excitation as the material volume is limited at nanometer-scale and electrical metal contacts would consequently induce large optical absorption loss. Therefore, the main challenge of this integration scheme is the realization of electrically driven III-V lasers and the design of efficient light coupling strategies with Si-photonics [42].

In this work, we evaluate the prospect of employing selectively grown III-V materials on Si for the next-generation fully integrated Si-photonics. First, we present an overview of the selective area growth of bufferless and in-plane InP

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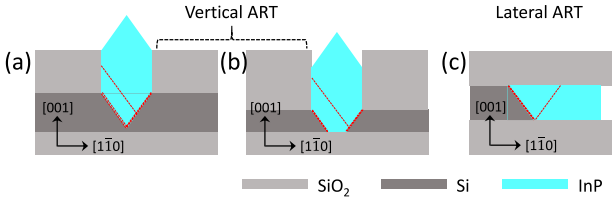

Fig. 1. (a) Schematic showing the growth of InP on V-grooved SOI using the "vertical ART" method. (b) Schematic showing the growth of InP on 220 nm SOI using the "vertical ART" method. (c) Schematic showing the growth of InP on SOI using the "lateral ART" method. The red dotted lines denote the confinement of crystalline defects at the III-V/Si interface and the block of defects by the oxide spacers.

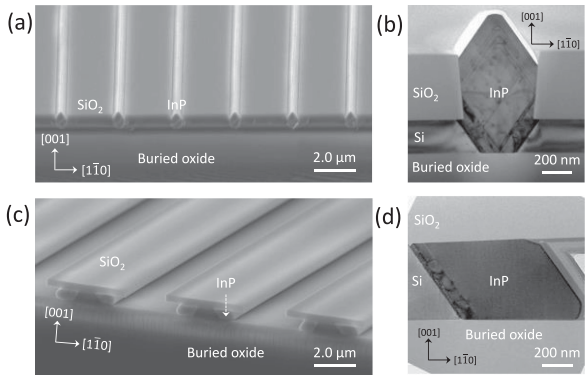

Fig. 2. (a) Tilted-view SEM image of InP nano-ridges grown on SOI using the "vertical ART" method. (b) Cross-sectional TEM image of one InP nano-ridge. (c) Tilted-view SEM image of InP grown on SOI using the "lateral ART" method. (d) Cross-sectional TEM image of InP grown laterally on SOI.

on (001)-oriented SOI platforms using metal organic chemical vapor deposition (MOCVD). Then we design and simulate both evanescent and butt coupling schemes for efficiently interfacing the epitaxial InP with Si-waveguides. And finally, we assess the possibility of employing the selectively grown InP for electrically driven lasers integrated with Si-photonics.

II. Bufferless InP Selectively Grown on SOI

Among the family of III-V compounds, InP acts as the host material for lasers emitting at telecom wavelengths and serves as the major platform for commercially available PICs. Naturally integrating InP with Si-photonics provides the essential light sources for current Si-based data/telecom applications, and, at the same time, synergizes these two platforms for unprecedented functionalities and performances [10]. Nevertheless, direct growth of InP on Si wafers is extremely challenging. Unlike GaAs growth on Si where the lattice mismatch is around 4% and the morphology and architecture of GaAs can be readily manipulated [23], the 8% lattice mismatch together with the large diffusivity of indium adatoms significantly complicate the hetero-epitaxy of InP on Si [24]. To date, the technology of 1.3 μm lasers grown on GaAs/Si templates is much more mature than that of 1.55 μm lasers grown on InP/Si templates [43]. Selective area epitaxy of InP with growth initiation at {111}-oriented Si facets and confinement/guidance provided by the growth masks proves to be a promising alternative. In this section, we outline our recent research of selective area growth of InP on patterned SOI substrates using both the conventional "vertical ART" approach and our novel "lateral ART" method. The dimension of the epitaxial InP can be adjusted from nanometer-scale to micrometer-scale, and the architecture can also be tailored. This epitaxial versatility and flexibility potentially facilitate the fabrication of different InP-based optoelectronic devices and the subsequent interfacing with Si-based photonic/electronic components.

A. Nanometer-Scale InP Stripes on SOI

Fig. 1 schematically summarizes the growth scheme of the "vertical ART" and the "lateral ART" techniques. In both schemes, the oxide trenches are aligned in the [110] direction perpendicular to the drawings, and wet etching is employed to create the {111}-oriented Si facets to prevent the formation of anti-phase boundaries [33]. In the "vertical ART" approach as shown in Fig. 1(a) and (b), growth initiates inside a pocket enclosed by two {111} Si facets and evolves vertically into nano-ridge structures [44]–[45]. Depending on the thickness of the Si-device layer on the SOI, the pocket is either a V-grooved furrow (see Fig. 1(a)) or a trapezoidal trough (see Fig. 1(b)). The width of the oxide trench is usually kept at around 500 nm to support the fundamental modes at telecom wavelengths. A narrower trench induces large optical loss while a wider trench compromises the defect necking effect that a minimum aspect ratio of 1.4 is needed. The height of the epitaxial InP hinges on the thickness of the oxide mask for selective area epitaxy and the total growth time. In the "lateral ART" approach as shown in Fig. 1(c), growth initiates from a {111}-oriented Si bevel and evolves laterally along the lateral oxide trench. The thickness of the Si-device layer can be adjusted from 220 nm to over 500 nm for mode guiding at telecom bands, and the width of the epitaxial InP is tunable through varying the undercut of the oxide trench as well as the growth parameters. In both methods, strain induced by the lattice mismatch is largely accommodated by a thin layer (around 10 nm) of highly twined regions at the III-V/Si interface, and crystalline defects including threading dislocations and stacking faults that penetrate into the InP crystal will be blocked by the oxide spacers. The red dotted lines in Fig. 1 denote this unique defect necking effect of the "ART" growth method. The defect density drastically reduces as InP grows away from the hetero-interface and the InP is presumably dislocation-free when the aspect ratio is larger than 1.4 [25].

Fig. 2 presents scanning electron microscopy (SEM) images of nanometer-scale InP grown on SOI using the "vertical ART" and the "lateral ART" methods. As shown in Fig. 2(a), the "vertical ART" approach produces InP nano-ridge array on SOI, which extends across the entire wafer. Fig. 2(b) displays a cross-sectional transmission electron microscopy (TEM) image of one nano-ridge. Detailed growth conditions can be found in Ref. [45]. Evidently, lattice mismatch is largely accommodated through a highly twined region at the III-V/Si interface, rendering the above InP ridge with excellent crystalline qualities. Fig. 2(c) shows a SEM image of nanometer-scale InP stripe

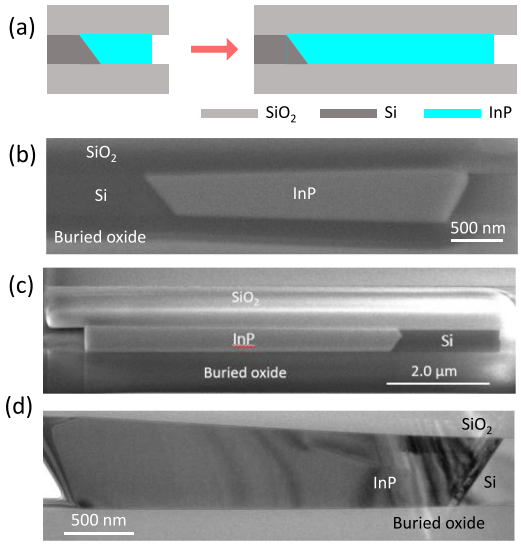

Fig. 3. (a) Schematic showing the growth of micrometer-scale InP on SOI using the "lateral ART" method. (b) Cross-sectional SEM image of 3.0 μm wide InP grown on SOI. (c) Cross-sectional SEM image of 6.0 μm wide InP grown on SOI. (d) Cross-sectional TEM image of micrometer-scale InP grown on SOI.

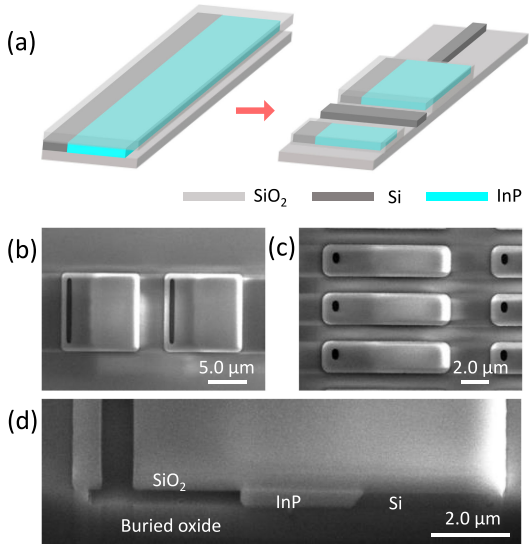

Fig. 4. (a) Schematic showing the growth of InP segments on SOI. (b) SEM image of 10 μm long InP segments grown on SOI. (c) SEM image of 2.0 μm long InP segments grown on SOI. (d) Cross-sectional SEM image of InP segments grown on SOI.

grown using the "lateral ART" approach. Pattern preparation and detailed growth parameters can be accessed in Ref. [29]. Symmetrical InP crystals form inside the lateral oxide trenches, and spans across the entire wafer. As shown by the cross-sectional TEM image in Fig. 2(d), crystalline defects induced by lattice mismatch are completely confined at the III-V/Si interface and blocked by the top SiO_2 layer and the buried oxide layer. The rest of the laterally grown InP crystal is thereby dislocation-free.

B. Micrometer-Scale InP Stripes on SOI

The nanometer-scale InP grown on SOI can support strong modes at the telecom bands and we have demonstrated room temperature lasers on SOI under optical pumping [45]–[46]. To realize electrically driven lasers, larger dimension InP is needed for patterning metal contacts with minimal induced optical absorption loss. In addition, enlarging the size of the epitaxial InP provides more flexibility in the design and fabrication of other III-V based devices such as modulators and photo-detectors. In the "vertical ART" method, we can expand the dimension of the InP through patterning deeper oxide trenches and growing higher ridges. In the "lateral ART" method, we can extend the dimension of the InP through etching deeper lateral oxide trenches and growing wider crystals. The beauty of the latter method compared with the former one lies at ease of scaling to achieve larger dimension InP while simultaneously maintaining a co-planar configuration with the Si device layer, as illustrated by the schematics in Fig. 3(a). We conducted the growth of micrometer-scale InP on SOI using the "lateral ART" method, and Fig. 3(b) and (c) show a cross-sectional SEM photo of InP crystals with a width of 3.0 μm and 6.0 μm, respectively. Similar to the nanometer-scale InP, crystalline defects are confined at the III-V/Si interface and the majority of the micrometer-InP are completely dislocation-free (see the TEM image in Fig. 3(d)). The linear change of the InP thickness in Fig. 3(b) and (d) results from a slight removal of the oxide mask during the wet-etching to create the deep undercut of the Si device layer for InP growth. This issue can be assuaged through performing the etching at a lower etch rate (see the example in Fig. 3(c)). The lateral dimension of the epitaxial InP is ultimately limited by the diffusion length of the growth precursors under viable optimized growth conditions and could theoretically reach up to tens of micrometers [47], [48].

C. InP Segments on SOI

In the study of nanometer/micrometer-scale InP stripes on SOI, the position of the epitaxial InP depends on the pre-defined parallel oxide stripes extending across the entire wafer. To allow for flexibility in future PIC designs, various growth patterns are investigated in controlling the position, dimension and architecture of InP selectively grown on SOI. As illustrated by the schematics in Fig. 4(a), we segment the long InP stripes grown on SOI into short sections with a variety of lengths through synergizing the "lateral ART" and the TASE method. The SAG of InP on SOI is enabled by the creation of oxide templates to guide the lateral epitaxy of InP inside the segmented lateral trenches. In this case, we achieved three-dimensional control of the thickness, width, and length of the epitaxial InP. The thickness of the InP follows that of the Si device layer; the width hinges on the depth of trench undercut and the growth time; and the length depends on the size of the oxide templates created by lithography. Additionally, the non-epitaxy area where growth masks reside can be reserved for patterning in-plane Si-waveguides, the position and structure of which can be precisely defined and aligned using photolithography (see Fig. 4(a)). Fig. 4(b) and (c) showcases SEM images of InP

segments with a length of 10 μm and 2 μm respectively, and Fig. 4(d) shows a cross-sectional SEM photo of the epitaxial InP segments. The thickness of the InP is around 480 nm; the length of the oxide templates or InP segments varies from a few hundred nanometers to tens of micrometers; and the width of the InP segments ranges from a few hundred nanometers to a few micrometers. Analogous techniques can also be applied to grow segmented InP ridges on SOI using the "vertical ART" method.

III. Light Coupling With Si-Photonics

The bufferless and in-plane attributes of the InP grown on SOI together with the intimate placement with the Si device layer facilitate efficient light coupling between InP-based active optical devices and Si-based passive photonic components. On-chip light interfacing has been successfully demonstrated by bonding high performance III-V devices onto Si resonators or waveguides, with the demonstration of high performance hybrid devices that exploit the advantages of both III-V and Si. Examples include narrow line-width lasers and high speed photo-detectors [10], [49], [50]. With selective epitaxy, as the position and dimension of the epitaxial InP and Si-waveguides can be concurrently defined using photolithography, we expect ultra-effective light coupling strategies which may lead to PICs with ultra-high density and complexity. In this section, we carry out a theoretical study of simple light coupling schemes between Si-waveguides and the epitaxial InP grown on SOI based on dimensions compatible with the InP grown by the "vertical ART" and "lateral ART" methods. Note that in the following designs, both the III-V laser and the Si-waveguides are air-cladded without oxide encapsulation. The flexible epitaxy of InP with different geometries and dimensions allows for both evanescent coupling and butt coupling. We only consider directional couplers in this section, although more advanced designs such as tapered and adiabatic couplers are equally applicable.

A. Evanescent Coupling

We use 3D Finite Difference Time Domain (FDTD) method to study the coupling efficiency between the epitaxial InP and directional Si-waveguides. The central wavelength is set at 1550 nm, but analogous results can be extended to the 1330 nm band as well. Fig. 5(a) depicts the evanescent coupling scheme of the Si rib waveguide and the InP ridge structures grown on 220 nm SOI using the "vertical ART" method. We aim at coupling the fundamental TE mode into the Si waveguides, while the mode inside the InP ridge is chosen as TE_{01} mode which is the lasing mode of our demonstrated lasers on SOI [45]. Compared with the fundamental modes, the TE_{01} mode exhibits a larger overlap with the active gain medium and a higher end-facet reflectivity. In addition, the profile of the TE_{01} mode facilitates efficient coupling of the fundamental mode into the Si waveguide as the height of the InP ridge exceeds that of the Si rib waveguide. As illustrated by the cross-sectional schematic in Fig. 5(a), the InP ridge features a width of 500 nm and a height of 800 nm; the Si rib waveguide made from the SOI device layer manifests a thickness of 220 nm, a width of 450 nm and a slab thickness of 50 nm. As shown by the plot

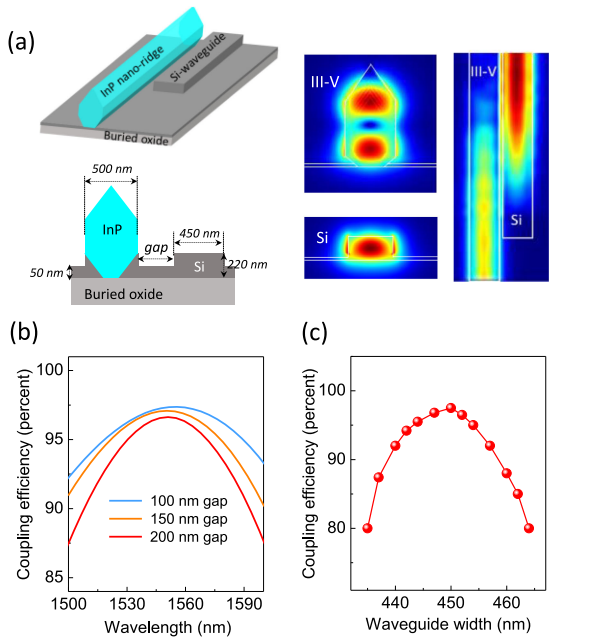

Fig. 5. (a) Coupling scheme, mode profiles, and field exchange image between the III-V laser and Si rib waveguide for the "vertical ART" method. (b) Coupling efficiency versus wavelength at varied coupling gap. (c) The evolution of coupling efficiency in relation to the width of the Si rib waveguide. The gap is set as 100 nm.

of field exchange in Fig. 5(a), the optical mode inside the III-V progressively couples into the Si rib waveguide as the overlap lengthens. With a gap between InP and Si fixed at 100 nm, the coupling efficiency can be as high as 97% and the coupling length is as short as 13 μm. When the gap increases to 150 nm and then to 200 nm, the coupling length correspondingly extends to 20 μm and 30 μm, respectively. Fig. 5(b) displays the coupling efficiency at different wavelengths with a gap of 100 nm, 150 nm and 200 nm. The peak coupling efficiency exceeds 95% in all three cases, and the efficiency drop is less than 10% with a 100 nm wavelength shift. Fig. 5(c) plots the coupling efficiency versus the waveguide width centered at 450 nm. The coupling efficiency remains as high as 80% when a 30 nm width variation is introduced into the rib waveguide.

Fig. 6(a) sketches the evanescent coupling scheme of the Si strip waveguide and the InP stripes/segments grown on SOI using the "lateral ART" method. The thickness of epitaxial InP and Si strip waveguide is 480 nm; the width of the Si strip waveguide is designed as 340 nm to reach the phase matching condition at 1550 nm; the width of the InP is chosen as 900 nm to support the TE_{01} mode for a fair comparison with the "vertical ART" approach. Note that, to support lasing of the TE_{01} mode in lasers, the geometry of the InP must be carefully tailored using conventional top-down processing and the orientation of the InGaAs quantum wells should be carefully engineered. In addition, gratings can also be employed to select the desired lasing mode. Similarly, the TE_{01} mode in the epitaxial InP is coupled into the fundamental TE mode in the Si waveguide, as illustrated by the plot of field exchange in Fig. 6(a). When the gap between the InP and Si is 100 nm, the peak coupling

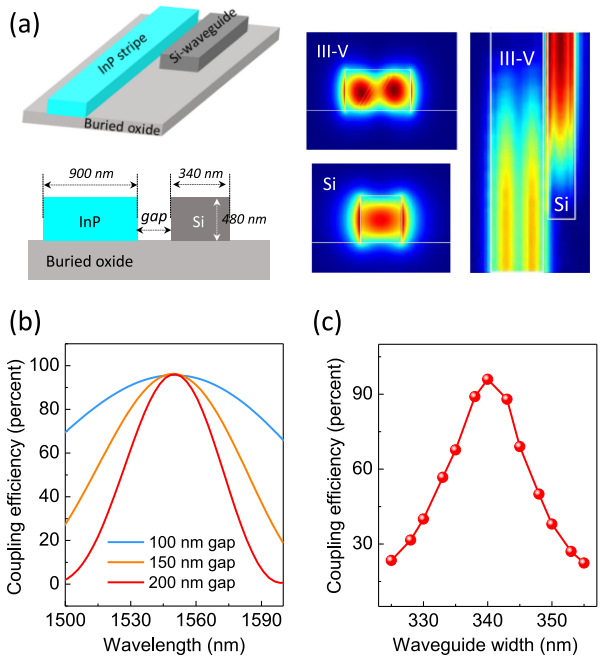

Fig. 6. (a) 3D schematic of laser with directional coupler, mode profiles inside the III-V and Si waveguides, and 2D field exchange image between the laser and Si strip waveguide for the "lateral ART" method. (b) Coupling efficiency at various wavelength for coupling gap is 100 nm, 150 nm and 200 nm. (c) The evolution of coupling efficiency in relation to the width of the Si rib waveguide. The gap is set as 100 nm.

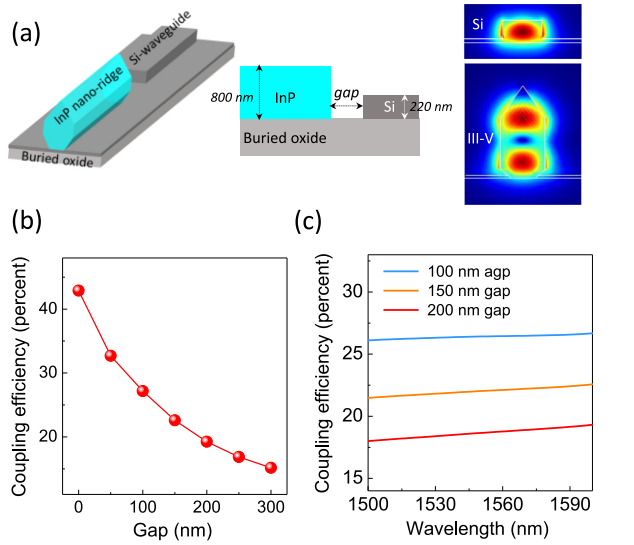

Fig. 7. (a) butt-coupling strategy and III-V laser mode and Si waveguide mode for the "vertical ART" method. (b) Coupling efficiency at 1550 nm for varied coupling gap. (c) Coupling efficiency versus wavelength at various coupling gap.

efficiency is around 95% and the coupling length is 16 μm. When the gap increases to 150 nm and then to 200 nm, the peak coupling efficiency maintains around 90% while the coupling length elongates to 27 μm and 41 μm, respectively. As shown by the plot of coupling efficiency relative to wavelength in Fig. 6(b), the tolerance over wavelength significantly reduces as the gap between InP and Si enlarges. Compared with the design using "vertical ART" approach, the coupling efficiency exhibits a relatively small tolerance over the width variation of the Si strip waveguide. As shown by the plot in Fig. 6(c), the coupling efficiency decreases to around 30% when a 20 nm width variation is introduced into the strip waveguide. This sensitivity relates to the unique geometry of the Si-waveguides, where a small variation of the waveguide width induces a large change of the effective index of the fundamental TE mode and thus a significant deviation from the phase-match condition.

B. Butt Coupling

The ability to selectively grow InP segments on SOI promotes another straightforward coupling approach of butt-coupling. Fig. 7(a) outlines the butt coupling scheme of the Si rib waveguide and the InP segment grown on 220 nm SOI using the "vertical ART" method. Similar to the case in the evanescent couple scheme, we select the TE_{01} mode in the epitaxial InP and couple it into the fundamental TE mode inside the Si rib waveguide. Fig. 7(a) also includes the cross-sectional schematic along the waveguide direction and the mode profile inside the epitaxial InP and the Si rib waveguide. The height of the InP ridge and the Si rib waveguide is 800 nm and 220 nm, respectively, while the width is set as 500 nm. The thickness of the Si rib is kept as 50 nm. As expected, the mode overlap between the epitaxial InP ridge and the Si rib waveguide is quite limited, and, as a result, a maximum coupling efficiency of 43% is obtained when the gap is set as zero. As the gap gradually broadens to 300 nm, the coupling efficiency reduces accordingly to around 15% as shown in Fig. 7(b). Fig. 7(c) shows the coupling efficiency relative to the wavelength at a gap of 100 nm, 150 nm and 200 nm. In sharp contrast to the evanescent schemes, the coupling efficiency is insensitive to the wavelength variation and remains stable across the entire C-band.

Fig. 8(a) illustrates the butt coupling scheme of the Si strip waveguide and the InP segment grown on SOI using the "lateral ART" method. Same thickness of the epitaxial InP segment and the Si strip waveguide ensures an efficient light coupling into the Si strip waveguide while maintaining a guided fundamental mode for the fundamental TE mode in the InP. Fig. 8(a) also shows the cross-sectional schematic along the waveguide direction and the mode profile inside the epitaxial InP and the Si strip waveguide. In this embodiment, the height of the epitaxial InP and the Si waveguide segment is set as 480 nm and the width is chosen as 800 nm. As shown in Fig. 8(b), a maximum coupling efficiency of 99% can be obtained when set the gap as zero, and a high coupling efficiency of around 75% is still achieved when the gap increases to 100 nm. As the air gap increases, the mode from the III-V laser enlarges due to diffraction, and consequently light coupling into the Si-waveguide decreases due to mode mismatch. Fig. 8(c) plots the coupling efficiency versus wavelength of the guided mode. Similar to the butt coupling scheme using the "vertical ART" approach, the butt coupling efficiency of the "lateral ART" method is also not sensitive to the wavelength change.

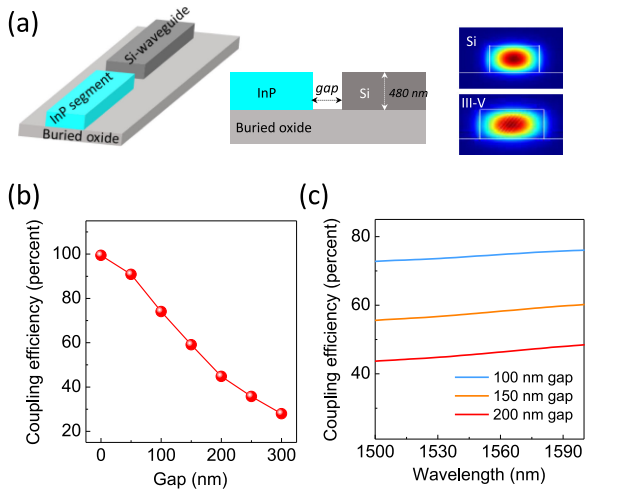

Fig. 8. (a) Butt-coupling strategy and cross-sectional view of III-V laser mode and Si waveguide mode for the "lateral ART" method. (b) Coupling efficiency versus coupling gap at 1550 nm. (c) Coupling efficiency as the function of wavelength at different coupling gap.

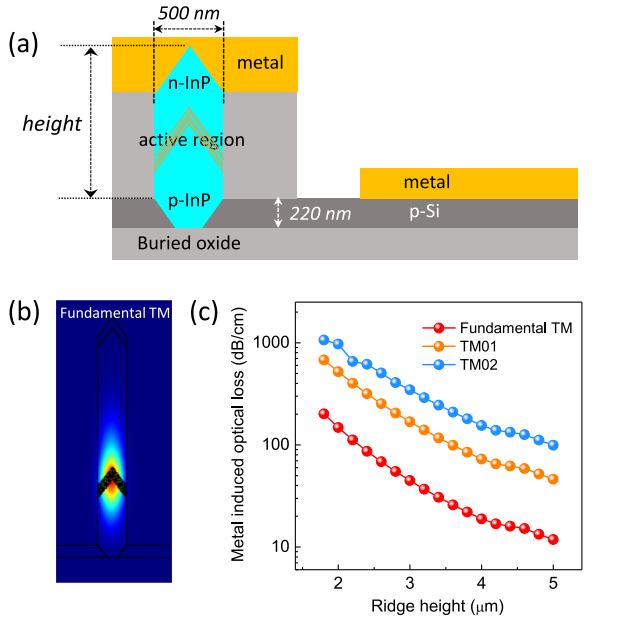

Fig. 9. (a) Schematic showing the design and simulation structure of electrically driven lasers grown on SOI using the "vertical ART" method. (b) Mode profile of the fundamental TM mode with a ridge height of 4.0 μm. (c) Calculated metal-induced propagation loss of the modes supported inside the InP waveguide.

IV. Towards Electrically Driven Lasers

Currently all lasers selectively grown on the industry-standard Si/SOI platform have been optically-pumped [14]–[22]. The challenge in realizing electrically driven devices mainly lies at patterning the metal contacts atop the nanometer-scale III-V alloys without inducing a large optical absorption loss. One direction is to exploit the unique photonic properties of metals to design and fabricate plasmonic lasers [51]. Another more straightforward solution is to obtain III-V materials with larger dimensions and subsequently separate the metal contacts from the guided optical modes. In this section, we investigate the possibility of employing InP selectively grown on SOI in realizing electrically driven lasers. We consider two integration schemes: vertical integration using the "vertical ART" method and lateral integration using the "lateral ART" approach.

A. Vertical Integration

Fig. 9(a) schematically depicts a structural design of the electrically driven laser grown on 220 nm SOI using the "vertical ART" method. The width of the epitaxial InP is set as 500 nm for efficient defect necking effect and wave-guiding at the 1550 nm band, and the height is defined as the distance between the InP tip and the Si device layer. The designed laser features a vertical configuration and can be doped into a p-i-n junction during the epitaxial process. The n-metal contact is placed right atop the n-InP, while the p-type contact is patterned on the Si-device layer which can be selectively doped using ion implantation. We have adopted such a structure to fabricate InP/InGaAs nano-ridge photodetectors directly grown on SOI [52]. Here, we focus on studying the metal-induced optical loss relative to the nano-ridge height for future electrically driven lasers on SOI. Fig. 9(c) plots the calculated values of three different modes, the fundamental TM mode, TM_{01} mode and TM_{02} mode, as the height of the epitaxial InP increases from 1.5 μm to 5.0 μm. As expected, the vertically elongated structure of the epitaxial InP support TM polarized modes (see Fig. 9(b)), while the TE polarized modes locate at the ridge bottom and the Si-device layer. The metal induced loss exponentially decreases as the height of the epitaxial InP increases. However, the value is still above 10 dB/cm when the nano-ridge height reaches 5.0 μm. The modal gain of InP/InGaAsP based telecom laser diodes is generally between 50–60 cm^{-1}, and the intrinsic loss falls between 10–20 cm^{-1} [53]. Although the mirror loss can be minimized through etching gratings or adopting a longer laser cavity, the metal induced loss in this configuration is still too large to attain low-threshold lasing behavior. Additionally, the TM polarization is not compatible with the commonly adopted TE polarization in Si-photonics. Also growing micrometer-high InP complicates the light interfacing with the underlying Si-waveguides and deprives the unique "bufferless" advantage of selective area growth. Another issue regards injecting charged carriers through the defective III-V/Si interface, which might induce high impedance and jeopardize the device performance.

B. Lateral Integration

Fig. 10(a) is a design of an electrically driven laser grown on SOI using the "lateral ART" growth method. In sharp contrast to the vertical integration scheme, the lateral configuration of the epitaxial InP right atop the buried oxide layer with lateral metal contacts enhances the fabrication flexibility. First flat [001]-oriented quantum structures can be regrown using the epitaxial InP as templates to favor the lasing of the fundamental TE mode. Also ridge structures can be formed to confine the guided modes at the central active region and consequently

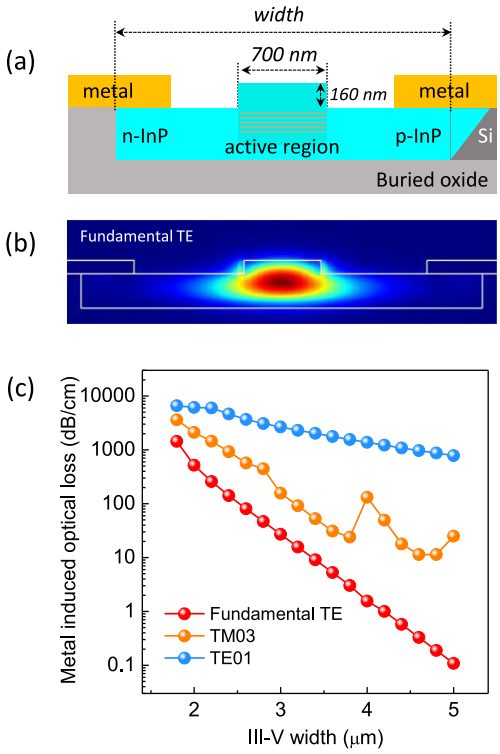

Fig. 10. (a) Schematic showing the design and simulation structure of electrically driven lasers grown on SOI using the "lateral ART" method. The flat (001)-oriented quantum wells are regrown on the InP /SOI templates. (b) Mode profile of the fundamental TE mode with an III-V width of 3.5 μm. (c) Calculated metal-induced propagation loss of the modes supported inside the InP waveguide.

minimize the optical absorption loss induced by the metal pads at both ends. In addition to doping the InP during epitaxial growth, we can also select ion implantation and thermal diffusion to obtain high quality p-i-n junctions [54], [55]. The lateral p-i-n configuration has been compared with its vertical counterpart, demonstrating comparable and even better performances [56], [57]. This configuration of InP on oxide also resembles that of III-V alloys bonded onto SOI, and accordingly may benefit from the laser designs and coupling strategies developed in the heterogeneous integration approach [10]. In the embodiment shown in Fig. 10(a), the height of the active region is 480 nm; the width of the ridge is 700 nm and the thickness of the doped InP is set as 320 nm; and the width of p-type and n-type metal contact is set as 500 nm. We calculated the metal induced optical loss through enlarging the distance between the etched ridge and metal contacts. Fig. 10(b) displays the mode profile of the fundamental TE mode when the InP width is set as 3.5 μm. Fig. 10(c) plots the evolution of the optical loss of three different guided modes relative to the total width of the epitaxial InP. The metal induced optical loss of the fundamental TE mode decreases exponentially with the InP width. And the value reduces to below 10 dB/cm when the InP width runs over 3.0 μm, and further decreases to below 1.0 dB/cm when the InP width exceeds 4.0 μm. This result highlights the great potential of realizing low-threshold electrically driven lasers

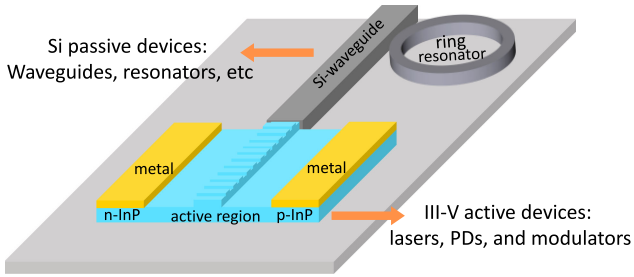

Fig. 11. Schematic illustrating the design of III-V active devices grown on SOI and seamlessly interfaced with Si-based passive components.

through selectively grown micrometer-scale InP materials on industry-standard SOI platforms.

This lateral integration scheme renders a unique co-planar configuration and intimate positioning of the epitaxial III-V active components with the Si-based passive elements. Together with the ability to grow InP stripes and segments, this integration strategy enables flexible and efficient light interfacing methods. Most significantly, the unique ability to grow micrometer-scale InP right atop the buried oxide layer points to the realization of the electrically driven lasers selectively grown on (001)-oriented SOI. Here, based on our above discussions, we envisage a fully integrated Si-based PIC as schematically depicted in Fig. 11. The micrometer-wide InP segments can be employed to fabricate a complete suite of III-V active devices including lasers, photodetectors and modulators, while the adjacent Si device layer could be tailored into waveguides, resonators, splitters and multiplexors. Light coupling between the co-planar III-V and Si can be achieved through either evanescent or butt coupling schemes. In addition, the efficient interfacing between the epitaxial III-V and Si-waveguides promotes the design and fabrication of ultra-high-performance hybrid devices that synergize the advantages of both material systems.

V. Conclusion

In conclusion, we presented a study of integration schemes of III-V devices with current Si-photonics platforms using selective area hetero-epitaxy. The "vertical and lateral ART" methods enable the direct epitaxy of bufferless and in-plane InP with flexible geometries and versatile dimensions on industry-standard SOI wafers. These selectively grown InP single crystal on SOI promote efficient light interfacing with Si-waveguides using both evanescent and butt coupling schemes. The ability to grow micrometer-scale InP right atop the buried oxide layer offers the potential of realizing electrically driven lasers directly grown on SOI and seamlessly integrated with Si-photonics. Our study here underscores the bright prospects of monolithically integrating III-V lasers with Si-photonics via selective hetero-epitaxy.

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