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Multi-heterojunction InAs/GaSb nano-ridges directly grown on (001) Si

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Abstract

We report on multi-stacked InAs/GaSb nano-ridges directly grown on (001) patterned Si substrates by metal-organic chemical vapor deposition (MOCVD). Uniform GaSb and InAs nano-ridges were demonstrated with optimized growth parameters. By adjusting the switching sequences, we also obtained defect-free InAs/GaSb and GaSb/InAs interfaces. Based on these fine-tuned growth conditions, multi-stacked InAs/GaSb nano-ridges were developed and characterized. The nano-ridges showed uniform morphology from scanning electron microscopy (SEM), and no observable crystalline defects were detected at the hetero-interfaces by transmission electron microscopy (TEM). These InAs/GaSb nano-ridges show great potential for applications in nano-scale tunneling devices and long wavelength light emitters and detectors. The demonstrated growth techniques provide helpful insights for the growth process control of 6.1 Å family compound semiconductors directly on Si by MOCVD.

Supplementary material for this article is available online

Keywords: InAs/GaSb nano-ridges, aspect ratio trapping, selective area epitaxy, 6.1 Å family compound semiconductor, metal-organic chemical vapor deposition

(Some figures may appear in colour only in the online journal)

1. Introduction

Tunneling field effect transistors (TEFTs) have been extensively studied due to their low drive voltage and steep subthreshold swing [1]. In particular, the InAs and III-Sb material system (the 6.1 Å family semiconductors) has been the focus of attention due to the broken gap band-alignment and resultant high tunneling current [2, 3]. The applications in long wavelength light emitters and detectors has further spurred the interest in these unique 6.1 Å family semiconductors [4–6]. However, most previous studies focused on the growth of vertical nanowires or thin films on native GaSb and GaAs substrates [7–10]. Direct hetero-epitaxy of high quality GaSb/InAs crystals and hetero-junctions on Si substrates could enjoy the economy of current Si foundries and bring additional functionalities to current Si-based optoelectronic integrated circuits [11–17]. The aspect ratio trapping (ART) growth technique has been widely studied in the hetero-epitaxy of GaAs and InP on Si [18–22], and has consequently produced nano-scale transistors, tunnel junctions and light emitters directly integrated on industry-standard (001) Si wafers [23–29]. Combining the ART method and the interfacial misfit (IMF) growth technique, GaSb and InAs nano-ridges have been grown on V-grooved Si with an ultra-thin GaAs wetting layer [14–16]. However, these as-grown nano-ridges, especially InAs, suffer from poor surface morphology [13, 15]. Additionally, the defect generation and suppression at the InAs/GaSb and GaSb/InAs interfaces of the nano-ridges has not been thoroughly investigated.

In this letter, we present the growth of multi-junction GaSb/InAs nano-ridges with excellent surface morphology and defect-free interfaces on (001) Si substrates using metal organic chemical vapor deposition (MOCVD). We found that the overall morphology of GaSb and InAs nano-ridges exhibits a strong dependence on the InAs growth rate and V/III ratio. Uniform nano-ridges were obtained through optimizing these two growth parameters, while a defect-free InAs/GaSb interface requires a set of specifically-designed growth parameters

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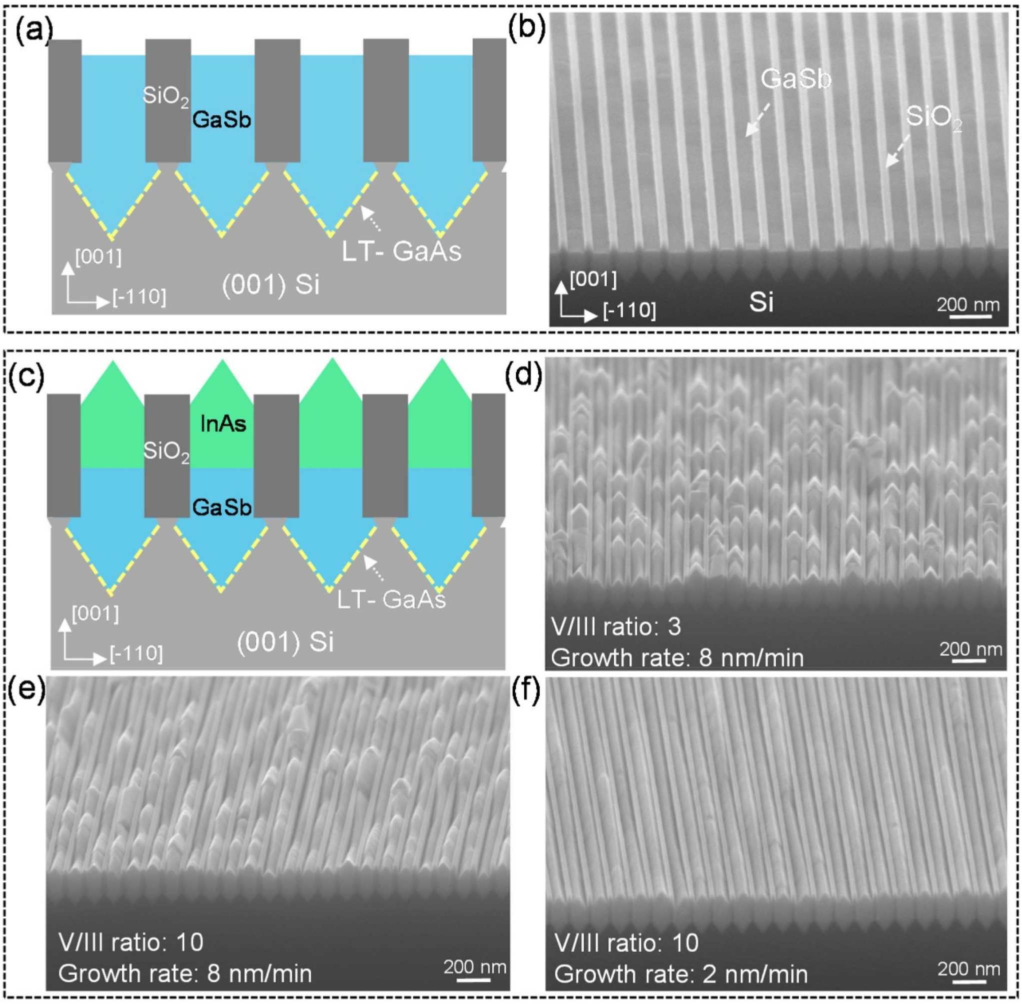

Figure 1. (a) Schematic diagram of GaSb nano-ridges grown on Si. (b) 70° tilted-view SEM image of GaSb nano-ridges. (c) Schematic diagram of InAs/GaSb hetero-structure nano-ridges grown on Si. (d)–(f) 70° tilted-view SEM image of InAs/GaSb nano-ridges with different growth conditions.

and switching sequences. The growth condition of defect-free GaSb/InAs interfaces, however, is much more lenient. Based on these optimized growth conditions, we then demonstrated the growth of four-stacked GaSb/InAs nano-ridges on Si. Our study therefore provides valuable insights for the epitaxy of defect-free 6.1 Å family semiconductors on (001) Si substrates.

2. Experimental details

The (001) Si wafers used in the experiments were patterned with [110]-oriented oxide stripes with 75 nm wide openings and a 130 nm pitch [19]. Preparation of the patterned Si substrates started with a brief HF dip to remove the native oxide on the initial (001)-oriented Si surfaces. A KOH-based anisotropic wet etching then followed to define the V-shaped pockets enclosed by (111)-oriented Si facets. Afterwards, the patterned Si substrate underwent a brief diluted-HCl bath and deionized water rinse before immediate transition into the reactor. We performed the hetero-epitaxy of InAs/GaSb nano-ridges on Si using a MOCVD system with a horizontal reactor (AIXTRON 200/4). Triethylgallium (TEGa) and trimethylindium (TMIn) were used as group III sources, with tertiarybutylarsine (TBAs) and trimethylantimony (TMSb) as group V sources. After a thermal cleaning process at 800 °C in a H_2 ambient, an ultra-thin GaAs disordered layer was deposited on the Si surface at 400 °C [21]. Then the reactor temperature was ramped to 500 °C for the growth of GaSb nano-ridges and subsequent InAs/GaSb hetero-structures.

The ultra-thin GaAs nucleation layer together with the IMF growth method produces GaSb nano-ridges with an excellent surface morphology inside nano-scale Si trenches, as evidenced by the scanning electron microscopy (SEM) photo in figure 1(b). Starting from the GaSb nano-ridges with (001)-oriented growth fronts, we then deposited InAs nano-ridges. As shown by the SEM image in figure 1(d), direct growth of InAs on GaSb results in severe deterioration of the surface morphology with the formation of InAs clusters. This behavior has also been observed by other researchers, however, has yet been successfully mitigated [13, 15]. The origin might relate to the large diffusion coefficient of the indium

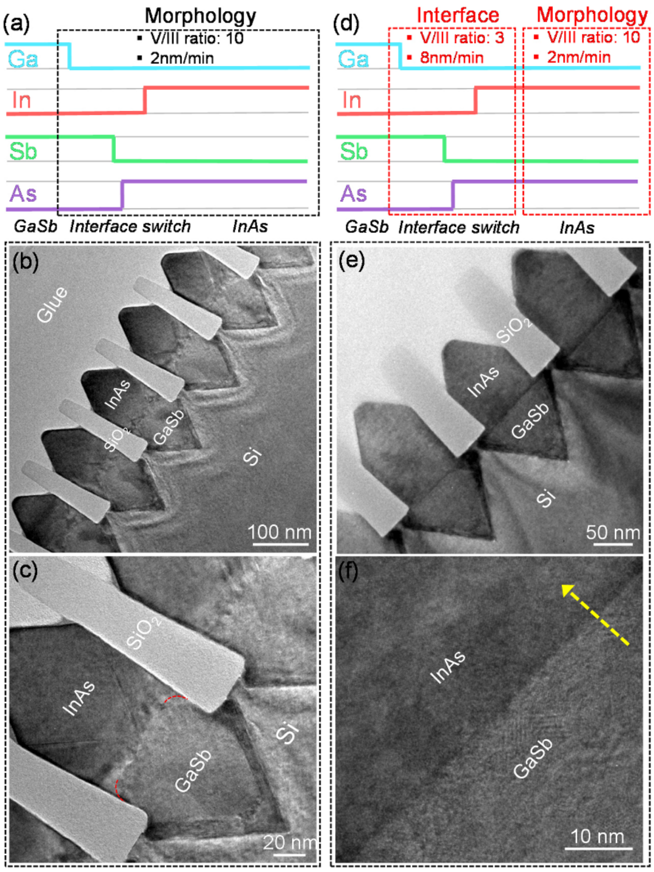

Figure 2. (a) Source switch sequence of InAs/GaSb heterojunction nano-ridges with one-step growth condition. (b) Global view cross-sectional TEM image of the InAs/GaSb nano-ridges with one-step growth. (c) Zoomed-in TEM image of the InAs/GaSb hetero-interface. (d) Source switch sequence of InAs/GaSb heterojunction nanoridges with two-step growth. (e) Global view cross-sectional TEM image of the InAs/GaSb nano-ridges with two-step growth. (f) Zoomed-in TEM image of the InAs/GaSb hetero-interface. The yellow arrow indicates the growth direction.

adatoms [30]. We found that the density and height of the surface bumps decreases when increasing the V/III ratio from 3 to 10 (see the SEM photo in figure 1(e)). We speculate that, with a high V/III ratio of 10, an increased number of arsenic adatoms were introduced to growth surfaces, capturing the diffused indium adatoms more quickly before they migrated to the bumps. It is well known for years that As and P alloys need to be grown at much higher V–III ratio than Sb compounds because As and P are much volatile and needs the over pressure. Similar smoothing effect can be achieved by significant reduction in the growth rate of InAs from 8 nm min^{-1} to 2 nm min^{-1}. The reduced growth rate could provide more time for the deposited InAs to evolve into stable nano-ridge structures with minimum surface energies [31]. Continuous InAs nano-ridges with excellent morphology form when simultaneously adopting a high V/III ratio of 10 and a low growth rate of 2 nm min^{-1} (figure 1(f)). In contrast to the (001) growth front of GaSb nano-ridges, the above InAs nano-ridges exhibit a convex growth front with two (111) facets. The non-planar growth front stems from the tendency to minimize the total surface energy during the epitaxy process, and has also been observed from other III–V nano-ridge structures such as GaAs and InP [19, 32].

3. Results and discussion

Broken band gap naturally forms from the slightly mismatched InAs/GaSb hetero-structure. As a result, various broken band alignments were designed and realized by researchers, and have been applied to tunneling devices as well as optoelectronic devices with cascaded active regions [4–6, 33, 34]. However, most of the epitaxy work was performed by molecular beam epitaxy (MBE), and an 'InSb'-like interface was used by most MBE researchers to manage the strain from the 0.62% lattice mismatch between the InAs and GaSb while avoiding the 'GaAs'-like interface [35, 36]. In contrast, ternary alloy interfaces have been adopted by most MOCVD researchers due to the incompatibility between the low melting point of InSb (535 °C) and the MOCVD growth temperature [37–40]. Lutzi *et al* also reported that low temperature growth could reduce the dislocation generation at the InAs/GaSb interface [9]. Our previous study of source switch sequence in combination with growth temperature demonstrated the effectiveness of 'GaAsSb' interface and the need to employ a low growth temperature [15]. Here, we further discovered that the interface growth rate and V/III ratio also have a significant effect on the defect generation and suppression at the InAs/GaSb hetero-interface. The InAs/GaSb source switch sequence used here is illustrated in figure 2(a).

We then grew InAs on GaSb nano-ridges using the optimized parameters for the surface morphology described in figure 1(f) and our previously demonstrated switching sequences for a defect-free hetero-interface [15]. However, a high density of threading dislocations (TDs) and stacking faults (SFs) was generated at the hetero-interface of each nano-ridge, as evidenced by the cross-sectional TEM image in figure 2(b), which indicates the incompatibility between the epitaxial parameters for uniform morphology and the growth conditions for a defect-free interface. Figure 2(c) shows a zoomed-in TEM image of the hetero-interface of one nano-ridge. Two (111)-plane SFs appear at the InAs/GaSb interface and propagate upwards until trapped by the oxide sidewall. Note that the GaSb buffer evolves into a rounded growth front during the switching process (guided with red lines in figure 2(c)), which furthers complicates the growth of defect-free hetero-junctions. The defective interface might relate to the Ga carryover effect and As-for-Sb swap effect [9, 37, 41, 42]. The Ga carryover effect refers to the methyl-exchange reaction between Ga and TMIn due to the stronger bond energy of the Ga-C bond than that of In-C, and the As-for-Sb swap corresponds to the Sb exchange with the incoming As reactant to form the more stable Ga-As bond [9, 41]. It indicates the incompatibility between the epitaxial parameters for uniform morphology and the growth conditions for a sharp and clean interface. In order to simultaneously obtain a uniform morphology and clean interfaces, we designed a two-step growth method (figure 2(d)). We first grew a thin

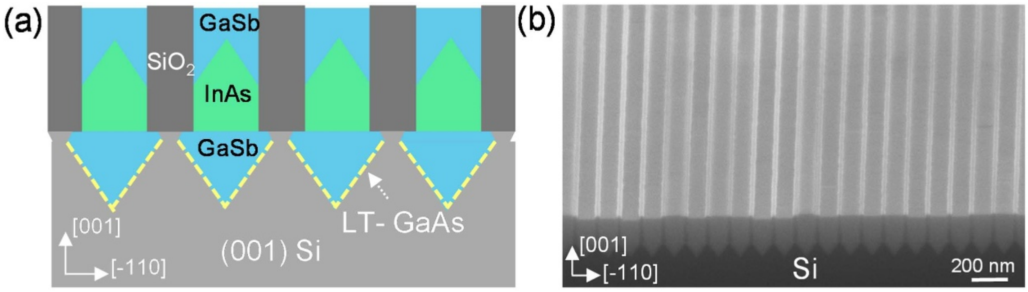

Figure 3. (a) Schematic diagram of GaSb/InAs/GaSb double hetero-junction nano-ridges grown on Si. (b) 70° tilted-view SEM image of GaSb/InAs/GaSb nano-ridges showing uniform morphology.

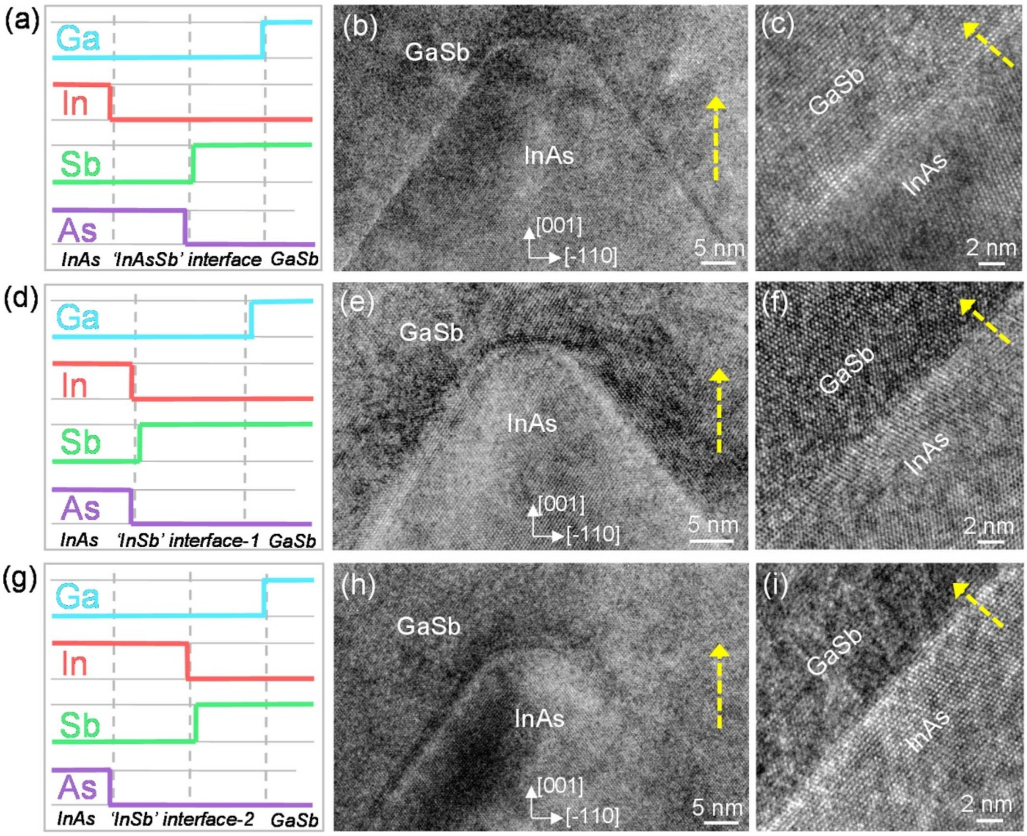

Figure 4. Source switch sequence of the (a) 'InAsSb' interface, (d) 'InSb' interface-1 and (g) 'InSb' interface-2. (b), (e) and (h) show cross-sectional TEM images of the GaSb/InAs hetero-interface with different source switch sequences. The yellow arrow indicates the growth direction. (c), (f) and (i) are zoomed-in TEM images of the GaSb/InAs hetero-interface. The yellow arrow indicates the growth directions.

layer of InAs to obtain a sharp InAs/GaSb interface and then switches to a lower growth rate to obtain a uniform InAs morphology. Employing an increased growth rate of 8 nm min^{-1} and decreased V/III ratio of 3, we firstly aim at minimizing the Ga carryover and As-for-Sb swap effect, thus achieving a sharp hetero-interface [15]. With a low InAs growth rate of 2 nm min^{-1} (see figure 2(a)), it would take a longer time for InAs to fully cover the bottom GaSb surface. Before the GaSb was fully buried underneath, it was exposed to the precursor ambient of InAs, which increases the possibility of the InAs ambient to 'etch' the bottom GaSb (Ga-carryover and As-for-Sb exchange). Instead, a high growth rate of InAs covers the bottom GaSb surface more quickly, thus reduces the time of InAs to 'etch' GaSb. As for the influence of V/III ratio, we speculate that a low V/III ratio introduces less arsenic reactants to the GaSb growth surface and subsequently minimizes the As-for-Sb exchange. With an increased V/III ratio of 10 and decreased growth rate of 2 nm min^{-1}, the second step targets a uniform surface morphology as discussed in the previous section. The efficacy of our designed two-step growth process is evidenced by both SEM (not shown here) and TEM measurements. As indicated by the cross-sectional TEM image in figure 2(e), uniform InAs/GaSb nano-ridges were achieved with defect-free hetero-interfaces. The reduced GaSb thickness shown in figure 2(e) (compared with figure 2(b)) was a result of intentionally decreased growth time of the

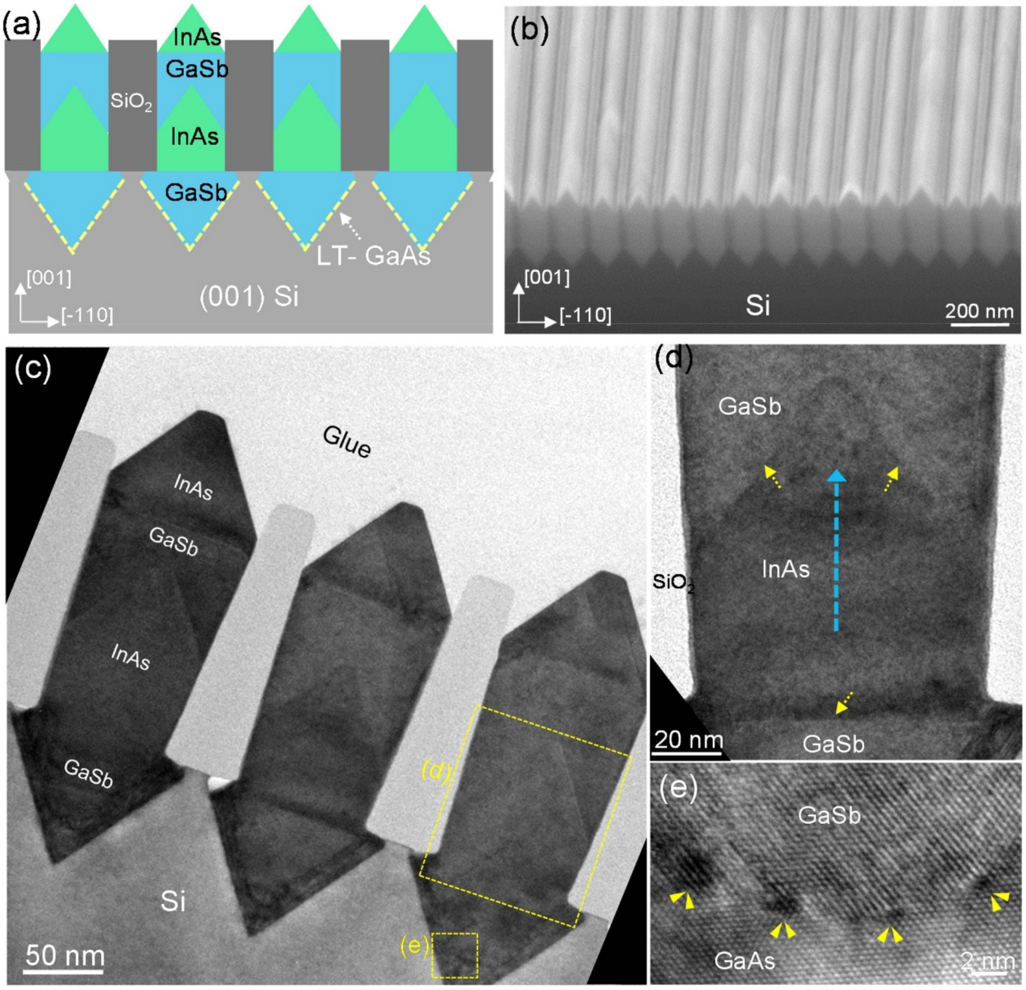

Figure 5. (a) Schematic diagram of the four-stacked InAs/GaSb nano-ridges grown on Si. (b) 70° tilted-view SEM image of the four-stacked nano-ridges. (c) Global view cross-sectional TEM image of the four-stacked nano-ridges showing good crystalline quality. (d) Zoomed-in TEM image to show the InAs/GaSb and GaSb/InAs hetero-interfaces. The blue arrow indicates the growth direction. (e) Zoomed-in TEM image at the GaAs/GaSb boundary.

GaSb-ridge. The optimized growth procedures shown in figure 2(d) allow GaSb to maintain a flat (001)-oriented growth front inside the oxide trenches regardless of the thickness and provides an identical (001)-oriented buffer for subsequent the InAs growth. Figure 2(f) displays a zoomed-in TEM image of the InAs/GaSb hetero-junction with a sharp (001)-oriented interface.

After optimizing the InAs/GaSb nano-ridges with excellent morphology and defect-free interfaces, we then moved to study the GaSb/InAs hetero-interfaces through growing double hetero-junction GaSb/InAs/GaSb nano-ridges, as shown by the schematic diagram in figure 3(a). Initializing the GaSb growth on InAs nano-ridges with two (111) facets produces GaSb nano-ridges with a flat (001) growth front, very similar to the case of the pure GaSb nano-ridges in figure 1(a). In contrast to InAs grown on GaSb nano-ridges with stringent requirements of the growth condition, uniform GaSb can be easily obtained atop the InAs ridge buffer without any meticulous tuning of the growth parameters. Additionally, the surface morphology of GaSb also improves, as attested by the disappearance of the surface textures (see figure 3(b)) compared to the InAs/GaSb nano-ridges in figure 1(f).

Figure 4 displays a systematic TEM study of the GaSb/InAs hetero-interfaces using different source switch sequences. We first adopted a similar switching sequence to that shown in figure 2 to form the 'GaAsSb' interface. As illustrated in figure 4(a), immediately after InAs growth the surface was exposed under a TBA flux to form an As-rich surface. Then the group V source was changed to TMSb to generate a nominal InAsSb alloyed interface. Finally, TEGa was introduced to start the GaSb growth. The GaSb/InAs interface was then inspected using TEM, as shown in figure 4(b). A sharp GaSb/InAs interface was formed without any interfacial intermixing phenomenon despite the growth on the multi-faceted InAs buffer. Figure 4(c) displays a zoomed-in TEM image of the hetero-interface and no visible dislocation can be found. We also adopted another two sets of source switch sequences of the 'InSb'-like interface, as illustrated in figures 4(d) and (g). In one 'InSb' interface, shown in figure 4(d), the TMIn and TBA flux were stopped immediately after the InAs growth.

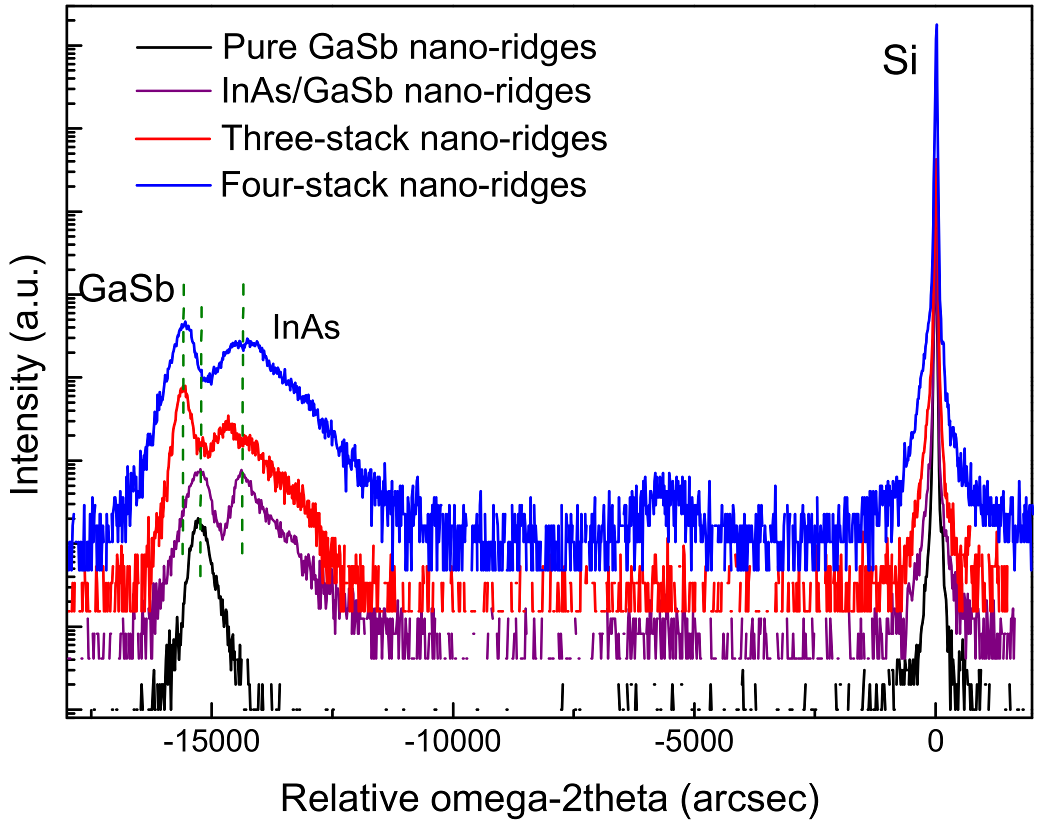

Figure 6. XRD omega-2theta relative scan of the optimized multi-stack InAs/GaSb nano-ridges.

Meanwhile, the TMSb flux was introduced to form the nominal 'InSb' interface. Then TEGa flux was opened to start the GaSb growth. For another 'InSb' interface, shown in figure 4(g), the TMIn flux after InAs growth was extended to form an indium-rich growth surface. Both of the 'InSb' interfaces were inspected using TEM. A sharp interface can always be observed no matter which source switch sequence was used (see figures 4(e) and (h)). Dislocations cannot be found in the zoomed-in TEM inspections, as shown in figures 4(f) and (i). Unlike the InAs/GaSb interface, the GaSb/InAs interface in the nano-trenches was not sensitive to the source switch sequence at all. A similar phenomenon was also observed in the planar GaSb/InAs thin film grown by other researchers [9]. As discussed previously, the growth difficulty of the InAs/GaSb interface comes from the Ga carryover effect and As-for-Sb swap process. However, if the growth sequence was inverted, both processes would be self-suppressed.

Up to this point, we were able to grow uniform GaSb and InAs nano-ridges as well as defect-free InAs/GaSb and GaSb/InAs hetero-interfaces. Building on these results, we then grew four-stacked InAs/GaSb nano-ridges inside the nano-scale Si trenches, as shown in the schematic diagram of figure 5(a). The four-stacked InAs/GaSb heterostructures exhibit an excellent surface morphology with a convex growth front, as evidenced by the SEM image of figure 5(b). We also performed cross-sectional TEM to study the multi-stacked nano-ridges. One representative TEM photo is displayed in figure 5(c). Most of the crystalline defects are confined within the bottom V-grooved pocket (see the dark area at the III–V/Si interface). Figure 5(e), displaying a TEM photo of the GaAs/GaSb boundary, reveals even-spaced interfacial misfit (IMF) dislocations. Using the optimized growth parameters of InAs/GaSb and GaSb/InAs interfaces, as discussed in figures 2(f) and 4, three defect-free hetero-interfaces were sequentially obtained. Figure 5(d) displays a zoomed-in TEM image of the bottom InAs layer sandwiched between two GaSb layers, manifesting the sharp and defect-free (001) InAs/GaSb interface and (111) GaSb/InAs interfaces. We fabricated tunnel junctions using the four-stacked InAs/GaSb nano-ridges [25], and the details can be found in the supplementary materials (available online at: stacks.iop.org/Nano/31/345707/mmedia).

X-ray diffraction (XRD) characterization was performed to characterize the as-grown nano-ridges using an Empyrean PANalytical system operating at 40 kV and 40 mA. Figure 6 shows the omega-2theta curve of the four different nano-ridges, namely pure GaSb nano-ridges, InAs/GaSb nano-ridges, three-stacked GaSb/InAs/GaSb nano-ridges and four-stacked InAs/GaSb/InAs/GaSb nano-ridges. A single GaSb peak was identified in the scan of the pure GaSb nano-ridge, as shown by the black curve. In the scan of the InAs/GaSb nano-ridges, both the InAs and GaSb peaks were identified, and the GaSb peak was aligned to the peak of the pure GaSb nano-ridges. In the three- and four-stacked nano-ridges, the two GaSb peaks were perfectly aligned but become misaligned with that of the pure GaSb and InAs/GaSb nano-ridges. The difference in the peak position stems from the different position of the GaSb layer and resultant different partial strain relaxation. A similar phenomenon is also observed for the peaks of the InAs.

4. Conclusion

In conclusion, we have demonstrated the growth of multi-stacked InAs/GaSb nano-ridges with excellent surface morphology and defect-free hetero-interfaces on exact (001) Si substrates by MOCVD. By reducing the growth rate and increasing the V/III ratio, we were able to grow uniform InAs nano-ridges on the GaSb buffer layer. We also optimized the growth parameters for both the InAs/GaSb and GaSb/InAs hetero-interfaces and thereby enabled the formation of defect-free hetero-interfaces. Building on these results, we then demonstrated the growth of three and four-stacked nano-ridges inside nano-scale Si trenches while maintaining the uniform morphology and defect-free interfaces. Future efforts include design and demonstration of nano-electronic devices such as tunnel junctions and TFETs using the multi-stacked InAs/GaSb nano-ridges. Additionally, growing InAs/GaSb nano-ridges inside sub-micrometer trenches could enable infrared light emitters and detectors for integrated nano-photonics. Therefore, the optimized epitaxy method offers helpful guidance in the MOCVD grown 6.1 Å family compound semiconductors. The well-developed InAs/GaSb nano-ridges here show great potential for applications in III–V nano-scale optoelectronic devices monolithically integrated on industry-standard (001) Si substrates.

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