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Bufferless III–V photodetectors directly grown on (001) silicon-on-insulators

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Efficient photodetectors (PDs) and lasers are critical components in silicon photonics technology. Here, we demonstrate bufferless InP/InGaAs PDs, directly grown on (001) silicon-on-insulators. The nano-scale PDs exhibit a high photoresponsivity of 1.06 A/W at 1.55 μm, and a wide operating range from 1450 nm to 1650 nm. The bufferless feature of nano-PDs facilitates effective interfacing with Si waveguides, thus paving the path toward fully integrated silicon photonics circuits.

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As the demand for energy-efficient data communications continues to increase exponentially, optical interconnects are becoming more prevalent for shorter-reach data communications because of their bandwidth and energy efficiency advantages over electrical interconnects [1]. In particular, silicon (Si) photonics has risen to meet this demand due to its inherent low-cost and high-volume manufacturing processes built on mature complementary metal oxide semiconductor (CMOS) fabrication technologies. A Si-based photonic integrated circuit (PIC) comprises laser sources, waveguides, modulators, and photo detectors (PDs) [2–4]. While Si is a superb material for light transmission and manipulation in the telecom band, its indirect band gap and transparency beyond 1100 nm preclude its application in efficient light generation and detection. Tremendous effort and progress have been made to include III–V compounds on the silicon-on-insulators (SOI) platform for light generation via either wafer bonding or direct hetero-epitaxy. Germanium (Ge) direct hetero-epitaxy developed for SiGe technologies in electronics has been used on SOI for light detection. Ge has strong absorption in the telecom wavelength range and is compatible with the CMOS process [5], but Ge-based PDs usually contain high dislocation densities leading to large dark currents [6,7]. As an alternative, III–V-based PDs on Si can offer much lower dislocation densities and smaller dark currents [8]. In addition, the ease of introducing low-dimensional quantum structures and bandgap engineering offer more design flexibility to III–V PDs and potentially better device performances [9]. The integration of III–V PDs on Si can be realized by both epitaxial growth and wafer/die bonding. Although the heterogeneous bonding technique delivers excellent device performances [10–13], the monolithic hetero-epitaxy method offers advantages of potentially lower cost and higher integration density [14]. Both III–V laser diodes and PDs have been integrated on Si by means of growing III–V thin films on Si, exploiting quantum dots as the active medium [15,16]. These direct hetero-epitaxial PDs showcase low dark currents and high sensitivities, with values comparable to these grown on native substrates [15]. However, the thick buffer layer required for defect reduction in the thin-film approach impedes effective interfacing between the epitaxial PDs and the Si waveguides. Besides, most reported III–V PDs on Si built on the GaAs material system for the 1.3 μm band. Employing the InP material system and expanding the detection wavelength to the 1.5 μm band and beyond could greatly enhance the circuit bandwidth and functionality.

In contrast to blanket epitaxy of III–V thin films on Si with thick buffer layers, dislocation-free and bufferless III–V compounds, including GaAs, InP, InAs, and GaSb, can be selectively grown on pre-patterned Si substrates [17–19]. Room temperature lasing has been demonstrated from these selectively grown III–V alloys in both the 1.3 μm and 1.5 μm bands [17,20], and efficient light coupling into Si waveguides has been designed on the SOI platform [21]. Here, building from our previously demonstrated InP/InGaAs nano-ridge lasers grown on (001) SOI [22], we present the design and integration of bufferless InP/InGaAs nano-ridge PDs on SOI for on-chip light detection in the 1.5 μm band. To accommodate electrical bias, we applied $p+$ doping to the InP/InGaAs nano-ridges grown on SOI to form PIN junctions. Metal contacts are patterned atop the $n+-$InP and the $p+-$Si device layer. The fabricated nano-ridge PDs exhibit a high responsivity over a 200 nm spectral range covering the E band, C band, and L band, and feature a responsivity of ∼1.06 A/W at 1.55 μm. Direct growth of these bufferless III–V PDs on (001) SOI facilitates the integration with other Si-based photonic components and points to a fully integrated Si-based PIC attainable in the near future.

Figure 1(a) schematically depicts the architecture of the designed nano-ridge PD grown on (001) SOI. The devised PD builds on the PIN III–V nano-ridge structures grown on a highly doped $p+-$Si device layer [see Fig. 1(b)]. According

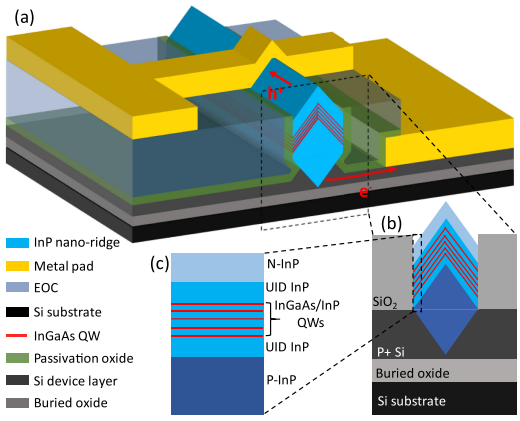

Fig. 1. (a) Device architecture of the designed bufferless InP/InGaAs PD grown on SOI. (b) Cross-sectional view of the as-grown structure. (c) Zoomed-in schematic showing the growth details.

to the growth sequence, the PIN III–V nano-ridge consists of a 700-nm-thick heavily doped p-InP buffer, five InP/InGaAs ridge quantum wells (6-nm-thick InGaAs and 25-nm-thick InP spacer), sandwiched between two 50-nm-thick unintentionally doped InP layers, and a 100-nm-thick heavily doped n+-InP layer, as illustrated by the cross-sectional schematic in Fig. 1(c). We adopted zinc as the p-type dopant and Si as the n-type dopant. The electron and hole densities of the heavily doped InP were estimated to be $6.2 \times 10^{18}/\text{cm}^3$ and $2.4 \times 10^{18}/\text{cm}^3$, respectively, according to Hall measurements of InP calibration thin films grown on planar semi-insulating InP wafers under identical growth conditions. The n-metal pad is patterned on top of the $n+-$InP layer, and the p-metal pad is formed atop the $p+-$Si device layer. The photo-generated electrons and holes are separated by the built-in electric field within the undoped regions and are collected by the two metal contacts [see Fig. 1(a)]. The positioning of the metal pads ensures a strong light absorption inside the III–V nano-ridge, and it minimizes the unwanted photon absorption of the metal.

The InP/InGaAs nano-ridges in this work were grown on patterned, thinned, and doped (001)-oriented SOI substrate, as illustrated in Fig. 2. The initial SOI substrate features a $1.5 \pm 0.08 -$ μm-thick silicon device layer, which was subsequently thinned down to 625 nm using a cycled thermal oxidation and buffered oxide etching process. Then the Si device layer was p-doped using ion implantation to facilitate the formation of ohmic contacts. Given that the Si device layer will be further thinned down in the following process to minimize light leakage, the doping depth must be well adjusted for minimal contact resistance. The thinned SOI was p-doped by implanting boron into the silicon device layer with a dose of 1×10^{16} cm^3 and an energy of 180 keV, corresponding to a doping depth of around 300 nm. Next, a 500-nm-thick thermal oxide was grown on the doped SOI at 1100°C to serve as the mask in the subsequent pattern fabrication and simultaneously activate the p-type dopant. Factors taken into consideration were the implant distribution and diffusion of the dopants, and the consumption of Si during oxidation. The peak doping concentration is estimated to locate at around 100 nm below the Si-oxide interface. Afterwards, [110]-oriented oxide trenches were patterned on the processed SOI wafer with a trench width of 500 nm and a pitch of 2.8 μm. V-grooved pockets were then formed using KOH-based selective wet etching. We grew the InP/InGaAs nano-ridges inside the patterned oxide trenches using a metalorganic chemical vapor deposition (MOCVD) system (AIXTRON 200/4) with a horizontal reactor. In our design, crystalline defects induced by lattice mismatch are mainly confined at the III–V/Si interface, enabling InP nano-ridges on SOI with excellent crystalline quality. The detailed growth procedures can be found in Ref. [23–25]. Figure 2(b) presents a tilted-view scanning electron microscopy (SEM) image of the as-grown InP/InGaAs nano-ridges on SOI, and Fig. 2(c) shows the room temperature photoluminescence spectrum with a peak at 1550 nm.

Figure 3(a) shows the fabrication process of the designed nano-ridge PD on SOI. To begin, a 500-nm-thick oxide mask was deposited on the as-grown sample by plasma-enhanced chemical vapor deposition (PECVD). We defined the device nano-ridge by photolithography and patterned the oxide mask using reactive-ion etching. Then we removed other nano-ridges without oxide protection using inductively coupled plasma (ICP) etching to eliminate any electrical crosstalk and maintain adequate area for the probing metal pads. After that, we etched away the remaining oxide using a buffered oxide etcher (BOE) and undercut the Si device layer using KOH-based wet solutions. To ensure both a strong light confinement inside the nano-ridge and a low-contact resistance at the p-Si, the thickness of the Si device layer was left at 250 nm. After p-metal deposition (40 nm Ti/200 nm Al), a 40-nm-thick atomic-layer (ALD) Al_2O_3 together with a 200-nm-thick PECVD oxide

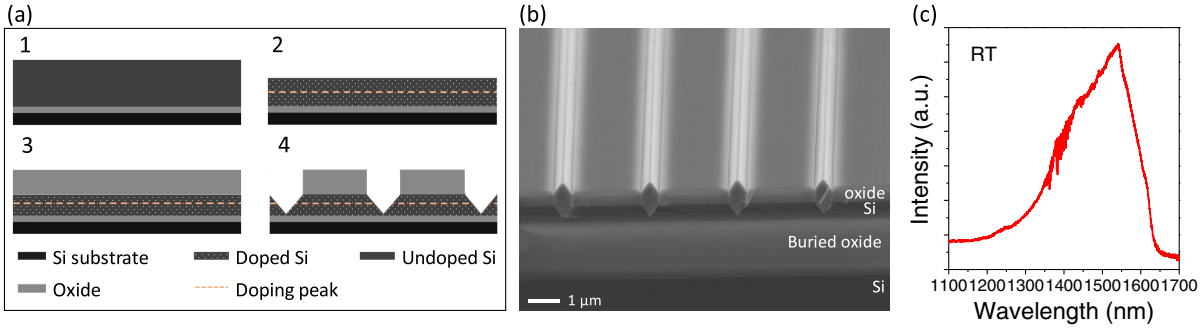

Fig. 2. (a) Thinning, doping, and patterning process of the SOI wafer for nano-ridge PD growth. (b) Tilted-view SEM photo of the as-grown InP/InGaAs nano-ridges on doped and patterned SOI. (c) Room temperature photoluminescence spectra of the as-grown InP/InGaAs nano-ridges with the peak at 1550 nm.

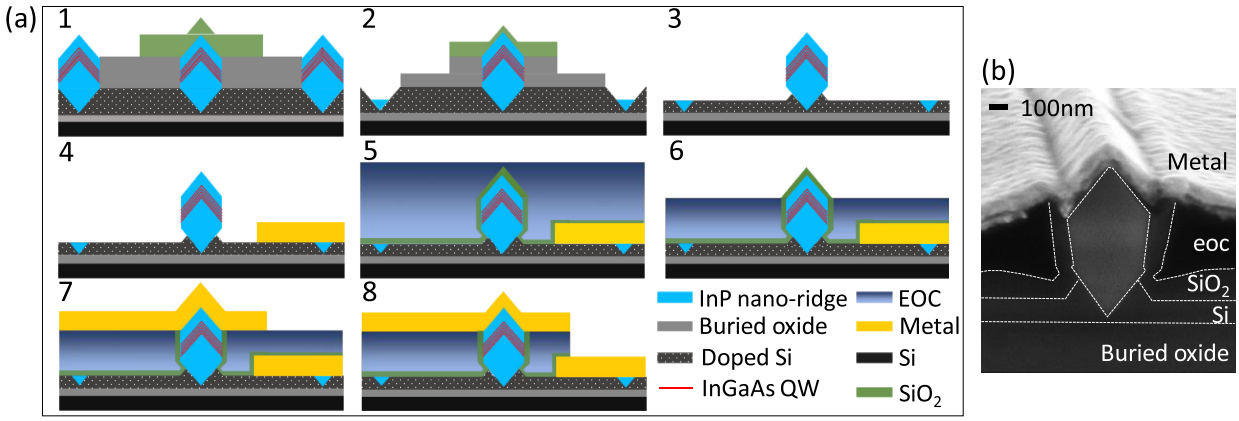

Fig. 3. (a) Fabrication steps of the PD directly grown on SOI in cross-sectional view with a detailed Si undercut and EOC coating and etch-back process. (b) 70° tilted-view SEM of the PD after the final fabrication step with dash lines at boundaries.

were grown as a passivation layer. Afterwards, a 1.2-μm-thick 2,2-bis (hydroxy methyl)-1-butanol (EOC) layer was coated and cured as planarization material and then was etched back to the nano-ridge tip for the following n-metal deposition. As a result of the planar and smooth morphology of the EOC layer together with the uniform nano-ridge height, the depth of the etch-back process can be precisely controlled. After the EOC etch-back, the oxide on top of the InP tip was removed by dry etching. The ohmic contact on the *n*-InP was achieved by evaporating 40 nm Ge/40 nm Au/24 nm Ni/200 nm Au on the nano-ridge tip and annealing for 2 min in a nitrogen ambient. The length of the n-metal defines the device area, with different device lengths from 5 μm to 115 μm fabricated. Finally, using the as-formed *n*-metals as the self-aligned mask, we etched away the EOC and the oxide layer atop the p-metal pads. Note that, despite the sub-wavelength scale of the nano-ridge PDs, the entire process was completed using conventional photolithography without any E-beam lithography process involved. Figure 3(b) displays a 70° tilted-view SEM image of the finished nano-ridge PD, revealing an excellent match between the actual device structure and our initial design.

The fabricated III–V nano-ridge PDs on SOI exhibit a typical diode current-voltage (I–V) characteristic with a turn-on voltage of around 0.7 V, and stable currents under reverse bias as shown in Fig. 4(a). The relatively high contact resistance was mainly a result of the small contact area between the n-metal and n-InP. The zoomed-in dark current without light illumination and photocurrent under the 21 μW input light at 1.5 μm are shown in the inset of Fig. 4(a). Under a −0.5 V bias, the dark current is 16 nA for the device with 75 μm in length, corresponding to a current density of 33 mA/cm^2. A tunable laser (from 1450 nm to 1650 nm) provides the measurement light source, and a source-meter measures the photo-generated current. The PD under test was biased at −0.5 V. Excitation light was coupled into the nano-ridge PD with a single-mode fiber with a core diameter of 9.0 μm. The fiber output end was placed several microns above the PD with an angle of around 78°, and the position was carefully tuned for an optimal coupling. An inline power meter with a 0.7 dBm insertion loss was placed between the laser source and nano-ridge PD to monitor the power of the incident light.

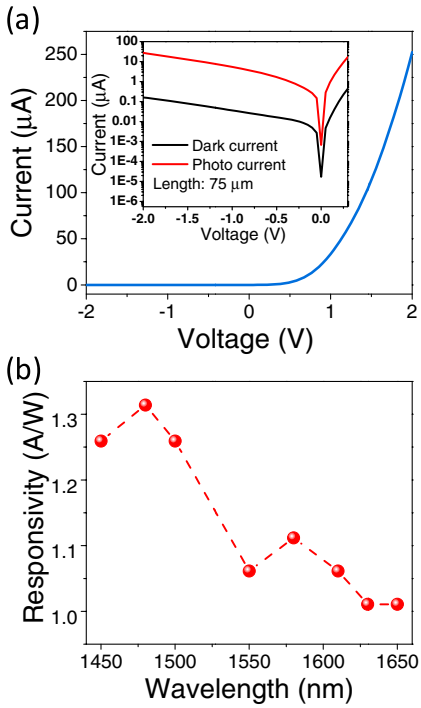

Fig. 4. (a) I–V curve of the PD, 500 nm wide and 75 μm long. Inset: zoomed-in dark current and photocurrent in log scale. (b) Evolution of responsivity plotted as the function of probing wavelength.

The responsivity was calculated by dividing the photocurrent by the incident optical power coupled into the nano-ridge. The laser excitation power was 0.5 mW. To obtain an estimation of the incident power on the device, the size ratio of ∼ 6% between the nano-ridge PD (500 nm wide) and the excitation laser spot (9 μm in diameter) was taken into consideration. Then we simulated the reflection of the InP upper cladding using finite-difference time-domain (FDTD) solver and obtained a value of 33.4% at 1.55 μm. With a scaled incident power of 21 μW, the responsivity is thereby calculated to be around 1.06 A/W with the measured photocurrent of 22.2 μA at 1.55 μm. Table 1 compares the results in this work with those in the literature.

Table 1. Comparison of PDs on Si Reported in the Literature

Type	Responsivity (A/W)	Dark Current (nA)	Photo-to-Dark Current Ratio
This work	1.06	16 (33 mA/cm^2)	153
Ge on Si [6]	0.037	35 (27 mA/cm^2)	40
Ge on Si [7]	0.16	10	500
InGaAs/InP on Si [8]	0.43	10 (0.8 mA/cm^2)	—
InGaAs/InP on Si [9]	0.5	200	10–100

We attribute the high sensitivity to the enhanced light confinement in the nano-ridge structure and resultant efficient optical-electrical conversion. As indicated by the broadband PL spectra in Fig. 2(c), the fabricated InP/InGaAs PD showcases photo-response over a wide wavelength range. We measured the operation spectral range and the corresponding photosensitivity of the nano-ridge PDs and summarized the results in Fig. 4(b). The photocurrent of the probed PD varies from 20 μA to 27 μA over the 200-nm-wavelength range from 1450 nm to 1650 nm. The corresponding responsivity reaches a peak of 1.31 A/W at 1480 nm and gradually reduces to 1.01 A/W at 1650 nm. This operational wavelength range of the InP-based PD is more than two times wider than that of those based on the GaAs material system and is expected to extend to the 1300 nm band [15,26]. A rise time of 4 μs and a fall time of 7 μs were obtained for the nano-ridge PD, which is mainly limited by the large *n*-contact resistance.

In conclusion, we demonstrated bufferless III–V PDs directly grown on (001) SOI substrate with a high sensitivity of 1.06 A/W at 1.55 μm. The PIN InP/InGaAs PDs display a high responsivity over a 200 nm operating-wavelength range from the E band to the L band. Monolithic integration of the bufferless III–V PDs on SOI highlights the potential light interfacing with Si waveguides and points to a fully integrated Si-based photonic integrated circuits.

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