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ABSTRACT

Epitaxial growth of III–V lasers on the (001) Si platform is emerging as the ultimate integration strategy for low-cost, energy-efficient, and wafer-scale photonic integrated circuits. As the performance of laser diodes grown on III–V/Si compliant substrates develops toward commercialization, the issue of light interfacing between epitaxial III–V lasers and Si-based waveguides is becoming increasingly pressing. As an alternative, selective area growth produces buffer-less III–V lasers on Si and thereby intrinsically promotes efficient light coupling with Si-photonics. As the dimension of the selectively grown dislocation-free III–V crystals is often limited at the sub-wavelength scale, the main challenge lies at the realization of electrically driven lasers and, specifically, at how to pattern the metal contacts without inducing large optical absorption loss. In this Perspective, we provide a brief overview of the state-of-the-art III–V lasers selectively grown on the (001) Si platform and discuss the outlook of this integration approach with an emphasis on the prospects of achieving electrically driven devices. We focus on the unique advantages offered by selective hetero-epitaxy as well as the challenges and potential solutions toward practical applications.

I. INTRODUCTION

In a similar way to how Si-based microelectronics revolutionized our modern society 60 years ago, Si-photonics is now reshaping our daily lives with commercialized products in data/telecom communications and a variety of imminent applications including high-performance computing, sensing, lidar, quantum communication, and artificial intelligence.[1–6] This wide deployment of Si in photonic functionalities is enabled by the large refractive index difference and the high-quality interface between Si and SiO_2, as well as the high-volume and low-cost manufacturing infrastructures provided by the microelectronics foundries.[7] As illustrated by the schematic in Fig. 1, the Si/SiN/SiO_2/Ge material system provides superior wave-guiding for light with wavelengths spanning from the visible region all the way up to the long wavelength mid-infrared regions.[8,9] Yet, constructing functional photonic integrated circuits (PICs) requires efficient and compact light sources—an unachievable goal using indirect band-structured group IV materials despite years of intensive effort in modifying the band structures and implementing quantum size effects.[10] In contrast, group III–V compounds with direct bandgaps, such as GaAs, InP, and GaSb, along with their alloys, have long been adopted to fabricate lasers emitting in the visible and the near-infrared bands, and recent innovations in quantum cascade lasers (QCLs) and inter-band cascade lasers (ICLs) have extended the emission wavelengths to the mid- and long-infrared regions.[11,12] Intuitively, synergizing the unique properties and functionalities of group IV and group III–V materials is the key for high-performance PICs over a wide range of wavelengths. Indeed, the integration of III–V lasers onto the Si platform has evolved from the hybrid integration with off-chip coupling[13] to heterogeneous integration using bonding or transfer printing[14,15] and then to monolithic integration via direct hetero-epitaxy.[16,17] While the first two approaches have enjoyed commercial success, the last method represents the ultimate solution for efficient, scalable, and compact PICs and is now receiving intense research investigation from both the academia and the industry. The ultimate goal is to directly grow high-performance III–V lasers on industry-standard (001) Si/silicon-on-insulator (SOI) platforms, which are continuous-wave electrically driven and seamlessly integrated with Si-waveguides (WGs).

In this Perspective, we provide a brief overview of the selective hetero-epitaxy of III–V lasers on industry-standard (001) Si platforms and outline the major challenges and possible solutions toward fully integrated Si-based PICs. This paper is arranged as

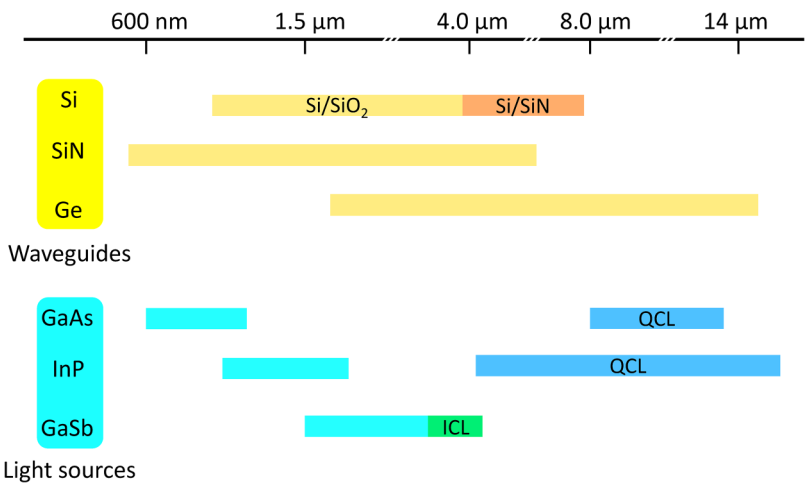

FIG. 1. Diagram showing the superior wave-guiding properties of $Si/SiO_2/SiN/Ge$ material system and the light emitting attributes of III–V compound semiconductors over a wide range of wavelengths.

follows. Section II compares the pros and cons of two different approaches of growing III–V lasers on Si: blanket hetero-epitaxy and selective hetero-epitaxy. We highlight their differences in terms of defect management, laser design, and light interfacing with Si-waveguides. Section III provides a brief review of current selective integration strategies, including aspect ratio trapping (ART), nano-ridge engineering (NRE), template assisted selective epitaxy (TASE), lateral aspect ratio trapping, conformal growth/corrugated epitaxial lateral overgrowth (CELOG), and some other interesting approaches. We emphasize the unique defect management techniques of each strategy and spotlight the resultant laser configurations and their implications for practical applications. Section IV elaborates on the prospects of selective hetero-epitaxy of III–V lasers on Si. This includes integrating a complete suite of III–V compounds on Si, downscaling the laser footprint, light interfacing with Si-photonics, and the future realization of continuous-wave and electrically driven lasers for practical applications.

II. BLANKET AND SELECTIVE HETERO-EPITAXY OF III–V LASERS ON SI

In general, direct hetero-epitaxy of III–V lasers on Si can be broadly classified into two directions: blanket epitaxy of III–V lasers on III–V/Si complaint substrates and selective epitaxy of III–V lasers on pre-patterned Si/SOI wafers. The main considerations of growing III–V lasers on Si usually consists of four inter-related issues: reduction or removal of crystalline defects generated from lattice, thermal and polarity mismatches between III–V and Si, the design and fabrication of III–V lasers directly grown on Si, reliability of the lasers, and the light interfacing between III–V active devices and Si-based passive components.[18] Figure 2(a) schematically illustrates the concept of blanket hetero-epitaxy of III–V lasers on Si. In this scenario, III–V thin films are uniformly deposited atop the Si wafers to construct III–V/Si compliant substrates using either metal organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE). Anti-phase boundaries (APB)

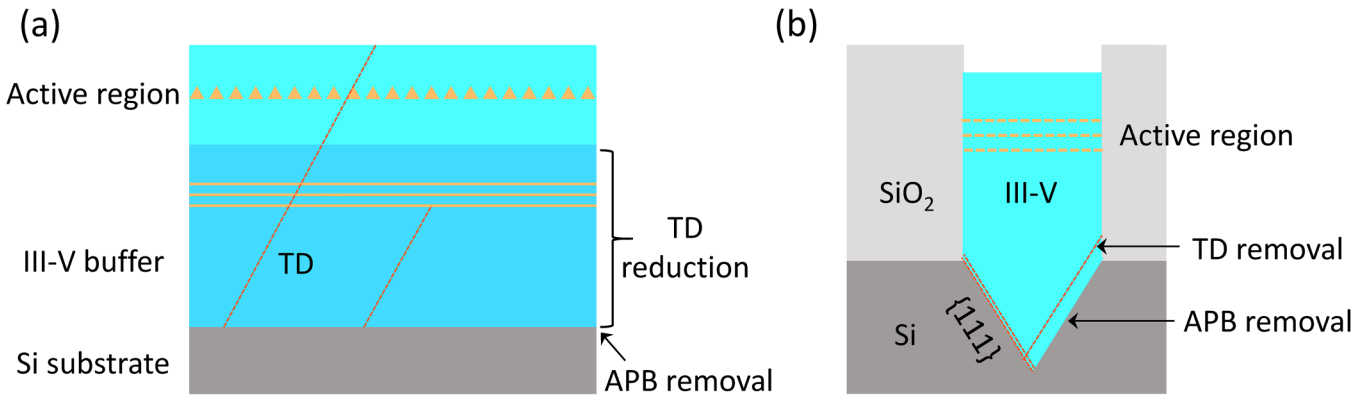

FIG. 2. (a) Schematic showing the integration of III–V lasers on Si via blanket hetero-epitaxy. (b) Schematic showing the integration of III–V lasers on Si via selective hetero-epitaxy. The red dotted lines denote the propagation and confinement of crystalline defects.

induced by polarity mismatch are eliminated at the III–V/Si interface through either careful surface treatment[19] or meticulous optimization of the nucleation conditions[20] or creating {111}-enclosed V-grooves.[21] The density of threading dislocations (TDs) induced by lattice mismatch is reduced through the introduction of thick buffer layers, the insertion of dislocation filters, and the incorporation of thermal cycle annealing;[22,23] and the TD density are in the order of 10^6 cm^{-2} for GaAs/Si templates,[24,25] 10^8 cm^{-2} for InP/Si templates,[26] and 10^7 cm^{-2} for GaSb/Si templates.[27] To avoid wafer bowing or crack from thermal mismatch, the thicknesses of the III–V buffers are kept to be no more than a few micrometers.[23] Building on these optimized III–V/Si templates, the design and fabrication of laser diodes follow the general procedures in conventional III–V photonics facilities, with the same general considerations and flexibility.[28] Currently, the performance of 1.3 μm GaAs-based quantum dot lasers is approaching those grown on native substrates,[16,25] while that of InP- and GaSb-based laser diodes emitting at longer wavelengths still lags behind their counterparts on native substrates.[27,29] The main challenge of this growth approach is the light interfacing between the upper III–V lasers and the bottom Si-waveguides, because the micrometer-thick III–V buffer layers are mandatory for defect reduction. Practical means of efficient light coupling is yet to be formulated. An abundance of review papers has been published regarding this growth approach, and the readers can refer to the listed references for detailed information.[16–18,29–32]

Figure 2(b) schematically delineates the selective hetero-epitaxy of III–V lasers on pre-patterned Si/SOI substrates. In this embodiment, III–V crystals are selectively deposited on pre-defined areas and the growth is usually guided by the growth mask or template.[33,34] MOCVD, with the provision of controlling the diffusion of precursors during growth, is thereby the dominant growth method in this case. In contrast to the bottom–up thin film growth in blanket epitaxy, selective epitaxy allows for additional flexibility in the growth of III–V materials on Si with regard to the growth direction,[35] material geometry/architecture,[36] and crystal phase.[37] APBs are normally eliminated through initiating growth from etched {111} Si surfaces.[38] Crystalline defects such as TDs and stacking faults (SFs) are confined within a thin layer (tens of nanometers) of III–V alloys due to the unique defect necking effect provided by the growth mask/template.[22] As a result, the epitaxial III–V alloys are in close proximity to the Si device layer, which inherently facilitates efficient light interfacing. Unlike the case of blanket hetero-epitaxy where the laser design is quite mature, laser design and fabrication using selective hetero-epitaxy hinges on the specific growth scheme and the resultant III–V geometry and dimension—a topic we will discuss in detail in Sec. III. Currently, room temperature lasing has been demonstrated from both GaAs- and InP-based devices with emission wavelength spanning across the entire near-infrared band.[39–51] However, these light emitters all require optical excitation, and realizing electrically driven devices will eventually provide more design options for on-chip integration.

III. SELECTIVE HETERO-EPITAXY OF III–V LASERS ON SILICON

In analogy to the case of Si where the application evolves from electronics to photonics, III–V crystals selectively grown on Si were initially developed to construct electronic devices for future logic applications and recently have been employed to fabricate lasers and photodetectors as the research on Si-photonics has been developing in the last decade.[52–59] Although there exist several different methods to selectively grow III–V crystals on Si, the central idea is to confine the crystalline defects generated from lattice mismatch at localized regions while the active region of the laser is constructed at low-TD or TD-free areas. To maintain sufficient gain from the as-grown III–V, the guided mode must be tightly confined within the epitaxial III–V crystals and light leakage into the Si substrate should be minimized. Aided by additional top–down processing, a variety of laser resonators including Fabry–Pérot lasers,[39,47–51] distributed feedback (DFB) lasers,[40–42,45] micro-disk, or ring lasers have been monolithically integrated onto the Si platform.[43,44,46] Table I lists the key metrics of these lasers in chronological order. In this section, we briefly review III–V lasers selectively grown on the (001)-oriented Si platforms, while the discussion of III–V nanowire and nano-pillar lasers grown on (111)-oriented Si wafers can be found elsewhere.[60–63]

A. Aspect ratio trapping

The aspect ratio trapping (ART) method enables the growth of III–V nano-ridges inside nano-scale V-grooved Si pockets environed by SiO_2 spacers,[33] with defects trapped in the lower part of the grooves. The creation of {111}-oriented V-grooved pockets [Fig. 3(a)] by anisotropic wet etching (e.g., potassium hydroxide and tetramethylammonium hydroxide) prohibits the formation of APBs.[23] In addition, initiating material deposition from {111}-oriented Si facets promotes strain relaxation via the formation of planar defects such as stacking faults and twins instead of more detrimental and propagating TDs [see the red dotted lines in Fig. 3(a)].[38] As a result, majority of the crystalline defects are confined right at the III–V/Si interface while most of the generated TDs would terminate at the oxide spacers [see the TEM photos of InP nano-ridge in Fig. 3(c)]. For stacking faults penetrating into the crystal, the ones parallel to the trench direction are trapped by the oxide spacers and those perpendicular to the trench often extend across the entire nano-ridge.[22] The symmetrical oxide spacers confine and guide the growth of the epitaxial III–V crystal, and nano-ridge structures with two convex {111} facets often form to minimize the total surface energy.[64–66] The width of the oxide opening is usually kept at around 500 nm for efficient wave-guiding at the telecom band and simultaneously maintaining an effective defect necking effect.[50] Figure 3(b) presents a tilted-view scanning electron microscopy (SEM) image of the III–V nano-ridge array selectively grown on (001)-oriented SOI wafers. These nano-ridges have been patterned across the entire wafer, and the spacing between adjacent nano-ridges can be varied from a few hundred nanometers to tens of micrometers.

In the literature, the ART approach is commonly adopted to grow InP-based lasers on Si. In the first place, growing InP inside V-grooved Si pockets favors strain relaxation via a highly twinned region at the InP/Si interface and thus enables the growth of active regions closer to the Si substrate. Also, InP can serve as a buffer layer for the growth of InGaAs-based quantum structures emitting in the technologically important 1.3 μm and 1.5 μm bands.[67–70] Using selectively grown InP nano-ridges, Wang *et al.* demonstrated a DFB

TABLE I. Key metrics of III–V lasers selectively grown on (001) Si/SOI platforms. All the demonstrated devices require pulse optical excitation (QW: quantum well, MQWs: multi-QWs, RT: room temperature, FP: Fabry–Pérot, DFB: distributed feedback, DBRs: distributed Bragg reflectors; ART: aspect ratio trapping; NRE: nano-ridge engineering; TASE: template assisted selective epitaxy).

Year	λ	Gain medium	Threshold	T	Cavity	Dimension	Growth scheme	Substrate	Reference
2013	880 nm	InP	1.69 pJ/pulse	RT	FP	Length: 1.4 μm diameter: 245 nm	ART	Si	39
2015	930 nm	InP	22 mW	RT	DFB	Length: 45 μm width: 500 nm	ART	Si	40
2016	1340 nm	InP/InGaAs QW	7.8 mW	RT	DFB	Length: 100 μm width: 500 nm	ART	Si	41
2017	1020 nm	GaAs/InGaAs MQWs	37 mW	RT	DFB	Length: 100 μm width: 364–530 nm	NRE	Si	42
2018	880 nm	GaAs	10 pJ/pulse	RT	Micro-disk	Diameter: 1–3 μm	TASE	Si	43
2018	1100 nm	InGaAs	2.6 pJ/pulse	200 K	Micro-disk	Diameter: 1.7 μm	TASE	SOI	44
2019	1020 nm	GaAs/InGaAs MQWs	10 kW/cm^2	RT	Loss-coupled DFB	Length: 300 μm width: 400 nm	NRE	Si	45
2019	860 nm	GaAs	10 pJ/pulse	RT	Micro-disk/ring	Diameter: 1.2 μm	TASE	SOI	46
2019	1373 nm	InP/InGaAs MQWs	300 W/cm^2	86 K	FP	Length: 200 μm width: 500 nm	ART	SOI	47
2019	1500 nm	InP/InGaAs MQWs	40 μJ/cm^2	RT	FP	Length: 50 μm width: 500 nm	ART	SOI	48
2019	1478 nm	InP/InGaAs MQWs	38 μJ/cm^2	RT	FP with DBRs	Length: 20 μm width: 500 nm	ART	SOI	49
2020	1500 nm	InP/InGaAs MQWs	20 μJ/cm^2	RT	FP	Length: 28 μm width: 500 nm	Lateral ART + ART	220 nm SOI	50
2020	845 nm	InP	58 μJ/cm^2	RT	FP	Length: 2.0 μm diameter: 500 nm	Surface kink assisted	Amorphous SiO_2	51

laser array emitting at around 920 nm in a 300 mm complementary-metal-oxide-semiconductor (CMOS) line [see the schematic in Fig. 3(d)].[40] In their work, the underlying Si substrate was selectively etched away to confine light within the epitaxial InP, and DFB gratings were fabricated atop the InP after smoothing the InP nano-ridge with chemical mechanical polishing (CMP). Room temperature single-mode lasing is thus obtained under optical excitation. Afterward, the same group extended the lasing wavelength from 920 nm to the 1.3 μm band by introducing a layer of InGaAs quantum well inside the polished InP.[41] Room temperature lasing behavior attests to the high quality of the epitaxial InP grown on Si, and processing the lasers in a CMOS pilot line proves the compatibility of this integration approach with the Si foundries. The InP nano-ridge can also be grown on (001) silicon-on-insulator (SOI) substrates for strong on-chip mode confinement and future light coupling into Si-waveguides. Han *et al.* demonstrated room temperature lasing at the 1.5 μm band through growing the InP nano-ridges on SOI wafers and embedding multiple InGaAs ridge quantum wells inside the InP [see the schematic in Fig. 3(e)].[48] The length of the lasers is around 50 μm (see Table I for the detailed device metrics). The authors then further shortened the length of the laser cavity down to 20 μm via etching distributed Bragg reflectors (DBR) at both ends[49] and later leveraged this ART growth technique to demonstrate 1.5 μm InP/InGaAs laser array grown on Si-photonics standard 220 nm SOI platforms.[50]

B. Nano-ridge engineering

When growing III–V materials from narrow oxide trenches using the ART method, TDs can be completely confined inside the oxide trenches benefiting from the high aspect ratio, while the enlarged III–V material outside the trench presumably can be rendered TD-free as shown by the schematic in Fig. 4(a) and the TEM image in Fig. 4(c). In addition, the shape of the III–V crystals outside the trench can be engineered by adjusting the growth conditions into a variety of different forms.[71] This nano-ridge engineering (NRE) method has been employed to grow GaAs and GaSb nano-ridge structures, and the TD density was measured to be in the order of 10^5 cm^{-2} when the trench opening is narrower than 100 nm.[22,72] However, there have been no reports of growing

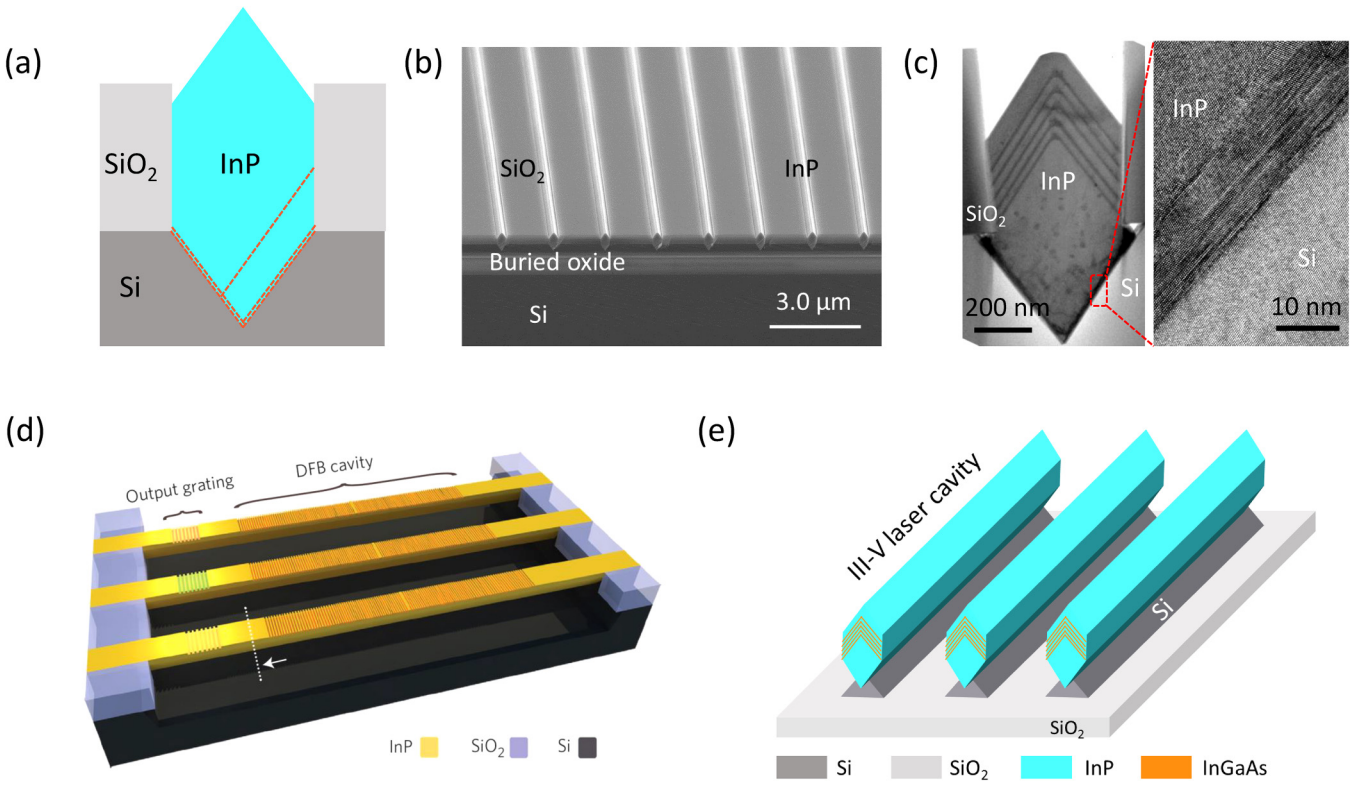

FIG. 3. (a) Schematic showing the growth of InP nano-ridges inside nano-scale oxide trenches via ART. The red dotted lines denote the confinement of the majority of crystalline defects at the InP/Si interface and the trapping of residual TDs at the SiO_2 sidewall. (b) Tilted-view SEM image of InP nano-ridge array grown on SOI grown by the ART method. (c) Cross-sectional TEM image of InP nano-ridge showing the formation of highly twined regions at the InP/Si interface. (d) 920 nm InP DFB laser array directly grown on Si substrates. The underlying Si is selectively etched away to confine light within the epitaxial InP. Adapted with permission from Wang *et al.*, Nat. Photonics **9**(12), 837–842 (2015). Copyright 2015 Spring Nature. (e) Telecom InP/InGaAs laser array directly grown on (001) SOI wafers.

InP nano-ridges using the NRE technique, possibly due to the difficulty in controlling the faceting of InP without the physical confinement of oxide spacers. Figure 4(b) displays a titled-view SEM photo of box-shaped GaAs nano-ridges grown on Si using the NRE technique.[36] The air-cladded GaAs nano-ridges tightly confine the optical mode within the epitaxial GaAs, and light leakage into the underlying Si substrate is negligible. Shi *et al.* demonstrated room temperature single-mode nano-ridge lasers grown on Si through

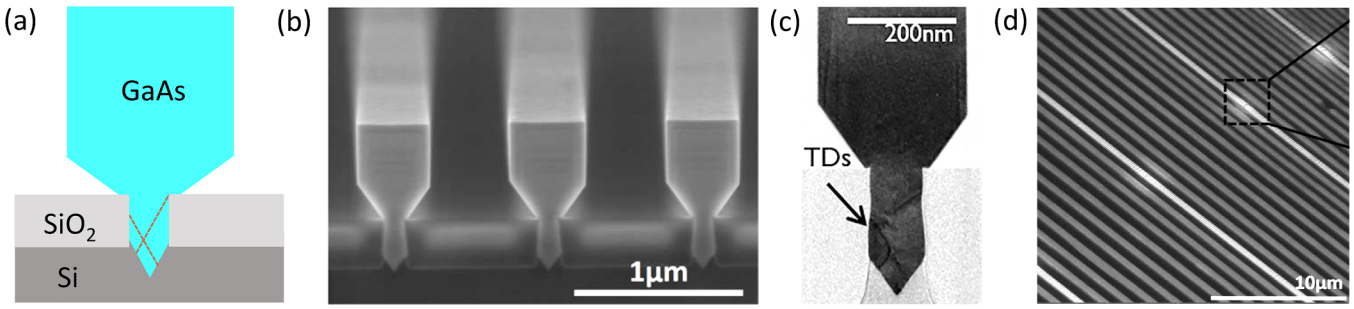

FIG. 4. (a) Schematic illustrating the concept of the NRE method. The red dotted lines denote the confinement of crystalline defects within the narrow oxide trenches. (b) SEM image of large-dimension GaAs ridge structures grown out of narrow oxide trenches. (c) Cross-sectional TEM image of GaAs nano-ridge grown on SOI using NRE. Adapted with permission from Kunert *et al.*, Appl. Phys. Lett. **109**(9), 091101 (2016). Copyright 2016 AIP Publishing. (d) SEM image of 1020 nm GaAs/InGaAs DFB nano-ridge lasers directly grown on Si. Adapted with permission from Shi *et al.*, Optica **4**(12), 1468–1473 (2017). Copyright 2017 OSA Publishing.

incorporating InGaAs quantum wells and InGaP passivation layers with patterned DFB gratings atop the nano-ridges [see the SEM photo in Fig. 4(d)].[42] The lasers operate under optical excitation, and the lasing wavelength can be tuned from 1000 nm to 1040 nm by adjusting the grating parameters. The same group later demonstrated loss-coupled DFB nano-ridge lasers with metallic gratings,[45] which sheds light on future realization of electrically driven devices. Currently, the lasing peaks of GaAs/InGaAs nano-ridge lasers are outside the range of Si-transparent wavelengths, and naturally the next step is to extend the emission peak to the telecom band. This goal might be achieved by either growing InGaAs nano-ridges with embedded indium-rich quantum wells or incorporating InAs quantum dots atop the (001)-oriented GaAs nano-ridge front. Another route toward telecom lasing involves the design of laser structures using the GaSb nano-ridges on Si.[72]

C. Template assisted selective epitaxy

As the III–V/Si nucleation area reduces, the density of the generated TDs progressively decreases; and accordingly, the release of misfit strain changes from plastic relaxation to elastic relaxation. The epitaxial III–V crystal is presumably TD-free when the diameter of the nucleation area is below 100 nm.[35] This unique mechanism has been exploited for the growth of self-assembled quantum dots on highly mismatched substrates (e.g., InAs quantum dots on GaAs and InP) and vertical III–V nanowires on (111)-oriented Si wafers.[73,74] As indicated by the schematic in Fig. 5(a), the template assisted selective epitaxy (TASE) method initiates III–V nucleation from a tiny Si seed to promote elastic relaxation and preclude the formation of TDs. The III–V nucleation then expands its dimension laterally following the guide of a hollow oxide template. The resultant III–V crystals are thereby free of any crystalline defects and can support fundamental modes in the near-infrared band. Wirths *et al.* demonstrated the direct growth of GaAs micro-disk lasers on (001) Si using the TASE method, as shown by the electron photos in Fig. 5(b).[43] The hexagonal GaAs micro-disk lasers operate under optical excitation and emit at around 840 nm. Interestingly, the GaAs micro-crystals grown on Si/SOI by TASE can also serve as virtual substrates for the regrowth of micro-disk and micro-ring lasers, as illustrated by the schematics in Fig. 5(c).[46] Although the morphology of the regrown crystals seems difficult to control, these micro-cavity lasers can still operate at room temperature under optical excitation. Surprisingly, the crystal orientation of the GaAs micro-substrates is not aligned with the (001) Si seed and instead switches to a [−110] orientation as the growth evolves,[46] which might pose challenges for the subsequent growth of quantum wells and quantum dots. To date, micro-cavity lasers grown on (001) Si by the TASE method are all GaAs-based, with the laser cavity also functioning as the active gain medium. Extending the lasing wavelength from the 850 nm band to the 1.3 μm and 1.5 μm bands necessitates the growth of InP- or GaSb-based micro-lasers on Si/SOI as well as the incorporation of quantum structures as active gain medium.

D. Lateral aspect ratio trapping

In blanket hetero-epitaxy of III–V lasers on Si wafers, research efforts have been centered at reducing the TD density of the III–V/Si templates. As the template technologies mature and qualify as compliant substrates, the incorporation of self-assembled quantum dots and diode laser designs from previously developed schemes in III–V photonics can be accordingly applied. This compatibility with existing technologies significantly speeds up the development of this straightforward approach. In a similar way, expediting the progress of selective hetero-epitaxy to obtain large-dimension III–V crystals on insulators will offer an alternative to the well-established technologies of the heterogeneous bonding approach. As schematically illustrated in Fig. 6(a), the lateral ART method allows for the direct growth of micrometer-scale III–V crystals right above the buried oxide layer.[75,76] In contrast to the ART approach discussed earlier, InP crystals produced by this strategy feature a coplanar configuration with the Si device layer, and the lateral dimension can be extended to a few micrometers and potentially to tens of micrometers. The lateral oxide trenches can be created via either anisotropic wet etching or soft dry etching. Initiating growth from the {111}-oriented Si bevel prohibits the formation of APBs, and the defect necking effect of the wide lateral trenches effectively blocks the propagation of TDs as a result of the high "aspect ratio" in the lateral direction. Figure 6(b) shows a tilted-view SEM image of InP grown on (001) SOI substrates using the lateral ART method. The lateral oxide trench guides the evolution of the InP stripes, which extends across the entire wafer. Through synergizing the lateral ART and the TASE methods, InP segments can be formed inside the lateral oxide templates as evidenced by the SEM image in Fig. 6(c). In this case, the crystal orientation of the epitaxial InP follows that of the (001)-oriented Si device layer. The large-area epitaxy of in-plane InP with different dimensions and geometries provides flexibility for the laser designs and subsequent light interfacing with Si-based waveguides. The grown III–V on insulator devices could eventually mimic III–V materials bonded onto SOI wafers as demonstrated in the commercialized heterogeneous integration approaches.

E. Conformal growth and corrugated epitaxial lateral overgrowth

Although the highly confined growth discussed above effectively blocks the propagation of crystalline defects, it also limits the maximum achievable dimension of the epitaxial III–V materials. The ART, the NRE, and the TASE methods often produce III–V crystals with sub-micrometer dimensions, and the lateral ART approach extends this dimension to a few micrometers. Further enlarging the dimension of the epitaxial III–V to tens and even hundreds of micrometers calls for selective regrowth using the epitaxial III–V on Si as seed layers. Figure 7(a) displays two strategies in the literature to achieve large-dimension III–V materials with a close proximity to the Si substrates. Growth initiates with the deposition of a thin-layer defective III–V film atop the planar Si wafer. In the conformal growth scheme,[77] a thin layer of growth mask is then patterned atop the III–V thin film for the subsequent undercut and regrowth process. In another scheme named corrugated epitaxial lateral overgrowth (CELOG),[78,79] the as-grown III–V thin film on Si is first patterned into short segments and then encapsulated with a thin oxide mask for the following selective regrowth process. In both strategies, III–V materials with dimensions up to tens of micrometers can be obtained [see the SEM photo in Fig. 7(b)].

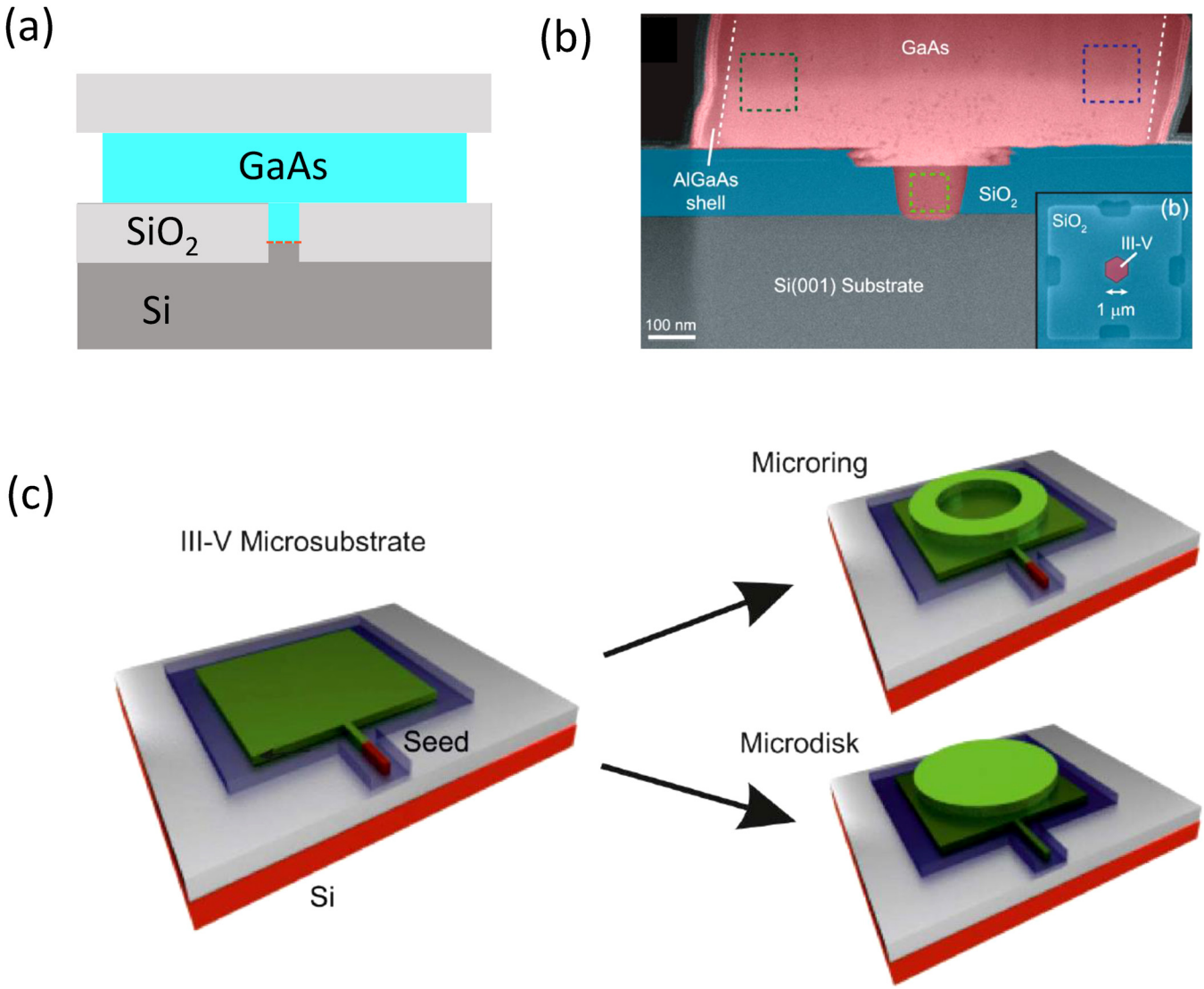

FIG. 5. (a) Schematic illustrating the concept of the TASE method. TDs are completely removed through initiating III–V from sub-100 nm Si surfaces. (b) Cross-sectional TEM image of GaAs micro-disk lasers grown on (001) Si substrate. Adapted with permission from Wirths *et al.*, ACS Nano **12**(3), 2169–2175 (2018). Copyright 2018 ACS Publications. (c) Schematic showing the regrowth of GaAs micro-disk/ring lasers atop the GaAs micro-substrates. Adapted with permission from Mayer *et al.*, IEEE Photonics Technol. Lett. **31**(13), 1021–1024 (2019). Copyright 2019 IEEE Publishing.

Crystalline defects induced by lattice mismatch are confined within the seed mesa while the laterally overgrown III–V is free of any TDs [see the TEM photo in Fig. 7(c)]. These large-dimension III–V crystals could be furthered processed into desirable templates for the subsequent growth of lasers structures.

F. Other methods

In addition to the selective growth schemes, another interesting path toward laser integration on Si involves transferring the nanowire/nano-pillar lasers grown on (111)-oriented Si platform to the (001)-oriented Si platform. This is accomplished through creating {111}-oriented Si bevels on (001)-oriented SOI wafers and then growing III–V nanowires from the masked Si facets, as schematically illustrated in Fig. 8(a).[80] Chang *et al.* utilized this method to grow GaAs nanowires on (001) SOI substrates and then constructed photonic crystal cavities with well-aligned nanowire arrays. Although they have not detected similar lasing behavior from the nanowire array grown on (001) SOI as they have previously demonstrated on the (111) SOI platform,[81] this integration approach

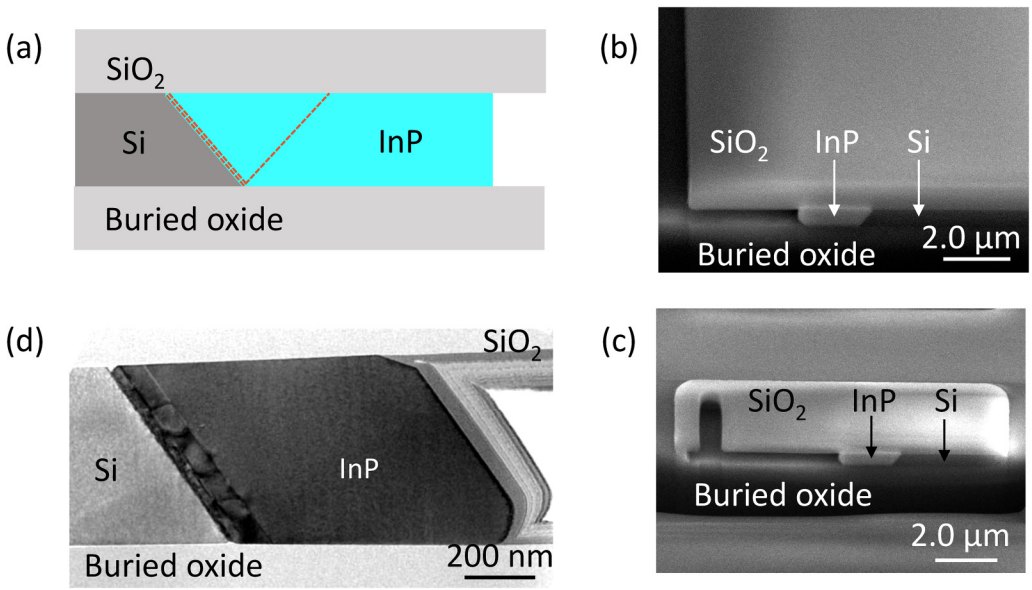

FIG. 6. (a) Schematic illustrating the scheme of lateral ART. The red dotted lines denote the confinement of the majority of crystalline defects at the InP/Si interface and the trapping of residual TDs by the top and bottom SiO_2 layers. (b) Tilted-view SEM photo of InP stripes directly grown on SOI using the lateral ART method. (c) Tilted-view SEM photo of InP segments directly grown on SOI through synergizing the lateral ART and the TASE methods. (d) Cross-sectional TEM image of InP grown on SOI using lateral ART.

highlights the potential of growing other III–V nanowires or nano-pillars on (001) Si/SOI substrates. However, the slanted configuration might complicate the laser fabrication and future realization of electrically injected devices.

Traditionally, III–V materials are grown on crystalline native or Si substrates; however, recent findings show that III–V crystals such as nano-pillars and micro-islands can be directly deposited atop amorphous SiO_2 layers.[51] As indicated by the schematic in Fig. 8(b), the surface kinks on the amorphous SiO_2 layer can serve as nucleation sites for the deposition of crystalline III–V crystals. The key is to ensure a large separation between adjacent nucleation sites to prevent the formation of poly-crystalline materials. One example of InP pillars is presented in Fig. 8(c), and as-expected, the InP nano-pillars manifest a random orientation.[51] As the lattice, thermal, and polarity mismatches are no longer a concern for growth on amorphous layers, the epitaxial III–V crystals are inherently free of dislocations as shown by the TEM image in Fig. 8(d). Besides, as the deposited InP crystals are embedded in a low index environment, the guided modes can be tightly confined within epitaxial InP crystals. Under optical excitation, room temperature lasing is detected from the as-grown InP nano-pillars and micro-islands. This surface kinks aided selective hetero-epitaxy can also be applied to other III–V compounds such as GaAs, InAs, and GaSb, but the growth parameters might be drastically different as the thermal dynamics of each material varies. Currently, this approach is at its infancy and the future work involves precise control of the position of the nucleation sites and orientation of the epitaxial III–V crystals.

IV. THE PROSPECT OF SELECTIVE HETERO-EPITAXY

Deployment of mature hetero-epitaxial III–V light emitters in standard Si/SOI platforms is the ultimately ideal goal of truly monolithic PICs. This imposes stringent requirements on the performance of the III–V lasers including continuous-wave electrical injection, room temperature and even high temperature operation, sufficient device lifetime, and efficient light coupling with Si-based photonic devices. To be compatible with current CMOS standard technologies, the growth of III–V devices on exact (001)-oriented Si/SOI wafers and a careful management of thermal budget and contamination are necessary. Although presently all the demonstrated III–V lasers selectively grown on Si operate under pulse optical excitation, recent innovations of growth strategies and device designs greatly propel the evolution to continuous-wave operation and electrical pumping. In addition, selective hetero-epitaxy offers a variety of unique advantages unavailable in other approaches. First, it allows for the growth of a complete suite of III–V compound semiconductors, including GaAs, InP, GaSb, and InAs, on exact (001) Si substrates.[35,82–86] Also, these epitaxial III–V alloys can be engineered to be TD-free, which is crucial for the reliability of lasers grown on Si. Next, this method enables the growth of III–V nano-structures with various geometries and architectures, and thereby produces lasers with an ultra-small footprint and benefits the construct of compact PICs.[43,44,46] Moreover, the unique defect management of selective hetero-epitaxy confines crystalline defects at localized regions and renders epitaxial III–V compounds in close proximity to the Si device layer, which is a significant plus

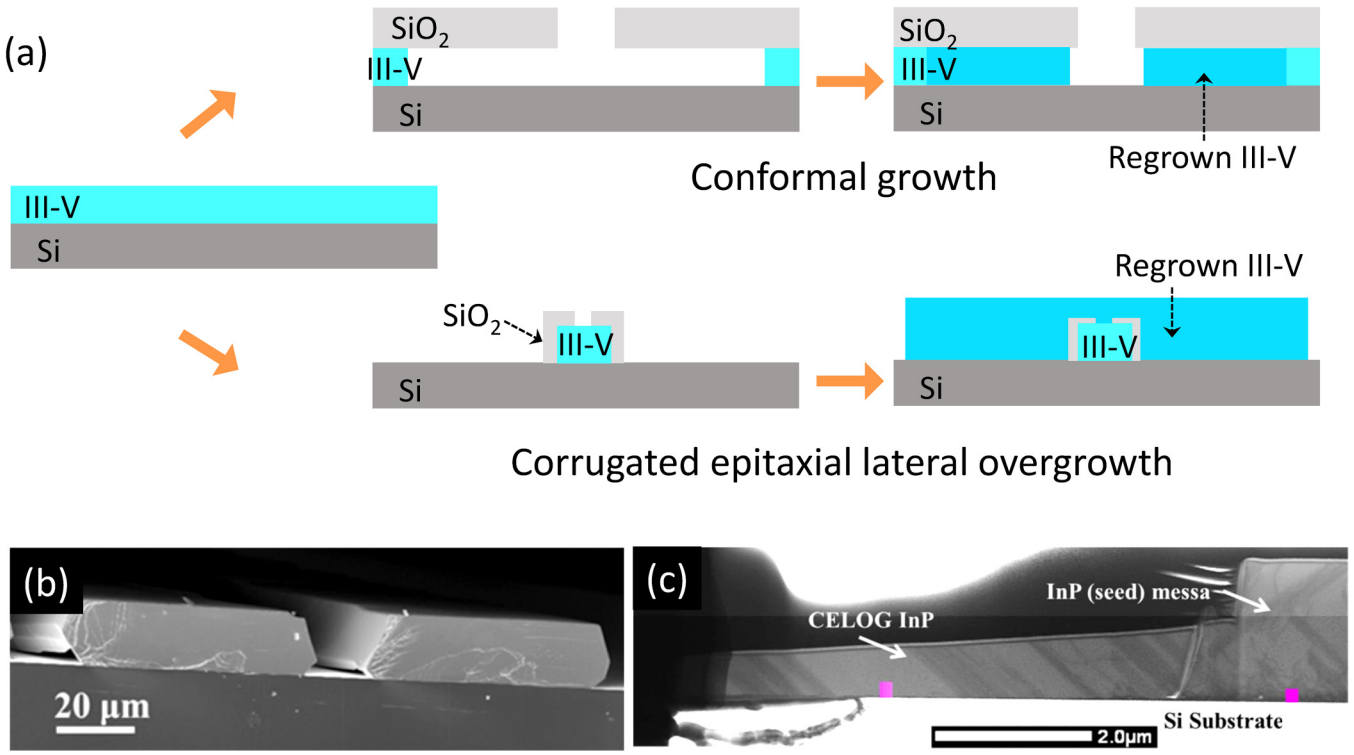

FIG. 7. (a) Schematic showing the concepts of conformal growth (Ref. 77) and corrugated epitaxial lateral overgrowth (CELOG). (b) SEM image of InP grown on Si using CELOG (Ref. 78). (c) Cross-sectional TEM image of InP grown on Si using CELOG. (Adapted with permission from Wondwosen *et al.*, J. Phys. D Appl. Phys. **48**, 045102 (2015). Copyright 2015 IOP Publishing.

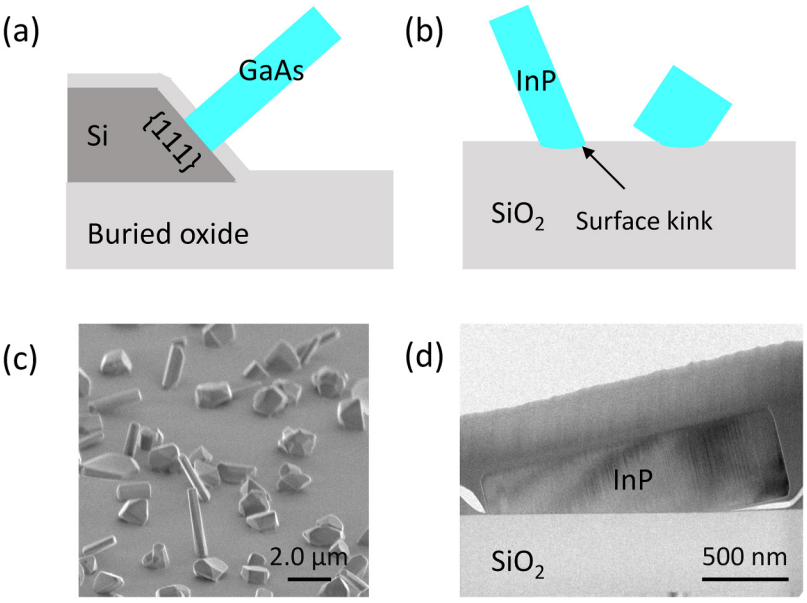

FIG. 8 (a) Schematic showing the growth of III–V nanowires from etched {111}-facets on (001) SOI wafers. (b) Schematic showing the deposition of III–V nano-pillars and micro-islands on amorphous SiO_2 wafers. The nucleation sites are surface kinks atop the amorphous SiO_2. (c) Tilted-view SEM photo of InP nano-pillars on amorphous SiO_2. (d) Cross-sectional TEM image of InP nanopillar grown on the amorphous SiO_2 layer.

for light interfacing with Si-waveguides.[87] Further selective hetero-epitaxy can also generate III–V crystals on Si/SOI with dimensions up to a few or even tens of micrometers.[76–79,88,89] These large-sized III–V materials enable the patterning of metal contacts without inducing large optical absorption loss, and thus pave the way toward the realization of electrically driven lasers. Finally, in the case of blanket hetero-epitaxy with thick buffers, material deposition often involves both MOCVD and MBE, and the total hetero-epitaxy process is usually long and involves a large overhead. In contrast, selective hetero-epitaxy is exclusively performed using MOCVD, and the elimination of the thick buffers together with surface diffusion from masked regions may reduce the growth time and resource consumption. In this section, we will discuss in detail the promises offered by selective hetero-epitaxy for III–V lasers' integration on Si toward practical applications.

A. A complete suite of TD-free III-V compounds on Si

Constructing multi-functional PICs entails the incorporation of a variety of materials onto the industry-standard Si platform. In terms of III–V compounds, this co-integration with Si enables the operation of PICs over a broad band of wavelengths and thereby for a wide range of applications. Current research on III–V/Si integration has been targeting data/telecom communications, and thus the GaAs and the InP material systems—where a wealth of information is readily available for efficient light emitting devices at the telecom band—have been extensively investigated. The methods discussed earlier for GaAs and InP can also be applied to grow highly mismatched GaSb and InAs alloys on Si, and efforts are underway to construct lasers using these materials. The successful development of selective hetero-epitaxy will offer the capability to integrate a complete suite of TD-free III–V compounds on Si substrates and extend the application of Si-photonics beyond data/telecom communications. As shown by the SEM photos in Figs. 9(a) and 9(b), the ART method produces uniform and high-quality GaSb and InAs nano-ridges inside sub-100 nm Si trenches.[82–86] Expanding the dimension to the sub-micrometer-scale for photonic applications has been proven viable as evidenced by the SEM image of GaSb nano-ridges grown inside wider Si trenches in Fig. 9(c). The NRE approach also creates large-dimension GaSb nano-ridges with tunable architectures on Si, which paves the way toward realizing both 1.5 μm and mid-infrared lasers on Si.[72] The TASE method has enabled the co-integration of vertical and horizontal GaSb and InAs nanowires on Si,[35] and similar concepts could be adopted to grow large-sized GaSb and InAs for mid-infrared photonic applications. The lateral ART scheme also gives rise to in-plane GaSb crystals selectively grown on Si as illustrated by the SEM image in Fig. 9(d). More importantly, these various selective growth schemes could enable the co-integration of different III–V compound semiconductors on the same Si wafer, as schematically illustrated in Fig. 9(e), albeit the necessity of various regrowth steps and careful thermal managements. The versatility of integrating a complete suite of TD-free and buffer-less III–V compounds on Si render selective hetero-epitaxy a highly competitive strategy for photonic integration.

B. Minimizing the laser footprint

Minimizing the laser footprint benefits the circuit performance in terms of operation speed, power consumption, and integration density, and meanwhile spawns novel applications beyond optical interconnects such as spectroscopy, sensing, and optical probing.[90,91] Selective hetero-epitaxy could produce high-quality III–V crystals with a variety of compositions, geometries, architectures, and dimensions. These bottom–up semiconductor crystals

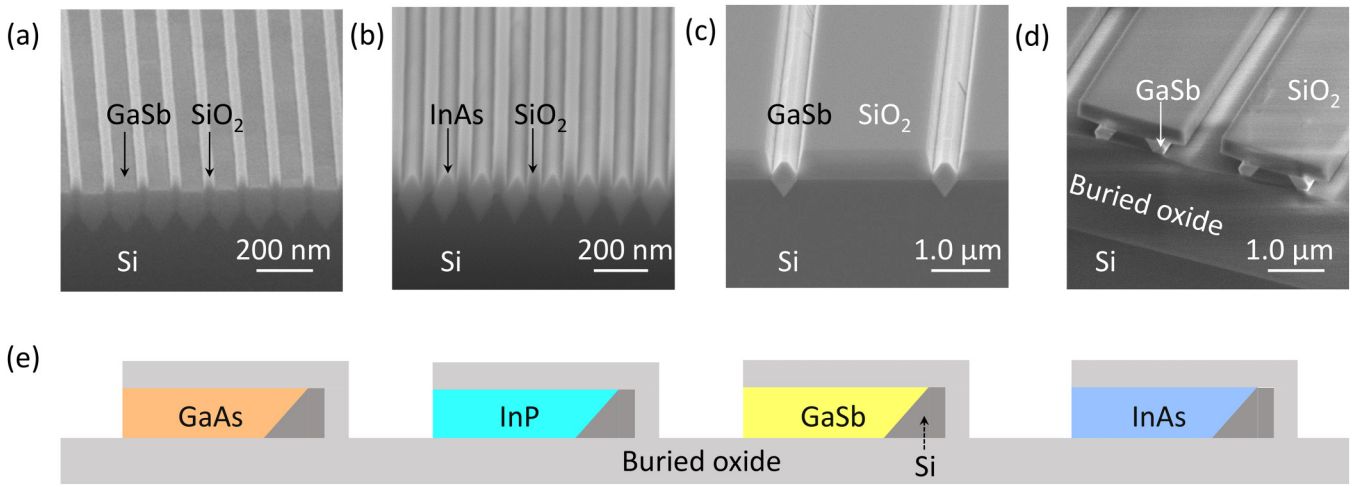

FIG. 9. Growth of GaSb and InAs on (001) Si/SOI using different selective hetero-epitaxy schemes. (a) Tilted-view SEM photo of GaSb nano-ridges grown inside 90 nm wide Si trenches using the ART method. (b) SEM photo of InAs nano-ridges grown inside 90 nm wide Si trenches using the ART method. (c) SEM photo of large-dimension GaSb nano-ridges grown inside 500 nm wide Si trenches using the ART method. (d) SEM photo of GaSb stripes inside lateral oxide trenches using the lateral ART method. (e) Schematic showing the co-integration of a complete suite of III–V compound semiconductors on the (001) Si platform.

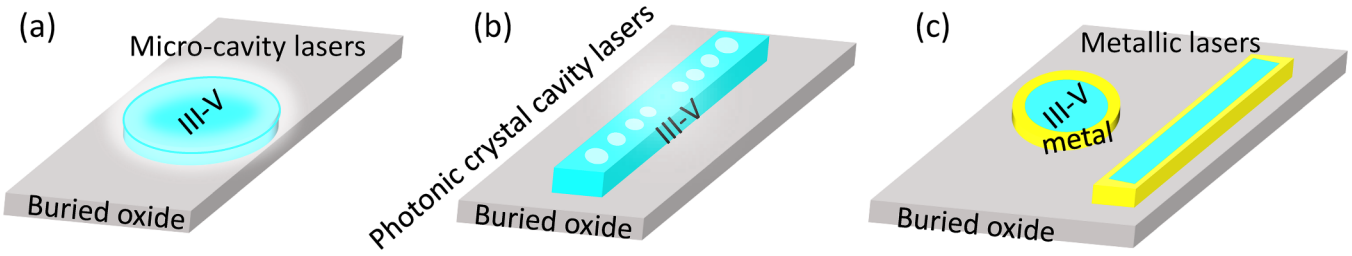

FIG. 10. (a) Schematic illustrating the integration of III–V micro-cavity lasers on (001) SOI. (b) Schematic illustrating the design of III–V photonic crystal cavity lasers on (001) SOI. (c) Schematic illustrating the design of III–V plasmon or non-plasmon mode metallic lasers on (001) SOI.

feature sizes ranging from tens of nanometers to tens of micrometers, and thereby are ideal candidates for fabricating small cavity lasers. Also the unique III–V on insulator configuration offered by some selective growth schemes confines light within the epitaxial material and facilitates downscaling of the cavity size.[43,76] As the physical dimension of the laser cavity shrinks, the gain offered by the active medium scales accordingly. To attain lasing with limited material gain, the mirror loss must be accordingly reduced to reach the threshold condition. High-quality (Q) cavities such as micro-disks/rings and photonic crystal cavities could help reduce the dimension of the laser footprint, and room-temperature electrically driven III–V lasers have been demonstrated on their native substrates.[92–94] These high-Q lasers can be transferred onto the Si/SOI platform once the metrics of the epitaxial III–V materials meet the requirement of the device fabrication, as schematically shown in Figs. 10(a) and 10(b). Another route toward minimizing the laser footprint involves the introduction of metals to enhance the mode confinement of the laser cavity as depicted in Fig. 10(c).[95,96] Despite the extra absorption loss induced by the metal encapsulation, the metallic contacts could serve as heat sinks and also ease electrical injection.[97] The footprint of high-Q lasers and non-plasmon metallic lasers is ultimately constrained by the diffraction limit of the emission wavelength. Plasmon mode metallic lasers could further downscale the laser dimension beyond the diffraction limit through exploiting the surface plasmon–polariton modes at the dielectric and the metal interface.[98,99]

C. Light interfacing with Si-photonics

Current research of III–V lasers grown on Si has been limited at demonstrating lasing functionalities using novel growth schemes and improving the performance of standalone devices. Yet, building a complete PIC requires light interfacing with Si-based photonic components. In addition, an efficient light interfacing between III–V and Si synergizes the merits of both material systems and engenders hybrid devices with unprecedented performances.[100,101] Selective hetero-epitaxy confines crystalline defects induced by lattice mismatch at the III–V/Si hetero-interfaces or within a thin layer of III–V materials. Such a "buffer-less" feature significantly eases the light interfacing with Si-waveguides. The coupling efficiency thereby hinges on the configuration of the III–V lasers relative to the Si-waveguides and the specific design of light couplers. As schematically illustrated in Figs. 11(a) and 11(b), the selective growth approaches can be divided into two categories according to the growth direction of the III–V crystals: vertical integration and lateral integration. The ART and the NRE methods produce vertically evolving III–V crystals and the resultant III–V lasers and the Si-waveguides locate at different planes. In sharp contrast, the TASE and the lateral ART approaches generate laterally evolving III–V crystals and, as a result, III–V lasers and Si-waveguides feature a coplanar configuration. Naturally, the lateral integration approach could achieve a higher coupling efficiency and a shorter coupling length compared with the vertical integration approach. Indeed, the study by Shi *et al.* shows that the coupling length of GaAs/InGaAs nano-ridges lasers grown by the NRE technique is around 45 μm for directional couplers and reaches up to 200 μm for advanced adiabatic couplers [see the schematics in Fig. 11(c)].[87] Our calculation indicates that the coupling length of III–V lasers grown by the TASE or the lateral ART approaches can be as short as 16 μm when the gap is set as 100 nm, as schematically shown in Fig. 11(d). Apart from the evanescent coupling, butt coupling between the epitaxial III–V lasers and the Si-waveguides is also a feasible solution [see the schematic in Fig. 11(e)] and could potentially achieve a high coupling efficiency through adjusting the gap between the III–V lasers and Si-waveguides as well as the architecture of the Si-waveguide coupler.[102] In this coplanar configuration, the spacing between III–V and Si can be precisely defined using photolithography down to tens of nanometers, which significantly reduces the coupling length and benefits the realization of ultra-compact Si-based PICs. Although current research of light interfacing is limited at theoretical studies, we will soon witness the transition to actual device implementations as the efforts toward fully integrated PICs intensify.

D. Toward continuous-wave operation

At room temperature, all the reported III–V lasers selectively grown on (001) Si/SOI platforms operate under pulse optical excitation, and continuous-wave lasing behavior has only been observed at cryogenic temperatures.[103,104] Compared to continuous-wave excitation, pumping the lasers with short optical pulses generates a throb of high density carriers required for population inversion, and thereby obviates the detrimental consequences induced by heat. In general, operating lasers under pulse excitation signals either high lasing thresholds of the devices or poor heat dissipation. As a result, to attain continuous-wave operation, one can work on these two directions: reducing the lasing thresholds through increasing the gain or

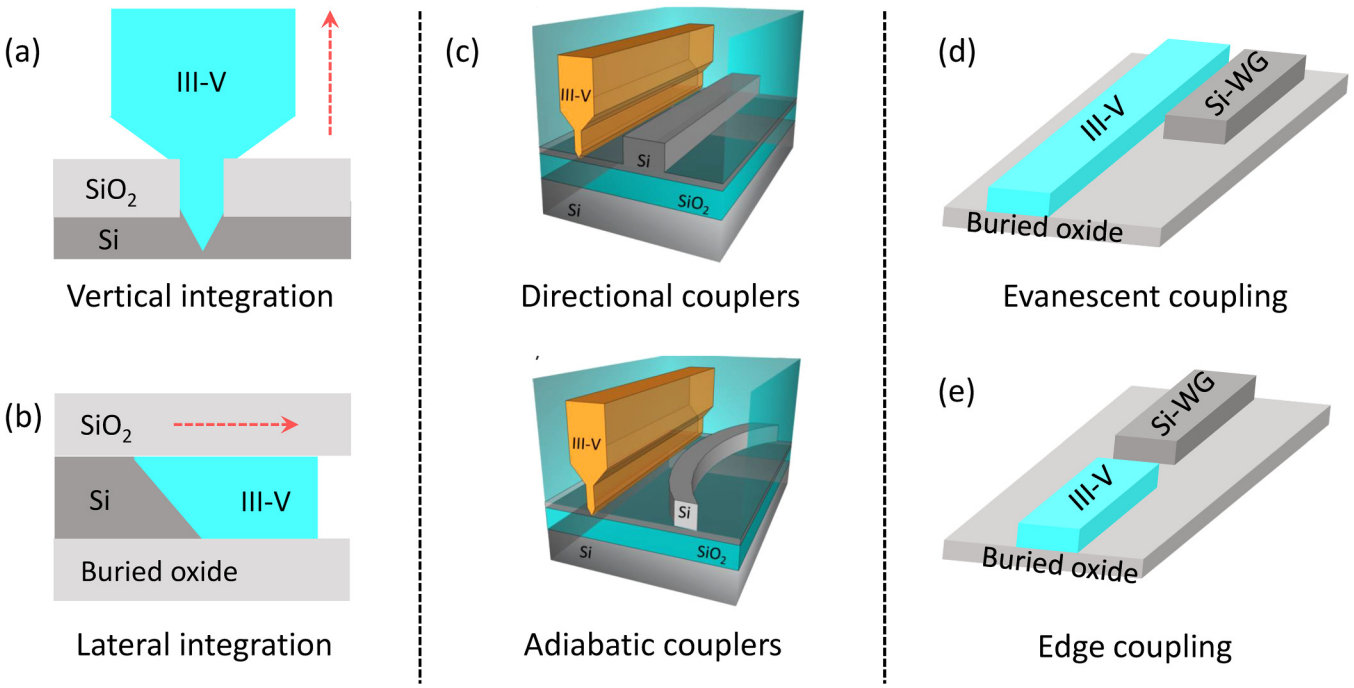

FIG. 11. (a) Schematic showing the vertical integration of III–V lasers on Si. The red dotted arrow denotes the growth direction. (b) Schematic showing the lateral integration of III–V lasers on Si. The red dotted arrow denotes the growth direction. (c) Schematics showing the designed directional couplers and adiabatic couplers based on III–V lasers grown on Si using the NRE methods. Adapted with permission from Opt. Express **27**(26), 37781–37794 (2019). Copyright 2019 OSA Publishing. (d) Evanescent coupling between epitaxial III–V crystals and the Si-waveguides (WGs) based on lateral integration. (e) Butt coupling between epitaxial III–V crystals and the Si-waveguides based on lateral integration.

decreasing the loss and enhancing the heat dissipation of the devices.[105] In the case of III–V lasers selectively grown on Si, the cavities generally manifest a sub-wavelength scale and the cavity loss is substantially larger than their macroscopic counterparts grown using blanket hetero-epitaxy. Advanced cavity designs including photonic crystal cavities and circular micro-disk/ring cavities could be adopted to minimize the mirror loss. Another issue relates to the large surface-to-volume ratio of the III–V lasers selectively grown on Si, and non-radiative recombination via surface states is sometimes substantial. Low dimension quantum structures such as quantum dashes and quantum dots could enhance the confinement of the charged carriers and minimize the surface recombination. In addition, these selectively grown III–V lasers on Si are often encapsulated by low index materials such as air and SiO_2 to tightly confine the optical mode inside the epitaxial material, which results in a poor heat dissipation of the devices. Adopting heat conducing materials, such as SiN and metals, could help cool down the working devices and attain continuous-wave operation.

E. Toward electrically driven lasers

The main roadblock obstructing the path toward electrical injection is the limited material volume of III–V crystals selectively grown on Si substrates and the resultant large optical absorption loss induced by metal contacts.[106] One possible solution involves the careful design of metal contacts to minimize the overlap with the optical mode supported inside the sub-micrometer III–V crystal. Figure 12(a) displays the design of GaAs/InGaAs p-i-n diodes by Ozdemir *et al.* using nano-ridges selectively grown on Si by the NRE method.[107,108] The authors performed the doping of the junctions during selective hetero-epitaxy and adopted a regrowth process to form a narrow p+ GaAs layer for the p-metal contact. The n-contact is patterned atop a heavily doped Si substrate. In this scenario, light is tightly confined within the wider active region, and metal induced optical absorption loss is proven to be negligible. Although lasing results have not been reported, the authors recently demonstrated p-i-n photodetectors using this design in a 300 mm CMOS line. The other route toward electrically injection includes expanding the size of the epitaxial III–V alloy from nanometer-scale to micrometer-scale, which naturally provides more space for separating the metal contacts from the active gain medium. Figure 12(b) displays the design of lateral InP-based p-i-n diodes selectively grown on SOI wafers.[76] In contrast to the vertical integration offered by the NRE and the ART method, this type of lateral configuration can be achieved by the TASE, the lateral ART, and the CELOG approaches. The dimension of the laterally evolved III–V crystal can be extended to a few micrometers by the lateral ART method and even to tens of micrometers by the CELOG method. The large-dimension III–V/

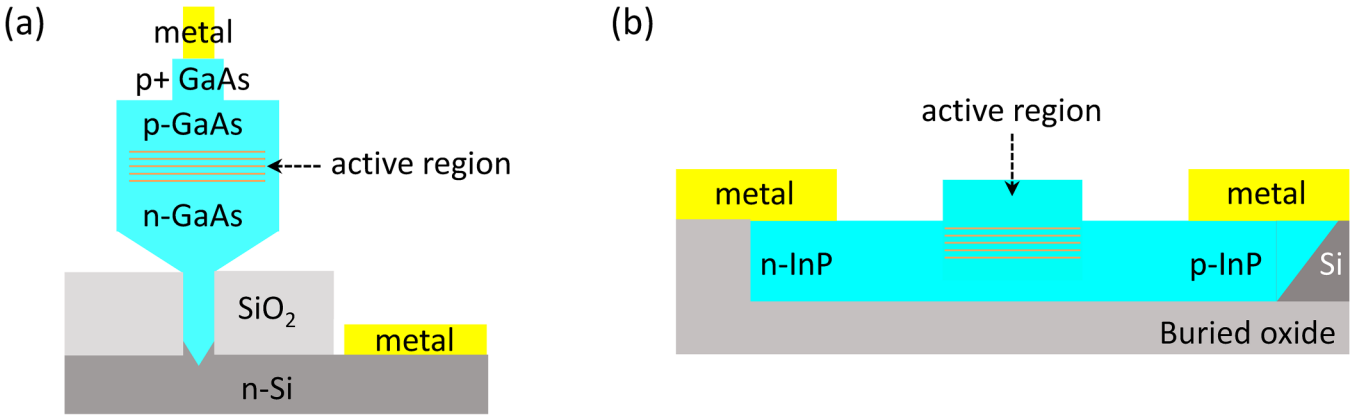

FIG. 12 (a) Schematic showing the design of electrically driven lasers based on sub-micrometer GaAs/InGaAs nano-ridges selectively grown on Si using the NRE method (Ref. 107). (b) Schematic showing a possible design of electrically driven lasers using micrometer-scale InP selectively grown on Si with a regrown active region.

SiO_2 can serve as virtue templates for the regrowth of flat (001)-oriented quantum wells, as has been widely adopted in the heterogeneous integration approach with bonded III–V thin films/membranes on SOI.[109] In addition, the unique configuration of III–V on insulator facilitates the confinement of light within the active region and thereby minimizes the optical loss induced by metal contacts. Doping of the III–V materials can be realized during the epitaxial process[110] and can also be performed after the material deposition using top–down processing techniques such as thermal diffusion and ion implantation. Lateral InGaAs p-i-n photodetectors with operation speed up to 25 GHz have recently been demonstrated.[111] These recent innovations, including the doping of the epitaxial III–V into p-i-n junctions, the tight mode confinement with minimal metal absorption loss, and the demonstrations of high-performance p-i-n photodetectors, foreshadow the realization of electrically driven lasers by selective hetero-epitaxy.

V. CONCLUSION

In conclusion, selective hetero-epitaxy is evolving as a promising strategy for III–V laser integration on Si because of its unique ability to seamlessly interface III–V active devices with passive Si components. In addition, the promise to integrate a complete suite of III–V compounds on Si together with the potential to downscale the laser footprint to nanometer-scale renders selective hetero-epitaxy suitable for multi-functional and ultra-compact PICs. Although currently the demonstrated lasers require optical excitation, novel growth schemes including NRE, TASE, and lateral ART enable the extension of the material dimension to micrometer-scale for future realization of electrically driven devices. These unique promises offered by selective hetero-epitaxy point to the implementation of fully integrated Si-photonics in the near future.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

REFERENCES

[1]R. Jones, P. Doussiere, J. B. Driscoll, W. Lin, H. Yu, Y. Akulova, T. Komljenovic, and J. E. Bowers, IEEE Nanotechnol. Mag. **13**(2), 17–26 (2019).
[2]D. Liang, A. Roshan-Zamir, Y. Fan, C. Zhang, B. Wang, A. Descos, W. Shen *et al.*, J. Lightwave Technol. **38**(13), 3322–3337 (2019).
[3]A. Z. Subramanian, E. Ryckeboer, A. Dhakal, F. Peyskens, A. Malik, B. Kuyken, H. Zhao *et al.*, Photonics Res. **3**(5), B47–B59 (2015).
[4]J. Sun, E. Timurdogan, A. Yaacobi, Z. Su, E. S. Hosseini, D. B. Cole, and M. R. Watts, IEEE J. Sel. Top. Quantum Electron. **20**(4), 264–278 (2013).
[5]J. W. Silverstone, J. Wang, D. Bonneau, P. Sibson, R. Santagati, C. Erven, J. L. O'Brien, and M. G. Thompson, in *2016 International Conference on Optical MEMS and Nanophotonics (OMN)* (IEEE, 2016), pp. 1–2.
[6]Y. Shen, N. C. Harris, S. Skirlo, M. Prabhu, T. Baehr-Jones, M. Hochberg, X. Sun *et al.*, Nat. Photonics **11**(7), 441 (2017).
[7]B. Jalali and S. Fathpour, J. Lightwave Technol. **24**(12), 4600–4615 (2006).
[8]R. Soref, Nat. Photonics **4**(8), 495–497 (2010).
[9]E. D. Palik, *Handbook of Optical Constants of Solids* (Academic Press, 1998), Vol. 3.
[10]D. Liang and J. E. Bowers, Nat. Photonics **4**(8), 511–517 (2010).
[11]Y. Yao, A. J. Hoffman, and C. F. Gmachl, Nat. Photonics **6**(7), 432–439 (2012).
[12]I. Vurgaftman, R. Weih, M. Kamp, J. R. Meyer, C. L. Canedy, C. S. Kim, M. Kim *et al.*, J. Phys. D Appl. Phys. **48**(12), 123001 (2015).
[13]R. Marchetti, C. Lacava, L. Carroll, K. Gradkowski, and P. Minzioni, Photonics Res. **7**(2), 201–239 (2019).
[14]T. Komljenovic, M. Davenport, J. Hulme, A. Y. Liu, C. T. Santis, A. Spott, S. Srinivasan, E. J. Stanton, C. Zhang, and J. E. Bowers, J. Lightwave Technol. **34**(1), 20–35 (2016).

[15]A. De Groote, P. Cardile, A. Z. Subramanian, A. M. Fecioru, C. Bower, D. Delbeke, R. Baets, and G. Roelkens, Opt. Express. **24**(13), 13754–13762 (2016).
[16]J. C. Norman, D. Jung, Y. Wan, and J. E. Bowers, APL Photonics **3**(3), 030901 (2018).
[17]A. Y. Liu and J. E. Bowers, IEEE J. Sel. Top. Quantum Electron. **24**(6), 1–12 (2018).
[18]Z. Wang, A. Abbasi, U. Dave, A. De Groote, S. Kumari, B. Kunert, C. Merckling *et al.*, Laser Photonics Rev. **11**(4), 1700063 (2017).
[19]M. Martin, D. Caliste, R. Cipro, R. Alcotte, J. Moeyaert, S. David, F. Bassani *et al.*, Appl. Phys. Lett. **109**(25), 253103 (2016).
[20]K. Volz, A. Beyer, W. Witte, J. Ohlmann, I. Németh, B. Kunert, and W. Stolz, J. Cryst. Growth **315**(1), 37–47 (2011).
[21]Q. Li, K. W. Ng, and K. M. Lau, Appl. Phys. Lett. **106**(7), 072105 (2015).
[22]B. Kunert, Y. Mols, M. Baryshniskova, N. Waldron, A. Schulze, and R. Langer, Semicond. Sci. Technol. **33**(9), 093002 (2018).
[23]Q. Li and K. M. Lau, Prog. Cryst. Growth Charact. Mater. **63**(4), 105–120 (2017).
[24]S. Chen, W. Li, J. Wu, Q. Jiang, M. Tang, S. Shutts, S. N. Elliott *et al.*, Nat. Photonics **10**(5), 307 (2016).
[25]D. Jung, R. Herrick, J. Norman, K. Turnlund, C. Jan, K. Feng, A. C. Gossard, and J. E. Bowers, Appl. Phys. Lett. **112**(15), 153507 (2018).
[26]Y. Xue, W. Luo, S. Zhu, L. Lin, B. Shi, and K. M. Lau, Opt. Express **28**(12), 18172–18179 (2020).
[27]M. R. Calvo, L. M. Bartolomé, M. Bahriz, G. Boissier, L. Cerutti, J. B. Rodriguez, and E. Tournié, Optica **7**(4), 263–266 (2020).
[28]Y. Wan, S. Zhang, J. C. Norman, M. J. Kennedy, W. He, S. Liu, C. Xiang *et al.*, Optica **6**(11), 1394–1400 (2019).
[29]B. Shi, Y. Han, Q. Li, and K. M. Lau, IEEE J. Sel. Top. Quantum Electron. **25**(6), 1–11 (2019).
[30]A. Y. Liu, S. Srinivasan, J. Norman, A. C. Gossard, and J. E. Bowers, Photonics Res. **3**(5), B1–B9 (2015).
[31]J. C. Norman, D. Jung, Z. Zhang, Y. Wan, S. Liu, C. Shang, R. W. Herrick, W. W. Chow, A. C. Gossard, and J. E. Bowers, IEEE J. Quantum Electron. **55**(2), 1–11 (2019).
[32]O. Marshall, M. Hsu, Z. Wang, B. Kunert, C. Koos, and D. V. Thourhout, Proc. IEEE **106**(12), 2258–2269 (2018).
[33]J. Z. Li, J. Bai, J.-S. Park, B. Adekore, K. Fox, M. Carroll, A. Lochtefeld, and Z. Shellenbarger, Appl. Phys. Lett. **91**(2), 021114 (2007).
[34]L. Czornomaz, E. Uccelli, M. Sousa, V. Deshpande, V. Djara, D. Caimi, M. D. Rossell, R. Erni, and J. Fompeyrine, in *2015 Symposium on VLSI Technology (VLSI Technology)* (IEEE, 2015), pp. T172–T173.
[35]H. Schmid, M. Borg, K. Moselund, L. Gignac, C. M. Breslin, J. Bruley, D. Cutaia, and H. Riel, Appl. Phys. Lett. **106**(23), 233101 (2015).
[36]B. Kunert, W. Guo, Y. Mols, B. Tian, Z. Wang, Y. Shi, D. Van Thourhout *et al.*, Appl. Phys. Lett. **109**(9), 091101 (2016).
[37]P. Staudinger, S. Mauthe, K. E. Moselund, and H. Schmid, Nano Lett. **18**(12), 7856–7862 (2018).
[38]M. Paladugu, C. Merckling, R. Loo, O. Richard, H. Bender, J. Dekoster, W. Vandervorst, M. Caymax, and M. Heyns, Cryst. Growth Des. **12**(10), 4696–4702 (2012).
[39]Z. Wang, B. Tian, M. Paladugu, M. Pantouvaki, N. L. Thomas, C. Merckling, W. Guo *et al.*, Nano Lett. **13**(11), 5063–5069 (2013).
[40]Z. Wang, B. Tian, M. Pantouvaki, W. Guo, P. Absil, J. V. Campenhout, C. Merckling, and D. V. Thourhout, Nat. Photonics **9**(12), 837–842 (2015).
[41]B. Tian, Z. Wang, M. Pantouvaki, P. Absil, J. V. Campenhout, C. Merckling, and D. Van Thourhout, Nano Lett. **17**(1), 559–564 (2017).
[42]Y. Shi, Z. Wang, J. V. Campenhout, M. Pantouvaki, W. Guo, B. Kunert, and D. V. Thourhout, Optica **4**(12), 1468–1473 (2017).
[43]S. Wirths, B. F. Mayer, H. Schmid, M. Sousa, J. S. Gooth, H. Riel, and K. E. Moselund, ACS Nano **12**(3), 2169–2175 (2018).
[44]S. Mauthe, B. Mayer, M. Sousa, G. Villares, P. Staudinger, H. Schmid, and K. Moselund, Nanophotonics VII **10672**, 106722U (2018).
[45]Y. Shi, M. Baryshnikova, Y. Mols, M. Pantouvaki, J. V. Campenhout, B. Kunert, and D. V. Thourhout, in *2019 Conference on Lasers and Electro-Optics Europe & European Quantum Electronics Conference (CLEO/Europe-EQEC)* (IEEE, 2019) p. 1.
[46]B. F. Mayer, S. Wirths, S. Mauthe, P. Staudinger, M. Sousa, J. Winiger, H. Schmid, and K. E. Moselund, IEEE Photonics Technol. Lett. **31**(13), 1021–1024 (2019).
[47]Y. Li, W. Yang, S. Du, X. Zhou, M. Wang, H. Yu, Y. Zhang, and J. Pan, in *International Photonics and OptoElectronics Meeting 2019 (OFDA, OEDI, ISST, PE, LST, TSA)* (Optical Society of America, 2019), paper JTh4E.6.
[48]Y. Han, W. K. Ng, Y. Xue, Q. Li, K. S. Wong, and K. M. Lau, Opt. Lett. **44**(4), 767–770 (2019).
[49]Y. Han, W. K. Ng, Y. Xue, K. S. Wong, and K. M. Lau, Photonics Res. **7**(9), 1081–1086 (2019).
[50]Y. Han, Z. Yan, W. K. Ng, Y. Xue, K. S. Wong, and K. M. Lau, Optica **7**(2), 148–153 (2020).
[51]Y. Han, Z. Yan, W. K. Ng, Y. Xue, K. W. Ng, K. S. Wong, and K. M. Lau, Appl. Phys. Lett. **116**(17), 172102 (2020).
[52]K. E. Moselund, H. Schmid, C. Bessire, M. T. Bjork, H. Ghoneim, and H. Riel, IEEE Electron Device Lett. **33**(10), 1453–1455 (2012).
[53]N. Waldron, C. Merckling, L. Teugels, P. Ong, S. A. U. Ibrahim, F. Sebaai, A. Pourghaderi, K. Barla, N. Collaert, and A. Voon-Yew Thean, IEEE Electron Device Lett. **35**(11), 1097–1099 (2014).
[54]N. Waldron, C. Merckling, W. Guo, P. Ong, L. Teugels, S. Ansar, D. Tsvetanova *et al.*, in *2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers* (IEEE, 2014), pp. 1–2.
[55]Q. Li, Y. Han, X. Lu, and K. M. Lau, IEEE Electron Device Lett. **37**(1), 24–27 (2015).
[56]Y. Han, Q. Li, and K. M. Lau, IEEE Electron Device Lett. **37**(6), 717–720 (2016).
[57]S. Sant, K. Moselund, D. Cutaia, H. Schmid, M. Borg, H. Riel, and A. Schenk, IEEE Trans. Electron Devices **63**(11), 4240–4247 (2016).
[58]Y. Han, Q. Li, and K. M. Lau, IEEE Electron Device Lett. **38**(5), 556–559 (2017).
[59]Y. Han, Q. Li, and K. M. Lau, IEEE Trans. Electron Devices **64**(10), 4078–4083 (2017).
[60]R. Chen, T. D. Tran, K. W. Ng, W. S. Ko, L. C. Chuang, F. G. Sedgwick, and C. Chang-Hasnain, Nat. Photonics **5**(3), 170–175 (2011).
[61]B. Mayer, L. Janker, B. Loitsch, J. Treu, T. Kostenbader, S. Lichtmannecker, T. Reichert *et al.*, Nano Lett. **16**(1), 152–156 (2016).
[62]F. Lu, I. Bhattacharya, H. Sun, T. D. Tran, K. W. Ng, G. N. M. Silveira, and C. Chang-Hasnain, Optica **4**(7), 717–723 (2017).
[63]H. Kim, W. J. Lee, A. C. Farrell, A. Balgarkashi, and D. L. Huffaker, Nano Lett. **17**(9), 5244–5250 (2017).
[64]Y. Han, Q. Li, and K. M. Lau, J. Appl. Phys. **120**(24), 245701 (2016).
[65]W. Guo, L. Date, V. Pena, X. Bao, C. Merckling, N. Waldron, N. Collaert *et al.*, Appl. Phys. Lett. **105**(6), 062101 (2014).
[66]Y. Han, Q. Li, K. W. Ng, S. Zhu, and K. M. Lau, Nanotechnology **29**(22), 225601 (2018).
[67]C. Merckling, N. Waldron, S. Jiang, W. Guo, N. Collaert, M. Caymax, E. Vancoille *et al.*, J. Appl. Phys. **115**(2), 023710 (2014).
[68]S. Li, X. Zhou, M. Li, X. Kong, J. Mi, M. Wang, W. Wang, and J. Pan, Appl. Phys. Lett. **108**(2), 021902 (2016).
[69]Y. Han, Q. Li, S. P. Chang, W. D. Hsu, and K. M. Lau, Appl. Phys. Lett. **108**(24), 242105 (2016).
[70]L. Megalini, B. Bonef, B. C. Cabinian, H. Zhao, A. Taylor, J. S. Speck, J. E. Bowers, and J. Klamkin, Appl. Phys. Lett. **111**(3), 032105 (2017).
[71]B. Kunert, W. Guo, Y. Mols, R. Langer, and K. Barla, ECS Trans. **75**(8), 409 (2016).
[72]M. Baryshnikova, Y. Mols, Y. Ishii, R. Alcotte, H. Han, T. Hantschel, O. Richard *et al.*, Crystals **10**(4), 330 (2020).
[73]D. Bimberg, M. Grundmann, and N. N. Ledentsov, *Quantum Dot Heterostructures* (John Wiley & Sons, 1999).
[74]K. Tomioka, Y. Kobayashi, J. Motohisa, S. Hara, and T. Fukui, Nanotechnology **20**(14), 145302 (2009).

[75]Y. Han, Y. Xue, and K. M. Lau, Appl. Phys. Lett. **114**(19), 192105 (2019).
[76]Y. Han, Z. Yan, Y. Xue, and K. M. Lau, Appl. Phys. Lett. **117**(05), 052102 (2020).
[77]O. Parillaud, E. Gil-Lafon, B. Gérard, P. Etienne, and D. Pribat, Appl. Phys. Lett. **68**(19), 2654–2656 (1996).
[78]M. Wondwosen, H. Kataria, Y. Sun, and S. Lourdudoss, J. Phys. D Appl. Phys. **48**, 045102 (2015).
[79]Y.-T. Sun, G. Omanakuttan, and S. Lourdudoss, Appl. Phys. Lett. **106**, 213504 (2015).
[80]T. Y. Chang, H. Kim, B. T. Zutter, W. J. Lee, B. C. Regan, and D. L. Huffaker, Adv. Funct. Mater. **30**, 2002220 (2020).
[81]H. Kim, W. J. Lee, A. C. Farrell, J. Morales, P. Senanayake, S. V. Prikhodko, T. J. Ochalski, and D. L. Huffaker, Nano Lett. **17**(6), 3465–3470 (2017).
[82]T. Orzali, A. Vert, B. O'Brian, J. L. Herman, S. Vivekanand, S. S. Papa Rao, and S. R. Oktyabrsky, J. Appl. Phys. **120**(8), 085308 (2016).
[83]Q. Li, B. Lai, and K. M. Lau, Appl. Phys. Lett. **111**(17), 172103 (2017).
[84]Y. Mols, J. Bogdanowicz, P. Favia, P. Lagrain, W. Guo, H. Bender, and B. Kunert, J. Appl. Phys. **125**(24), 245107 (2019).
[85]Z. Yan, Y. Han, and K. M. Lau, Nanotechnology **31**(34), 345707 (2020).
[86]Z. Yan, Y. Han, and K. M. Lau, J. Appl. Phys. **128**(3), 035302 (2020).
[87]Y. Shi, B. Kunert, Y. D. Koninck, M. Pantouvaki, J. V. Campenhout, and D. V. Thourhout, Opt. Express **27**(26), 37781–37794 (2019).
[88]N. H. Julian, P. A. Mages, C. Zhang, and J. E. Bowers, J. Cryst. Growth **402**, 234–242 (2014).
[89]G. Omanakuttan, Y. T. Sun, C. R. Hedlund, C. Junesand, R. Schatz, S. Lourdudoss, V. Pillard *et al.*, Opt. Mater. Express **10**(7), 1714–1723 (2020).
[90]M. T. Hill and M. C. Gather, Nat. Photonics **8**(12), 908–918 (2014).
[91]R. Ma and R. F. Oulton, "Applications of nanolasers," Nat. Nanotechnol. **14**(1), 12–22 (2019).
[92]J. V. Campenhout, P. Rojo-Romeo, P. Regreny, C. Seassal, D. V. Thourhout, S. Verstuyft, L. D. Cioccio, J. M. Fedeli, C. Lagahe, and R. Baets, Opt. Express **15**(11), 6744–6749 (2007).
[93]Y. Chassagneux, R. Colombelli, W. Maineult, S. Barbieri, H. E. Beere, D. A. Ritchie, S. P. Khanna, E. H. Linfield, and A. Giles Davies, Nature **457**(7226), 174–178 (2009).
[94]K. Takeda, T. Sato, A. Shinya, K. Nozaki, W. Kobayashi, H. Taniyama, M. Notomi, K. Hasebe, T. Kakitsuka, and S. Matsuo, Nat. Photonics **7**(7), 569–575 (2013).
[95]M. T. Hill, Y. S. Oei, B. Smalbrugge, Y. Zhu, T. De Vries, P. J. Van Veldhoven, F. W. M. Van Otten *et al.*, Nat. Photonics **1**(10), 589–594 (2007).
[96]M. P. Nezhad, A. Simic, O. Bondarenko, B. Slutsky, A. Mizrahi, L. Feng, V. Lomakin, and Y. Fainman, Nat. Photonics **4**(6), 395–399 (2010).
[97]P. Tiwari, P. Wen, D. Caimi, S. Mauthe, N. Vico Triviño, M. Sousa, and K. E. Moselund, arXiv:2009.03572 (2020).
[98]M. A. Noginov, G. Zhu, A. M. Belgrave, R. Bakker, V. M. Shalaev, E. E. Narimanov, S. Stout, E. Herz, T. Suteewong, and U. Wiesner, "Demonstration of a spaser-based nanolaser," Nature **460**(7259), 1110–1112 (2009).
[99]J. Ho, J. Tatebayashi, S. Sergent, C. F. Fong, Y. Ota, S. Iwamoto, and Y. Arakawa, Nano Lett. **16**(4), 2845–2850 (2016).
[100]C. T. Santis, S. T. Steger, Y. Vilenchik, A. Vasilyev, and A. Yariv, Proc. Natl. Acad. Sci. U.S.A. **111**(8), 2879–2884 (2014).
[101]A. Ramaswamy, J. E. Roth, E. J. Norberg, R. S. Guzzon, J. H. Shin, J. T. Imamura, B. R. Koch *et al.*, in *Optical Fiber Communication Conference* (Optical Society of America, 2015), p. Th5B-5.
[102]Y. Han, Y. Xue, Z. Yan, and K. M. Lau, "Selectively grown III-V lasers for integrated Si photonics," J. Lightwave Technol. (unpublished).
[103]Y. Han, W. K. Ng, C. Ma, Q. Li, S. Zhu, C. C. S. Chan, K. W. Ng *et al.*, Optica **5**(8), 918–923 (2018).
[104]Y. Han, Q. Li, S. Zhu, K. W. Ng, and K. M. Lau, Appl. Phys. Lett. **111**(21), 212101 (2017).
[105]L. A. Coldren, S. W. Corzine, and M. L. Mashanovitch, *Diode Lasers and Photonic Integrated Circuits* (John Wiley & Sons, 2012), Vol. 218.
[106]G. Crosnier, D. Sanchez, S. Bouchoule, P. Monnier, G. Beaudoin, I. Sagnes, R. Raj, and F. Raineri, Nat. Photonics **11**(5), 297–300 (2017).
[107]C. I. Ozdemir, Y. De Koninck, N. Kuznetsova, M. Baryshnikova, D. Van Thourhout, B. Kunert, M. Pantouvaki, and J. Van Campenhout, "InGaAs/GaAs multi-quantum well nano-ridge waveguide photodetector epitaxially grown on a 300-mm Si wafer," in *IEEE Photonics Conference* (IEEE, 2020).
[108]A. Vais, L. Witters, Y. Mols, A. S. Hernandez, A. Walke, H. Yu, M. Baryshnikova *et al.*, in *2019 IEEE International Electron Devices Meeting (IEDM)* (IEEE, 2019), pp. 9.1.1–9.1.4.
[109]T. Fujii, K. Takeda, H. Nishi, N. P. Diamantopoulos, T. Sato, T. Kakitsuka, T. Tsuchizawa, and S. Matsuo, Optica **7**(7), 838–846 (2020).
[110]Y. Xue, Y. Han, Y. Wang, Z. Zhang, H. K. Tsang, and K. M. Lau, Opt. Lett. **45**(7), 1754–1757 (2020).
[111]S. Mauthe, Y. Baumgartner, M. Sousa, Q. Ding, M. D. Rossell, A. Schenk, L. Czornomaz, and K. E. Moselund, Nat. Commun. **11**(1), 1–7 (2020).