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Yu Han, Ying Xue, and Kei May Lau[a)]

AFFILIATIONS

Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong

[a)]**Email:** eekmlau@ust.hk

ABSTRACT

Efficient on-chip laser sources of Si photonics can be built from direct epitaxy of dislocation-free III–V alloys on industrial-standard (001) Si wafers. Here, we report on selective lateral epitaxy of InP on patterned (001) silicon-on-insulators (SOIs) by metal organic chemical vapor deposition. Based on the conventional "aspect ratio trapping" approach, we created undercut patterns to alter the growth front to the lateral direction. Growth of InP inside the nano-scale SOI trenches results in dislocation-free InP crystals right atop the buried oxide layer. The intimate placement of the InP crystals with the Si device layer points to the development of dislocation-free nano-ridges for integration of efficient III–V light emitters with Si-based photonic components on SOI.

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Current Si photonics can benefit from epitaxially grown III–V laser sources to realize fully integrated photonic integrated circuits.[1–3] Over the years, several techniques have been developed to directly grow III–V materials on industry-standard (001)-oriented Si substrates.[4–6] The key is how to engineer the generation and propagation of defects such as threading dislocations (TDs), stacking faults (SFs), and antiphase boundaries (APBs), and so the region where devices reside is free of crystalline defects.[7] Combining the traditional two-step growth procedure with dislocation filters and thermal cycle annealing, the TD density of a GaAs thin film on Si has been reduced to the level of $10^6\,cm^{-2}$, and the lifetime of lasers fabricated on the GaAs/Si template has been increased up to 10×10^6 h.[8] In spite of these impressive results, a lower TD density is always more desirable for longer laser lifetime. Moreover, coupling of lasers grown on top of the III–V buffer, typically a few microns thick, with the bottom Si-based photonic components is difficult. As an alternative, selective area growth of III–V alloys on patterned Si wafers could constrain defects at the III–V/Si interface and render defect-free III–V nano-structures. In one approach named template assisted selective epitaxy (TASE), III–V alloys initially nucleate at confined Si surfaces as nano-crystals and then develop into micron-scale III–V layers following predefined oxide patterns.[9,10] Room temperature stimulated emission at 800 nm has been reported from GaAs micro-disks grown on Si using the TASE method.[11] In another approach called aspect ratio trapping (ART), in-plane III–V nano-ridges, such as GaAs, InP, InAs, and GaSb, are formed inside nano-scale V-grooved Si trenches.[12–21] Room temperature lasing has been demonstrated from InP nano-ridges at 900 nm,[22] GaAs/InGaAs nano-ridges at 1020 nm,[23] and InP/InGaAs nano-ridges at 1330 nm and 1550 nm,[24–27] manifesting the potential of the ART approach for optoelectronic applications.

Figure 1(a) depicts a schematic of the conventional ART method with III–V nano-ridges nucleating at V-grooved Si surfaces and evolving along the [001] direction. Depending on the growth conditions and materials deposited, strain induced by III–V/Si lattice mismatch can be released by the formation of a high density of SFs and/or TDs. Benefitting from the defect necking effect, the TD density of the epitaxial III–V nano-ridge decreases as the III–V nano-ridge grows away from the V-grooved pocket. If the height of the oxide spacer h is larger than $1.4d$, where d is the width of the trenching opening, the hetero-epitaxial III–V is presumably free of dislocations as indicated by dotted red lines in Fig. 1(a).[7] For efficient wave-guiding at telecommunication wavelengths, the width of the nano-ridge should be, generally speaking, larger than 300 nm, which corresponds to a nano-ridge height of 420 nm. Such a large height complicates the coupling of the laser sources on top with the bottom Si-based devices. Additionally, the defective III–V layer beneath might hamper the carrier injection and metallization of future electrically injected nano-ridge lasers.

Here, building on the conventional ART approach, we present an alteration of "lateral ART" for the epitaxy of III–V nano/micro structures on (001)-oriented silicon-on-insulators (SOIs). Figure 1(b)

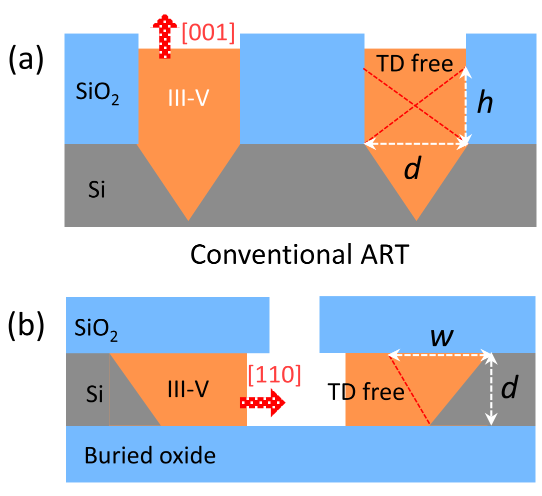

FIG. 1. (a) Schematic showing the defect trapping and growth mechanism of the conventional ART approach. (b) Schematic illustrating the defect trapping and growth mechanism of the proposed lateral ART approach.

schematically summarizes the designed growth strategy. Nano-scale Si trenches are engineered in a way that the Si surface locates at both sides of the undercut trench and is sandwiched between the top oxide spacer and the buried oxide layer. We initiate III–V/Si hetero-epitaxy at the exposed {111} Si surfaces that would not lead to the formation of APBs. Unlike the conventional ART method with vertical growth along the vertical [001] direction, the lateral ART features a horizontal growth front along the [110] direction. Given a Si device layer thickness of d, the width of the defective III–V layer is $w = 1.4d$ as shown in Fig. 1(b). A simple change of the growth direction unleashes numerous advantages unavailable in the conventional ART approach. The dimension of III–V nano-ridges grown by the conventional ART approach is limited by the trench width and thus photolithography; structural imperfections at the oxide sidewall created by dry etching will induce additional planar defects inside the epitaxial III–V alloys.[21] In sharp contrast, the dimension of III–V nano-ridges grown by lateral ART hinges on the thickness of the Si device layer which can be precisely controlled down to a few nanometers; and the atomic sharp surface of the oxide sidewall precludes the formation of any unwanted planar defects. In the conventional ART approach, the defective III–V lies right underneath the TD-free region and is thus difficult to be fully removed. In contrast, the defective III–V layer of the lateral ART resides at one side of the TD-free-region and can be readily etched away, rendering the TD-free III–V layer in contact with the buried oxide and close to the Si device layer. The in-plane and close placement of the III–V layer with the Si device layer also facilitates the integration of III–V light emitters with Si-based photonic components. Besides, the refractive index contrast between the epitaxial III–V and the buried oxide brings on strong mode confinement and could enable III–V light emitters with ultrasmall footprint. Additionally, in the lateral ART approach, the flexible undercut of the Si device layer and possible coalescence of the III–V layer could produce not only III–V nano-ridges but also micro-scale III–V layers atop the buried oxide. Interestingly, the dimension of the defective III–V layer can be significantly reduced by decreasing the thickness of the Si device layer. III–V crystals can then be formed via the coalescence of lateral nano-ridges and the subsequent vertical growth along the [001] direction.

Growth of III–V nano-ridges using the proposed lateral ART method started with the preparation of nano-patterned SOI wafers. The (001)-oriented SOI features a Si device layer thickness of $1.5 \pm 0.08\,\mu$m, a buried oxide thickness of $2.0 \pm 0.08\,\mu$m, and a Si handle layer thickness of $725 \pm 15\,\mu$m. We thinned down the Si device layer to 600 nm using the cycled oxidation/etching process and then grew the 500 nm thick SiO_2 spacer using thermal oxidation. The remaining Si device layer thus has a thickness around 350 nm. Nano-scale Si trenches with a width of 450 nm and a pitch of 2.8 μm were then patterned along the $[1\bar{1}0]$ direction on the SOI wafer using photolithography and following the dry etching process (see Fig. 2). Next, we etched the Si trenches into {111}-oriented V-grooves using KOH based anisotropic wet etching (30% at 90 °C). Prolonged etching resulted in a lateral undercut of the Si device layer and therefore symmetrical lateral Si trenches on SOI wafers.

To investigate the feasibility of the devised lateral ART approach, in this work, we focus on the lateral epitaxy of InP on SOI as depicted in Fig. 1(b). Prior to growth, the patterned SOI was dipped into diluted HF solution to remove the native oxide and then was immersed into KOH solution (45% at 70 °C) to obtain fresh {111}-oriented Si surfaces. Immediately after, the sample was loaded into the metal organic chemical vapor deposition (MOCVD) system (AIXTRON 200/4) and underwent a thermal cleaning process at 800 °C in a H_2 ambient. We selected triethylgallium (TEGa), tertiarybutylarsine (TBA), trimethylindium (TMIn), and tertiarybutylphosphine (TBP) as growth precursors. It should be mentioned that the previous growth condition of InP nano-ridges using the conventional ART method is not applicable for the growth using the lateral ART approach, possibly due to the difference in growth orientations. Another set of growth conditions are, therefore, formulated for the epitaxy of lateral ART. We began with the deposition of a 10 nm thick low temperature (LT) GaAs wetting layer at 400 °C with a V/III ratio of 22 and continued with the growth of a LT-InP nucleation layer at 430 °C with a V/III ratio of 211. Afterwards, the reactor temperature was ramped up to higher temperatures (from 630 °C to 670 °C) for the growth of a high temperature (HT) InP main layer with a V/III ratio of 187.

Figure 3 presents scanning electron microscopy (SEM) photos of lateral InP-epi grown at different epitaxial conditions using the designed lateral ART approach. Note that the samples were intentionally tilted on the SEM stage for better view of the lateral-epi morphology. Without the LT-InP nucleation layer, the HT-InP grown at 670 °C forms large islands and exhibits a nice faceting of the growth front, but an incomplete coverage of the Si surface as shown in Fig. 3(a). The large distance between adjacent InP islands stems from the poor affinity between HT-InP and the LT-GaAs wetting layer as well as the large diffusion length of indium adatoms at high temperatures.

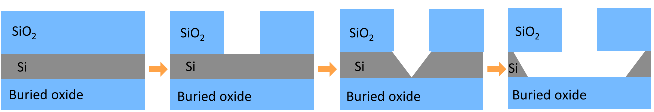

FIG. 2. Schematic summarizing the preparation of nano-patterned SOI wafers for the growth of III–V nano-ridges using the devised lateral ART approach.

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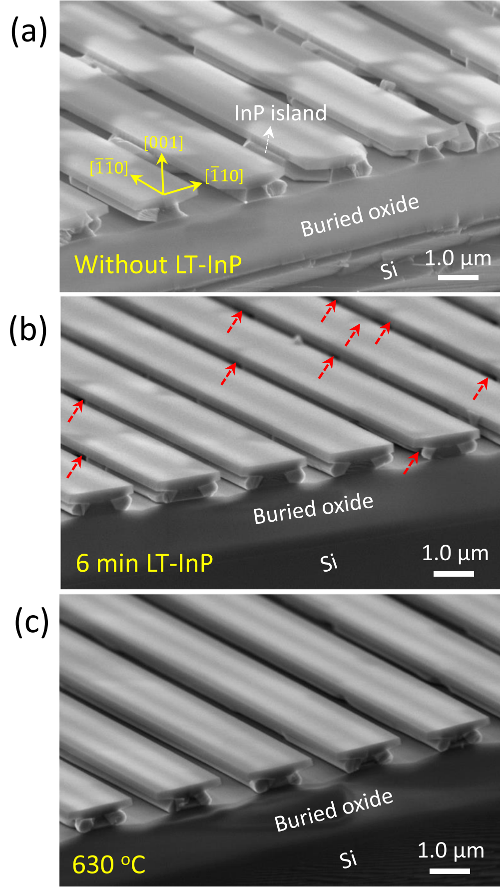

FIG. 3. (a) Tilted view SEM photo of InP grown using the lateral ART approach without the LT-InP nucleation layer. Larger InP islands with clear faceting are formed. (b) Tilted view SEM photo of InP grown using the lateral ART approach at 670 °C. Some dents are formed at the InP surface. (c) Tilted view SEM photo of InP grown using the lateral ART approach at 630 °C. The density of surface dents continues to decrease.

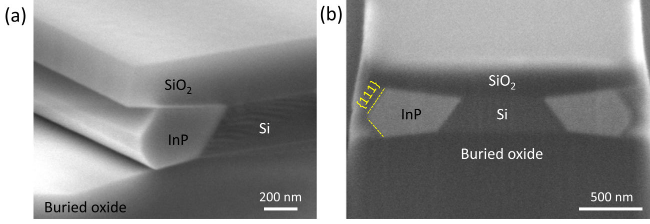

FIG. 4. (a) Tilted view SEM image of one InP sandwiched between the top oxide spacer and the buried oxide layer. (b) Cross-sectional SEM images of two symmetrical InP grown using the lateral ART approach.

To enable full coverage of HT-InP on the Si surface, we introduced a thin LT-InP nucleation layer between the LT-GaAs wetting layer and the HT-InP main layer. As shown by the SEM image in Fig. 3(b), the growth discontinuity (distance between adjoining InP islands) reduces and some InP islands coalesce into continuous nano-ridges. However, there are still some dents on the surface of the InP-epi due to the imperfect coalescence of InP islands during the HT-InP growth stage [see the red arrows in Fig. 3(b)]. To facilitate the coalescence of HT-InP islands, we reduced the growth temperature of HT-InP from 670 °C to 650 °C and then to 630 °C. Eventually, the density and depth of the surface dents significantly decreased, as evidenced by the SEM photo in Fig. 3(c). It should be pointed out that epitaxy of the HT-InP layer at lower temperatures such as 600 °C and 550 °C jeopardizes the surface morphology of the InP-epi with the presence of dense and shallow surface dents.

Figure 4(a) shows a tilted SEM image of one InP-epi "wing" grown using the lateral ART approach, and Fig. 4(b) displays a cross-sectional SEM image of two symmetrical InP-epi wings. As we designed, the Si pedestal sandwiched between the top oxide spacer and the buried oxide layer features two {111}-oriented surfaces. Starting from the nucleation sites provided by the {111} Si facets, the InP crystal evolves laterally along the [110] direction into wing-structures with two {111} facets. The angle between the two {111} facets is around 110° which indicates a zincblende crystal structure. We further confirmed the formation of zincblende InP in the following transmission electron microscopy (TEM) and room temperature photoluminescence (PL) measurements. Unlike the symmetrical {111} facets of nano-ridges grown by ART,[28] the top {1$\bar{1}$1} facet is slightly larger than the bottom {$\bar{1}$11} facet in lateral ART. We ascribe this asymmetry to the difference in the tilted angles between the top oxide spacer and the buried oxide layer [see Fig. 4(a)]. To investigate the defect generation and trapping mechanism of the lateral ART approach, we prepared TEM lamella using a focused ion beam (FEI Helios G4) and the specimen was subsequently inspected using a JEOL2010F field-emission microscope. As evidenced by the TEM photo in Fig. 5(a), most of the defects are restricted at the III–V/Si interface, and the InP layer away from the interface is defect-free [see Fig. 5(b)]. A close-up of the III–V Si interface reveals the formation of a high density of planar defects along the {1$\bar{1}$1} Si surface and a few planar defects along the {$\bar{1}$11} direction [see Fig. 5(c)]. These, planar defects are formed to accommodate the strain induced by the lattice mismatch between III–V and Si. While planar defects along the {1$\bar{1}$1} can be confined right at the III–V/Si interface, those along the {$\bar{1}$11} direction will penetrate into the InP main layer and terminate at the top oxide spacer.

We then studied the optical properties of the lateral InP-epi using micro-PL measurements. Excitation was delivered by a continuous-wave 514 nm laser, and photon emission was gathered by a thermoelectric-cooled InGaAs detector. The excitation laser was focused into a rectangular-spot with a dimension of 40 μm × 4 μm and was aligned along the lateral InP-epi direction during the measurement. Figure 6 presents the room temperature emission spectra of lateral InP-epi grown at different temperatures. The emission peak resides around 925 nm, attesting the zincblende structure of the lateral InP-epi. As the growth temperature increases from 630 °C to 670 °C, the peak intensity gradually increases and the spectral linewidth progressively narrows from 57 nm to 46 nm, in spite of the increasing number of surface dents. The improved optical property might stem from the larger material volume and better crystalline quality at higher temperatures. We also noticed a slight blue-shift of the emission peak as the growth temperature increases, which might result from the change of unintentional dopant concentration and the density of stacking faults. Note that, under similar excitation

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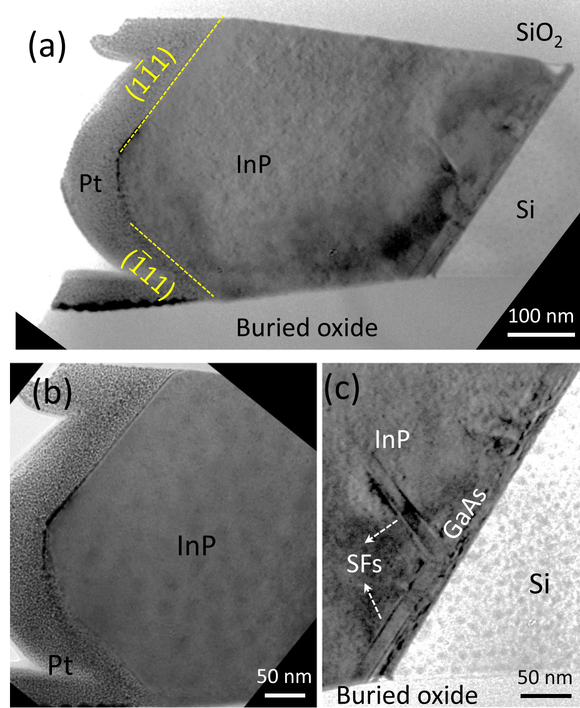

FIG. 5. (a) Cross-sectional TEM image of one InP grown by lateral ART. Most of the defects are confined at the III/Si interface. (b) Zoomed-in TEM image of the TD-free InP region. (c) Close-up TEM photo of the III–V/Si interface showing the formation of a high density of planar defects to release the strain induced by the 8% lattice mismatch between InP and Si.

conditions, the PL line-width of planar InP (semi-insulating InP wafer) is around 20 nm. We attribute the relatively broader line-width of our epitaxial InP to the generated crystalline defects at the III–V/Si interface which disrupt the perfect stacking of crystal planes and thus broaden the emission spectra. The strong emission intensity and the narrow line-width of the PL spectra suggest an excellent crystalline quality of the lateral InP-epi grown by the lateral ART approach.

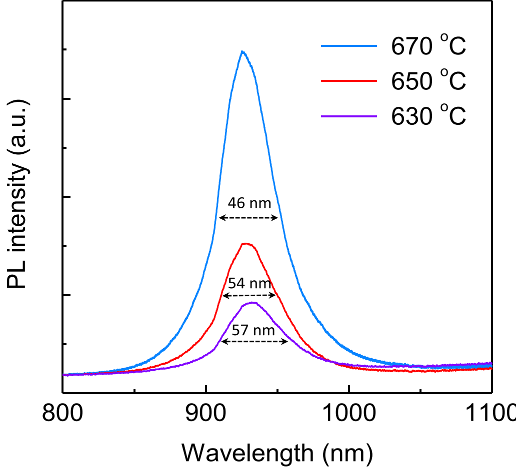

FIG. 6. Room temperature PL spectra of InP grown using the lateral ART approach at 670 °C, 650 °C, and 630 °C.

In conclusion, building from the conventional ART approach, we have developed a technique named lateral ART for the direct lateral epitaxy of dislocation-free III–V nano/micro-layers on (001)-oriented SOI wafers. By positioning Si nucleation sites between the top oxide spacer and the buried oxide layer, we enabled the selective lateral growth of dislocation-free lateral InP-epi right atop the buried oxide layer. Future work includes the growth of nano-scale and micro-scale III–V crystals on SOI through coalescence of adjacent lateral InP-epi. Growth parameters will be carefully engineered to manipulate the faceting and evolution of III–V alloys inside/outside the lateral Si trenches. This lateral ART approach could also be applied to the epitaxy of III–V materials with other structures and compositions and could bring additional functionalities on current Si photonics chips.

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