High-Voltage p-GaN HEMTs With OFF-State Blocking Capability After Gate Breakdown

Huaxing Jiang, *Member, IEEE*, Renqiang Zhu, Qifeng Lyu, and Kei May Lau, *Fellow, IEEE*

***Abstract*— In this letter, we report high-performance p-GaN HEMTs on Si with robust gate operation. For the first time, the preserved OFF-state drain blocking capability has been demonstrated in p-GaN HEMTs after forward gate breakdown. Benefitting from the reduced metal/p-GaN contact region, the gate breakdown was limited to take place only at the metal/p-GaN junction, with the p-GaN/AlGaN/GaN junction intact. The device shows state-of-the-art characteristics with a large threshold voltage of 1.75 V at I_D of 100 μA/mm (2.3 V by linear extrapolation), a high maximum drain current of 610 mA/mm at V_{GS} of 8 V, a low specific ON-resistance of 1.8 m$\Omega \cdot$ cm^2, and a high breakdown voltage of 1100 V defined at I_D of 1 μA/mm with grounded substrate.**

***Index Terms*— HEMT, p-GaN gate, normally-OFF, OFF-state, gate breakdown.**

I. Introduction

NORMALLY-OFF GaN high electron mobility transistors (HEMTs), with the merit of inherent fail-safe operation, fast switching speed, and low reverse conduction loss, have shown tremendous promise for efficient power switching applications [1]. Several approaches, including gate recess, p-(Al)GaN gate, and fluorine implantation, can be employed to realize normally-OFF GaN transistors and excellent device metrics such as high breakdown voltage (V_{BR}) and low ON-resistance (R_{ON}) have been demonstrated [2]–[11]. Among the aforementioned methods, p-(Al)GaN gate technology is currently the only one being employed in commercialized normally-OFF GaN HEMTs because of better controllability and stability in threshold voltage [1], [12], [13]. However, as a result of the metal-semiconductor gate contact scheme, either Schottky or Ohmic, the gate stack of p-GaN HEMTs is quite vulnerable, typically showing large gate leakage (I_G) and limited gate swing [6], [7]. An excessively high forward gate bias, e.g., gate voltage spikes at high speed switching transient, would often lead to catastrophic gate breakdown, with sudden and irreversible increase of gate leakage, thus device failure. To ensure the fail-safe operation of p-GaN HEMT power switches, it is vital to maintain the OFF-state blocking capability of the p-GaN HEMTs at V_{GS} of 0 V, i.e., a low standby drain leakage current, in case the gate breakdown occurs due to unexpected excessive gate overdrive. Otherwise, the surge of drain current after gate breakdown combining with a high OFF-state drain voltage can cause severe damage to the whole switching system, not only the device itself.

However, in all the reported p-GaN HEMTs, to our best knowledge, the forward hard breakdown of the gate stack increases both the forward and reverse I_G by several orders of magnitude, resulting in significant increase of OFF-state I_D and complete loss of gate control [14]–[17]. The failure mechanism of forward gate breakdown of p-GaN HEMTs is still under debate [15], [16], [18]. It is found that in the conventional p-GaN HEMT design, the gate metal is commonly self-aligned with the p-GaN gate [8], [19], [20], conveniently using the gate metal as the etching mask for p-GaN patterning. This design can spread the gate potential evenly on the p-GaN along the lateral channel direction. However, this gate architecture leads to high electric field (E-field) at the p-GaN edge near p-GaN/AlGaN junction, resulting in immature hard breakdown in the gate stack upon a small V_{GS}. A percolation path may be formed in the AlGaN barrier after gate breakdown [21], [22], shorting the p-GaN and 2-D electron gas channel through which the drain terminal is connected. Consequently, the p-GaN/AlGaN/GaN junction (p-i-n diode) which is the key to block high OFF-state V_{DS} (reverse biased p-i-n diode) under normal circumstances is destroyed, resulting in significant increase of reverse I_G.

In this work, for the first time, we have demonstrated a high-voltage p-GaN HEMT with OFF-state blocking capability after forward gate breakdown, by properly managing the E-field distribution in the gate stack thus keeping the p-GaN/AlGaN/GaN junction intact. Although the forward I_G increased significantly after forward gate breakdown, preventing the device from further normal operation, the OFF-state drain voltage and reverse gate leakage blocking capability are preserved in the device. We demonstrate such capability in our p-GaN HEMTs that exhibit a high V_{BR} of 1100 V at I_D of 1 μA/mm with grounded substrate, a low R_{ON} of 1.8 m$\Omega \cdot$cm^2, and a maximum I_D ($I_{DS,max}$) of 610 mA/mm, which are comparable to state-of-the-art device results.

II. Device Design and Fabrication

The MOCVD grown p-GaN/AlGaN/GaN heterostructure on a 6-inch Si substrate is from a commercial supplier. The epitaxial structure consists of a 5-μm high-resistivity GaN buffer, a 400-nm i-GaN channel, a 10-nm $Al_{0.2}Ga_{0.8}N$ barrier, and a 70-nm Mg-doped p-GaN cap, as shown in Fig. 1. The hole concentration in the p-GaN layer after

Manuscript received January 22, 2019; accepted February 2, 2019. Date of publication February 5, 2019; date of current version April 2, 2019. This work was supported by the Research Grants Council of Hong Kong under General Research Fund Grant 16215818. The review of this letter was arranged by Editor G. H. Jessen. *(Corresponding author: Kei May Lau.)*

The authors are with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong (e-mail: eekmlau@ust.hk).

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2019.2897694

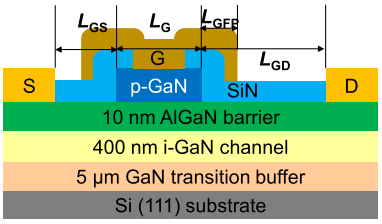

Fig. 1. Cross-sectional schematic of a fabricated p-GaN HEMT.

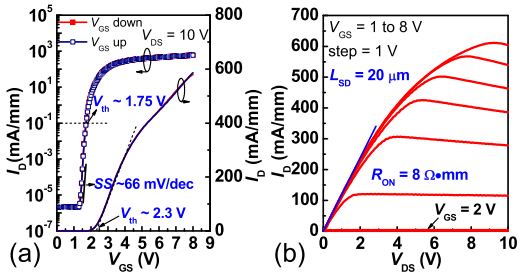

Fig. 2. (a) Transfer and (b) output characteristics of a representative p-GaN HEMT.

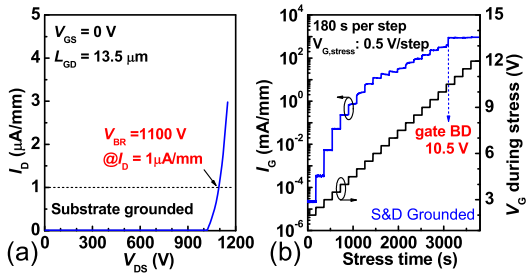

Fig. 3. (a) OFF-state drain leakage current and (b) step stress forward gate breakdown of the p-GaN HEMT.

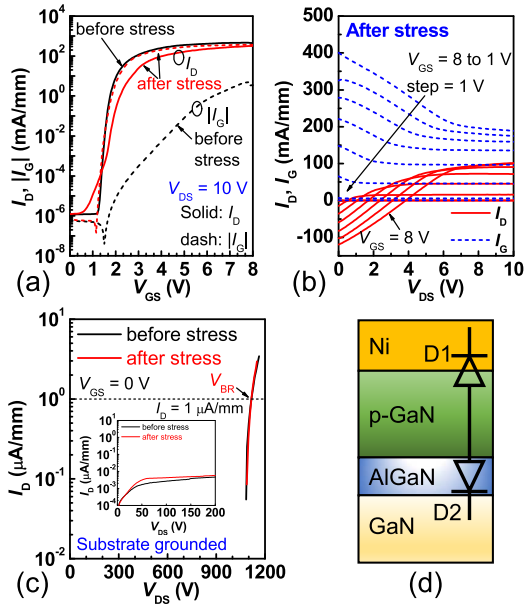

Fig. 4. (a) I_D and I_G versus V_{GS} of the device before and after the step stress measurement. (b) I_D and I_G versus V_{DS} of the device after the step stress. (c) OFF-state I_D before and after gate stress measurement. Inset: OFF-state I_D-V_{DS} for $V_{DS} \leq 200$ V. (d) Cross-sectional schematic and simplified equivalent circuit model of the gate stack of the p-GaN HEMT.

activation is $\sim 1 \times 10^{18}$ cm^{-3}. The device fabrication started with p-GaN patterning using a low-power (10 W) BCl_3/Cl_2-based inductively coupled plasma dry etching, with a 100-nm plasma-enhanced chemical vapor deposition (PECVD) SiO_2 as the etching mask. Then, Ti/Al/Ni/Au-based metal stack was deposited and annealed at 850°C for 30 s in nitrogen ambient for the source/drain Ohmic contacts. The device isolation was performed using fluorine implantation. Subsequently, a 100-nm PECVD SiN was deposited for surface passivation. After opening of the strategically smaller gate window on top of the p-GaN, a Ni/Au-based metal stack was formed as the gate contact. Since no post-metallization annealing was performed, the contact between Ni and p-GaN is Schottky like. Unless otherwise specified, the devices in this work feature a p-GaN gate length (L_G) of 5 μm, a gate-drain distance (L_{GD}) of 13.5 μm, a gate-source distance (L_{GS}) of 1.5 μm, and a gate width (W_G) of 10 μm. The gate metal foot is 2 μm, and the gate-connected field plate (GFP) is 2 μm on the drain side and 0.5 μm on the source side.

III. Device Results and Discussion

Fig. 2(a) shows the transfer characteristics of the fabricated device, with almost no hysteresis. The threshold voltage V_{th} is extracted to be 1.75 V at I_D of 0.1 mA/mm and 2.3 V by linear extrapolation. A high ON/OFF current ratio of 5×10^8 and a steep subthreshold slope (SS) of 66 mV/dec have been achieved. Fig. 2(b) shows the device output characteristics. At V_{GS} of 8 V, the device is able to deliver a high $I_{DS,max}$ of 610 mA/mm with a low accompanied R_{ON} of 8 $\Omega \cdot$ mm. By normalization to the device area, the specific ON-resistance $R_{ON,sp}$ is calculated to be 1.8 m$\Omega \cdot$cm^2, taking 1.5 μm transfer length for each Ohmic contact into account. Fig. 3(a) plots the OFF-state I_D versus V_{DS} at V_{GS} of 0 V with the substrate grounded, measured using a curve tracer (Tektronix 370A) with a minimum current resolution of 0.1 nA (0.01 μA/mm). As a result of high-resistivity buffer and well-managed electric field at the gate edge on the drain side, the device exhibited a high (soft) V_{BR} of 1100 V, defined at the criteria of I_D reaching 1 μA/mm. The I_D mainly arises from the substrate current. The large $I_{DS,max}$, high V_{BR}, and low R_{ON} are comparable to state-of-the-art normally-OFF GaN-on-Si transistors reported. The forward gate breakdown was evaluated by a step stress measurement for the devices to gauge the gate stack reliability (Fig. 3(b)). A step stress was applied to the gate terminal from 2 V to 12 V at 0.5 V/step with source and drain grounded. The duration of each step is 180 seconds. The gate stack with Ni on p-GaN showed a hard gate breakdown of 10.5 V.

The I_D and I_G versus V_{GS} of the device before and after the gate step stress are compared in Fig. 4(a). After the step stress measurement, I_G increases significantly and surpasses I_D when V_{GS} is larger than 1.5 V at V_{DS} of 10 V, suggesting a hard breakdown of the gate. Nevertheless, the device can still be turned OFF with a comparably low I_D and I_G at V_{GS} of 0 V. Fig. 4(b) plots the I_D and I_G versus V_{DS} of the device after the step stress. In contrast to the well behaved I_D-V_{DS} of the pre-stressed device shown in Fig. 2(b), the abnormal I_D-V_{DS}

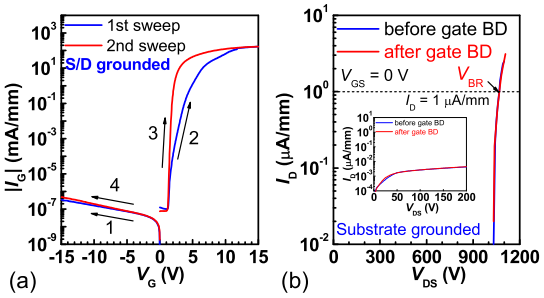

Fig. 5. (a) Comparison of forward and reverse I_G before and after gate breakdown test with maximum forward V_{GS} of +15 V. The arrows and numbers indicate the measurement sequence. (b) OFF-state drain leakage current before and after forward gate breakdown. Inset: OFF-state I_D-V_{DS} for $V_{DS} \leq 200$ V.

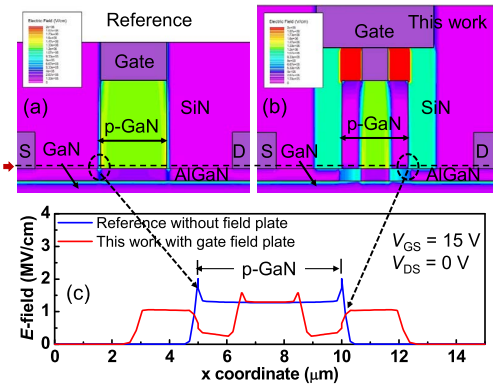

Fig. 6. Simulated E-field distribution in the gate stack region under forward gate bias of 15 V for p-GaN HEMTs with (a) rectangular gate metal self-aligned with p-GaN and (b) T-shaped gate metal with gate-connected field plate. (c) E-field distribution in p-GaN near the AlGaN barrier surface along the cutline shown in (a) and (b).

of the device post stress exhibited a much weaker gate modulation on I_D and the I_D curves intersect the V_{DS} axis when the device is turned ON ($V_{GS} > 2$ V), indicating the loss of proper switching capability after gate breakdown. The negative I_D at large V_{GS} and small V_{DS} (positive V_{GD}) suggests that the gate leakage current flowing into the drain terminal is larger than the current flowing out from the drain terminal into the source, as evidenced by the much larger I_G (the sum of I_{GS} and I_{GD}) at the same V_{GS}. When V_{GS} reduces from 8 V to 1 V, both I_G and I_D decrease dramatically, showing a turning-OFF process. Fig. 4(c) compares the OFF-state I_D and V_{BR} before and after the gate stress measurement. Since the leakage current for V_{DS} under 1000 V was below the measurement resolution, an Agilent 4156C semiconductor parameter analyzer was used to measure the currents for $V_{DS} \leq 200$ V, as shown in the inset of Fig. 4(c). Similar OFF-state I_D and V_{BR} were observed in the device before and after the stress measurement. Therefore, the OFF-state leakage blocking capability of the gate stack is clearly maintained in the device after hard gate breakdown. Even though the transistor cannot be further operated as a normal switch, the function of protecting the switching system can be achieved. The retained leakage blocking capability in our device can be explained by a typical two-diode model for the gate stack of the p-GaN HEMT with a Schottky gate, which consists of a Ni/p-GaN Schottky diode (D1) and a p-GaN/AlGaN/GaN p-i-n diode (D2), as illustrated in Fig. 4(d). While the hard forward gate breakdown damages the reverse-biased Schottky diode D1 only, the forward-biased p-i-n diode D2 remains intact. The reverse I_G and OFF-state I_D can still be blocked by the functional reverse-biased D2 and maintain at low levels similar to that before the gate breakdown, despite the irreversible increase of the forward I_G.

To further consolidate our results and explanation, the gate of another device is intentionally broken down after the first forward sweep to an excessively high V_{GS} of 15 V, as proven by the dramatically increased I_G at repeated low forward V_{GS} (Fig. 5(a)). The device still showed almost identical reverse I_G in the second sweep. Moreover, the OFF-state I_D and V_{BR} of the device after gate breakdown remained nearly the same as that before gate breakdown (Fig. 5(b)), suggesting that the D2 is still normally functioning. To our best knowledge, this is the first report on the retained high-voltage blocking capability of p-GaN HEMTs after forward gate breakdown. Since this is a general behavior observed in our p-GaN HEMTs, we believe the retained blocking capability can also be anticipated in large area devices using the gate structure design here.

To explain the distinct gate breakdown behaviors of our devices, we compared the simulated E-field distribution under a V_{GS} of 15 V for the conventional gate design which has a self-aligned gate metal with p-GaN and the T-shaped gate design here (Fig. 6). For the conventional design, an E-field peak locates at the p-GaN edge near the AlGaN surface, which can be flattened and suppressed by employing the T-shaped structure with gate-connected field plate and reduced metal/p-GaN contact periphery. The high peak E-field in the traditional design may result in undesirable breakdown near the p-GaN/AlGaN interface or inside AlGaN at the p-GaN edge, leading to the destruction of D2, thus losing OFF-state blocking function. While, the peak E-field in our design is significantly suppressed at the p-GaN edge and well confined inside the p-GaN gate region by the reduced metal/p-GaN contact area, protecting the p-i-n diode D2 from being damaged under large forward gate bias, thus maintaining the reverse blocking capability. Therefore, the gate contact architecture of p-GaN HEMTs needs to be carefully designed to realize the retained OFF-state blocking capability in the devices.

IV. Conclusion

For the first time, high-performance normally-OFF p-GaN HEMTs with retained high-voltage blocking capability after forward gate breakdown have been demonstrated. High V_{BR}, low R_{ON}, high $I_{DS,max}$, large V_{th}, and nearly ideal SS were achieved simultaneously in the device. The distinct OFF-state blocking capability is attributed to the unique gate design properly managing the E-field at the p-GaN gate edge that is critical to realize reliable gate operation for high voltage applications.

Acknowledgment

The authors thank Dr. K. Cheng from Enkris Semiconductor Inc. for providing the epi wafer and the staff of the Nanosystem Fabrication Facility (NFF) and Material Characterization and Preparation Facility (MCPF) at HKUST for their technical support.

REFERENCES

[1] K. J. Chen, O. Häberlen, A. Lidow, C. L. Tsai, T. Ueda, Y. Uemoto, and Y. Wu, "GaN-on-Si power technology: Devices and applications," *IEEE Trans. Electron Devices*, vol. 64, no. 3, pp. 779–795, Mar. 2017. doi: 10.1109/TED.2017.2657579.

[2] H. Wang, J. Wang, M. Li, Q. Cao, M. Yu, Y. He, and W. Wu, "823 mA/mm drain current density and 945 MW/cm2 Baliga's figure of merit enhancement-mode GaN MISFETs with a novel PEALD-AlN/LPCVD-Si3N4 dual gate dielectric," *IEEE Electron Device Lett.*, vol. 39, pp. 1888–1891, Nov. 2018. doi: 10.1109/LED.2018.2879543.

[3] M. Tao, S. Liu, B. Xie, C. P. Wen, J. Wang, Y. Hao, W. Wu, K. Cheng, B. Shen, and M. Wang, "Characterization of 880 V normally off GaN MOSHEMT on silicon substrate fabricated with a plasma-free, self-terminated gate recess process," *IEEE Trans. Electron Devices*, vol. 65, no. 4, pp. 1453–1457, Apr. 2018. doi: 10.1109/TED.2018.2808345.

[4] M. Hua, J. Wei, G. Tang, Z. Zhang, Q. Qian, X. Cai, N. Wang, and K. J. Chen, "Normally-off LPCVD-SiN_x/GaN MIS-FET with crystalline oxidation interlayer," *IEEE Electron Device Lett.*, vol. 38, pp. 929–932, Jul. 2017. doi: 10.1109/LED.2017.2707473.

[5] R. Hao, W. Li, K. Fu, G. Yu, L. Song, J. Yuan, J. Li, X. Deng, X. Zhang, Q. Zhou, Y. Fan, W. Shi, Y. Cai, X. Zhang, and B. Zhang, "Breakdown enhancement and current collapse suppression by high-resistivity GaN cap layer in normally-off AlGaN/GaN HEMTs," *IEEE Electron Device Lett.*, vol. 38, no. 11, pp. 1567–1570, Nov. 2017. doi: 10.1109/LED.2017.2749678.

[6] M. Ishida, T. Ueda, T. Tanaka, and D. Ueda, "GaN on Si technologies for power switching devices," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3053–3059, Oct. 2013. doi: 10.1109/TED.2013.2268577.

[7] O. Hilt, R. Zhytnytska, J. Böcker, E. Bahat-Treidel, F. Brunner, and A. Knauer, "70 mΩ/600 V normally-off GaN transistors on SiC and Si substrates," in *Proc. IEEE 27th Int. Symp. Power Semiconductor Devices IC's (ISPSD)*, May 2015, pp. 237–240. doi: 10.1109/ISPSD.2015.7123433.

[8] N. E. Posthuma, S. You, S. Stoffels, H. Liang, M. Zhao, and S. Decoutere, "Gate architecture design for enhancement mode p-GaN gate HEMTs for 200 and 650V applications," in *Proc. IEEE 30th Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, May 2018, pp. 188–191. doi: 10.1109/ISPSD.2018.8393634.

[9] Y.-H. Wang, Y. C. Liang, G. S. Samudra, H. Huang, B.-J. Huang, S.-H. Huang, T.-F. Chang, C.-F. Huang, W.-H. Kuo, and G.-Q. Lo, "6.5 V high threshold voltage AlGaN/GaN power metal-insulator-semiconductor high electron mobility transistor using multilayer fluorinated gate stack," *IEEE Electron Device Lett.*, vol. 36, no. 4, pp. 381–383, Apr. 2015. doi: 10.1109/LED.2015.2401736.

[10] H. Jiang, C. W. Tang, and K. M. Lau, "Enhancement-mode GaN MOS-HEMTs with recess-free barrier engineering and high- k ZrO2 gate dielectric," *IEEE Electron Device Lett.*, vol. 39, no. 3 pp. 405–408, Mar. 2018. doi: 10.1109/LED.2018.2792839.

[11] S. Huang, X. Liu, X. Wang, X. Kang, J. Zhang, Q. Bao, K. Wei, Y. Zheng, C. Zhao, H. Gao, Q. Sun, Z. Zhang, and K. J. Chen, "High uniformity normally-OFF GaN MIS-HEMTs fabricated on ultra-thin-barrier AlGaN/GaN heterostructure," *IEEE Electron Device Lett.*, vol. 37, no. 12, pp. 1617–1620. Dec. 2016. doi: 10.1109/LED.2016.2617381.

[12] K.-Y. R. Wong, M. H. Kwan, F. W. Yao, M. W. Tsai, Y. S. Lin, and Y. C. Chang, "A next generation CMOS-compatible GaN-on-Si transistors for high efficiency energy systems," in *IEDM Tech. Dig.*, Dec. 2015, pp. 9.5.1–9.5.4. doi: 10.1109/IEDM.2015.7409663.

[13] H. Okita, M. Hikita, A. Nishio, T. Sato, K. Matsunaga, H. Matsuo, M. Mannoh, and Y. Uemoto, "Through recessed and regrowth gate technology for realizing process stability of GaN-GITs," in *Proc. 28th Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, Jun. 2016, pp. 23–26. doi: 10.1109/ISPSD.2016.7520768.

[14] M. Meneghini, I. Rossetto, C. D. Santi, F. Rampazzo, A. Tajalli, A. Barbato, M. Ruzzarin, M. Borga, E. Canato, E. Zanoni, and G. Meneghesso, "Reliability and failure analysis in power GaN-HEMTs: An overview," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2017, p. 3B-2.1-3B-2.8. doi: 10.1109/IRPS.2017.7936282.

[15] M. Ťapajna, O. Hilt, E. Bahat-Treidel, J. Würfl, and J. Kuzmík, "Gate reliability investigation in normally-off p-type-GaN cap/AlGaN/GaN HEMTs under forward bias stress," *IEEE Electron Device Lett.*, vol. 37, no. 4, pp. 385–388, Apr. 2016. doi: 10.1109/LED.2016.2535133.

[16] I. Rossetto, M. Meneghini, O. Hilt, E. Bahat-Treidel, C. De Santi, S. Dalcanale, J. Wuerfl, E. Zanoni, and G. Meneghesso, "Time-dependent failure of GaN-on-Si power HEMTs with p-GaN gate," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2334–2339, Jun. 2016. doi: 10.1109/TED.2016.2553721.

[17] M. Ruzzarin, M. Meneghini, A. Barbato, V. Padovan, O. Haeberlen, M. Silvestri, T. Detzel, G. Meneghesso, and E. Zanoni, "Degradation mechanisms of GaN HEMTs with p-type gate under forward gate bias overstress," *IEEE Trans. Electron Devices*, vol. 65, no. 7, pp. 2778–2783, Jul. 2018. doi: 10.1109/TED.2018.2836460.

[18] T.-L. Wu, D. Marcon, S. You, N. Posthuma, B. Bakeroot, S. Stoffels, M. Van Hove, G. Groeseneken, and S. Decoutere, "Forward bias gate breakdown mechanism in enhancement-mode p-GaN gate AlGaN/GaN high-electron mobility transistors," *IEEE Electron Device Lett.*, vol. 36, no. 10, pp. 1001–1003, Aug. 2015. doi: 10.1109/LED.2015.2465137.

[19] J. Kim, S.-K. Hwang, I. Hwang, H. Choi, S. Chong, H.-S. Choi, W. Jeon, H. S. Choi, J. Y. Kim, Y. H. Park, K. Y. Kim, J. B. Park, J. B. Ha, K. Y. Park, J. Oh, J. K. Shin, U. I. Chung, I. K. Yoo, and K. Kim, "High threshold voltage p-GaN gate power devices on 200 mm Si," in *Proc. 25th Int. Symp. Power Semiconductor Devices IC's (ISPSD)*, May 2013, pp. 315–318. doi: 10.1109/ISPSD.2013.6694412.

[20] N. E. Posthuma, S. You, H. Liang, N. Ronchi, X. Kang, D. Wellekens, Y. N. Saripalli, and S. Decoutere, "Impact of Mg out-diffusion and activation on the p-GaN gate HEMT device performance," in *Proc. 28th Int. Symp. Power Semiconductor Devices ICs (ISPSD)*, Jun. 2016, pp. 95–98. doi: 10.1109/ISPSD.2016.7520786.

[21] S. Stoffels, B. Bakeroot, T. L. Wu, D. Marcon, N. E. Posthuma, S. Decoutere, A. N. Tallarico, and C. Fiegna, "Failure mode for p-GaN gates under forward gate stress with varying Mg concentration," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2017, pp. 4B-4.1–4B-4.9. doi: 10.1109/IRPS.2017.7936310.

[22] M. Meneghini, I. Rossetto, M. Borga, E. Canato, C. D. Santi, F. Rampazzo, G. Meneghesso, E. Zanoni, S. Stoffels, M. V. Hove, N. Posthuma, and S. Decoutere, "Degradation of GaN-HEMTs with p-GaN Gate: Dependence on temperature and on geometry," in *Proc. IEEE Int. Rel. Phys. Symp. (IRPS)*, Apr. 2017, pp. 4B-5.1–4B-5.5. doi: 10.1109/IRPS.2017.7936311.