1.55-μm Lasers Epitaxially Grown on Silicon

Bei Shi , Yu Han , Qiang Li, and Kei May Lau

(Invited Paper)

Abstract—We have developed InP-based 1.55-μm lasers epitaxially grown on (001) Si substrates for photonics integration. To overcome the fundamental material challenges associated with mismatch III–V on Si hetero-epitaxy, a Si V-groove epitaxy platform was established, leading to device quality III–V nanostructures and thin films. Combining metal organic chemical vapor deposition grown 1.55-μm InAs quantum dots (QDs) and the InP/Si thin-film templates, we have achieved electrically driven 1.55-μm QD lasers on Si operating at room temperature. To reduce device footprint and energy consumption, a bufferless integration path by growing InP nano-ridge lasers on prepatterned silicon-on-insulators wafers has been explored. Material and device characterizations and an outlook for device component integration are discussed.

Index Terms—Integrated photonics, quantum dots, nano-lasers, wafer scale integration, MOCVD.

I. INTRODUCTION

TODAY, silicon (Si) photonics is progressing rapidly to enable photonic integrated circuits (PICs) with substantially reduced footprint, cost and energy dissipation. Integration of lasers on silicon substrates is essential to complete the Si-based PICs and on-chip interconnects [1], [2]. Although intense efforts have been devoted to silicon lasers such as porous silicon, silicon nanocrystals, erbium doped silicon oxide and Raman lasers, to date, these devices are mostly operating at optical pumping conditions. The lack of an efficient light emitter due to the indirect bandgap properties of silicon continues to pose a major roadblock [3]. In contrast to group-IV semiconductors, most of III–V compound semiconductors have direct bandgaps with excellent photon absorption and emission efficiency. III–V lasers with emission wavelengths at 1.3–1.55 μm grown on lattice-matched substrates have been commercialized for decades. III–V lasers directly grown on Si would offer a simple, low-cost and high-throughput integration path towards all optical components integrated on the same platform.

For more than 30 years, the crystal lattice mismatch issue between silicon and III–V laser materials was considered to be an intractable problem that has impeded monolithic integration of laser sources on silicon-based photonic integrated circuits. Tremendous effort has been devoted to overcoming several fundamental challenges, including a large mismatch in the lattice constants and thermal expansion coefficients, and the growth of polar materials on non-polar substrates. In addition to material incompatibility, a viable integration process that can be implemented in Si-photonics chips is needed. Over the past two decades, dramatic advances have been made driven by the emergence and development of advanced epitaxy techniques. Significant research has been directed to nanowire growth on (111) Si substrates, in which elastic relaxation in lateral directions leads to a significant increase in critical layer thickness [4]. Dislocation-free axial and core-shell structures have been reported by various groups [5]–[7]. Telecom-wavelength nanowire lasers on a silicon-on-insulators (SOI) platform operating in a single mode at room temperature was also demonstrated recently [8]. However, the compatibility issue due to the use of (111) oriented wafers and the challenges in achieving room-temperature continuous-wave (CW) electrical lasers are yet to be resolved. Another growing area that is attracting tremendous attention is direct growth of monolithic quantum dot (QD) lasers on Si. The three-dimensional quantum confinement and the near-discrete density of states of QDs give rise to superior performance surpassing their quantum well (QW) counterparts. As a result of the in-plane carrier confinement, QD lasers are much less sensitive to threading dislocations [2]. QD lasers grown on lattice mismatched Si have the potential of achieving low threshold current density, high temperature stability and long device lifetime without suffering the same fate as conventional GaAs QW lasers grown on Si [9]. Highly efficient 1.3 μm QD lasers on Si have been reported in the past few years [2], [10]–[13], highlighting the promise of this integration path for practical telecommunication and data-com applications. In addition to the nanowire and QD laser platforms, selective III–V patterned epitaxy on complementary metal-oxide-semiconductor (CMOS) compatible (001) Si wafers has been evolving rapidly. Notably, Aspect Ratio Trapping (ART) growth in narrow trenches has realized box-shaped GaAs nano-ridges with an impressively low

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threading dislocation density of $3 \times 10^6/\text{cm}^2$ [14]. Both In-GaAs/GaAs ridge lasers [15], [16] and InP distributed feedback laser array [17] have been demonstrated on standard 300 mm Si wafers with room-temperature pulsed operation. In another approach, template-assisted selective epitaxy (TASE) in conjunction with confined lateral epitaxial overgrowth (or "tunnel epitaxy") is being developed [18]–[20]. III–V/Si hetero-epitaxy is initiated from highly confined nucleation sites and expanded into micro-sized layers onto insulators. These important advances over the past few years generate significant attention towards monolithic integration platforms.

In this work, we present our research of 1.55 μm InP based QD lasers and nano-lasers grown on (001) Si through a V-groove ART epitaxy platform developed by metal organic chemical vapor deposition (MOCVD). Although extensive research has been carried out on the integration of 1.3 μm lasers on Si, progress in developing 1.55 μm InP-based lasers has been slow. However, it is a strategically important area, from traditional telecommunications to developing LiDAR technologies for autonomous driving. Optical fiber infrastructures have been built for the lowest optical power loss at the 1.55 μm wavelength, and InP-based long wavelength diode laser is the prevailing mature technology deployed in optical communication system for decades. In terms of life time, InP/InGaAsP laser diodes are in general more reliable than GaAs/AlGaAs based laser diodes, and less prone to rapid degradation phenomena caused by recombination enhanced dislocation climb [21].

This article is organized as follows. In Section II, we describe the V-groove ART epitaxy platform which leads to both coalesced InP on Si films and uncoalesced InP nanostructures for device applications. In Section III, 1.55 μm QD growth by MOCVD is first introduced, with an aim to achieve enhanced optical properties. We then present both optically and electrically pumped QD lasers on Si and discuss the possible schemes for light coupling into Si waveguides. In Section IV, we present the realization of InP nano-ridges with stacked InGaAs QW on SOI substrates. A discussion to achieve nano-photonic integrated circuits is proposed. Finally, a brief summary is given in Section V.

II. V-GROOVE ART EPITAXY PLATFORM

We developed the V-groove ART platform using selective area growth (SAG) in lithographically defined line openings on (001) Si substrates using SiO_2 as growth mask [22]. The SiO_2 stripes lie along the [110] direction. V-shaped trenches with {111} facets were formed by self-limited etching in diluted potassium-hydroxide (KOH) solutions.

Direct growth of InP on the Si V-grooves is a non-trial task. The 8% lattice mismatch, the large migration mobility of the In adatoms and the increased difficulty in the surface cleaning of nano-sized trenches could result in prounced non-uniformity and high-density planar defects. Planar defects running in the plane perpendicular to the trench direction can't be trapped by the V-groove epitaxy or the ART method [14]. Therefore, we first developed GaAs nano-ridges and thin films on V-grooved Si, which serves as an intermediate buffer for subsequent InP epitaxy. A two-step method consisting of a low-temperature
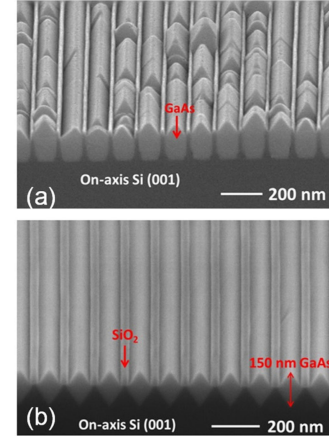

Fig. 1. SEM images of SAG of GaAs on line patterned (100) Si substrates without (a) and with (b) V-grooves.
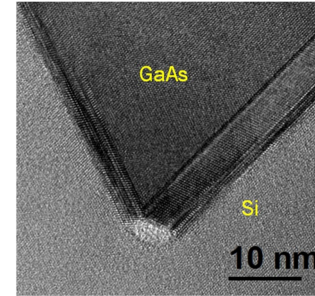

Fig. 2. High resolution TEM image at the GaAs/Si hetero-interface revealing stress relaxation through a highly twined region with thickness less than 10 nm.

nucleation layer and a high-temperature main layer growth was used for GaAs SAG. As shown by the SEM images in Fig. 1, the use of V-grooves significantly reduced morphological defects including planar defects observed in cross-sectional and plan-view transmission electron microscopy (TEM) studies. More importantly, because a single step on the Si (111) surface has the height of one Si (111) double-layer (0.31 nm), antiphase-domains (APB)-free growth can be obtained without using offcut Si, showing better compatibility with mainstream CMOS technology.

Fig. 2 presents a cross-sectional TEM image taken at the GaAs/Si hetero-interface. Instead of forming misfit dislocations, the lattice mismatch was accommodated by a highly twinned region less than 10 nm thick. Defect-free GaAs was realized on top of this special stress relaxation layer, although more TEM inspection along the trench direction revealed some threading dislocations propagating towards the oxide sidewalls [22]. Nevertheless, building on the unique strain relaxation mechanism in GaAs V-groove epitaxy, we have developed both coalesced InP thin films and uncoalesced InP ridge structure from a single trench, which will be discussed respectively.

A. Coalesced InP Thin Films on V-Grooved Si

To grow low defect density InP thin films on Si, the SiO_2 ridges in Fig. 1(b) were removed and the GaAs nano-crystals were merged into a coalesced GaAs-on-V-grooved-Si (GoVS)
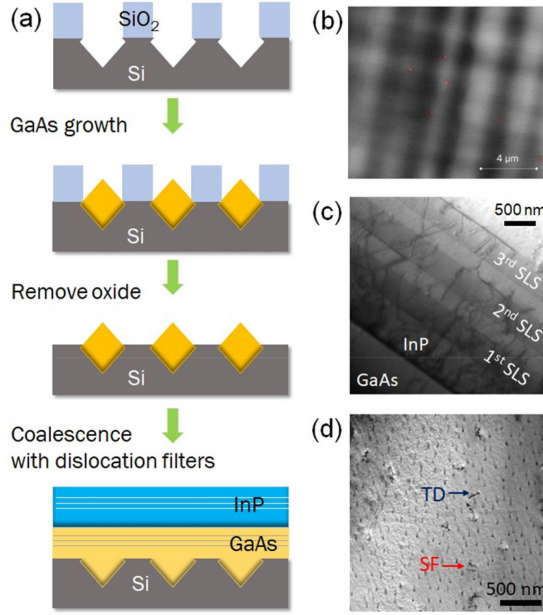
Fig. 3. (a) Growth process for InP on V-grooved Si. (b) An ECCI image taken from a GoVS template with dislocations circled. (c) A cross-sectional TEM image showing InGaAs/GaAs SLS dislocation filters in InP. (d) A plan-view TEM image taken from InP on V-grooved Si.

TABLE I
SUMMARY OF DISLOCATION FILTERING APPROACHES AND SURFACE DEFECT
DENSITIES FOR III–V GROWN ON SI

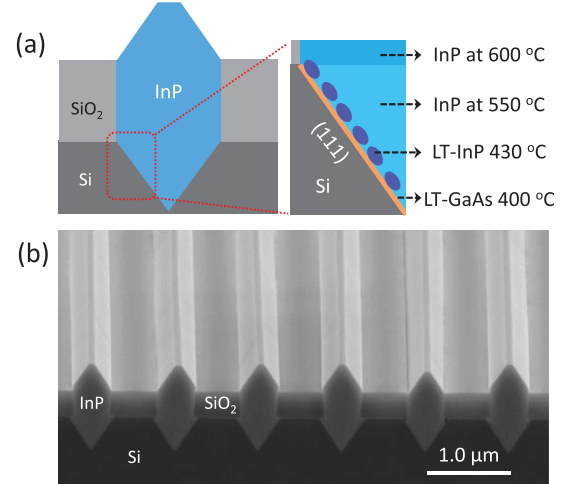| Epitaxial material	Dislocation filter layers	Buffer thickness (μm)	Characterization	Surface defect density
GaAs/Si	1 set of 10× {10 nm $Al_{0.3}Ga_{0.7}As$/8 nm GaAs}	2 μm GaAs	ECCI	9×10^7/cm^2 [12]
GaAs/Si	3 sets of 10× {10 nm $In_{0.16}Ga_{0.84}As$/10 nm GaAs}	3.1 μm GaAs	ECCI	6×10^6/cm^2
InP/GaAs /Si	2 sets of 5× InAs/InP QDs (h_{QD}=5 nm)	0.6 μm GaAs+2.8 μm InP	PV-TEM	3×10^8/cm^2 [23]
InP/GaAs /Si	3 sets of 10× {10 nm $In_{0.6}Ga_{0.4}As$/30 nm InP}	2.3 μm GaAs+3.1 μm InP	PV-TEM	1.5×10^8/cm^2 [25]

Fig. 4. (a) Schematic of the growth sequence of InP nano-ridges on V-groove Si trenches. (b) SEM image of InP nano-ridge arrays grown inside Si trenches.

template by regrowth [22]. Due to the trapping effect from the tip of the Si ridge, most of the twin defects in the sub-10nm stress relaxing layer were confined in the V-shaped trenches. InP was grown on the GoVS templates using a two-step growth process. A schematic of the procedure is given in Fig. 3(a). Both GaAs and InP are free of antiphase boundaries, according to large-area inspection by AFM and SEM.

To reduce the threading dislocations generated in the coalescence process and from the InP/GaAs hetero-interface, dislocation filtering layers were used in both GaAs and InP. Various defect characterization approaches, including x-ray diffraction rocking curve measurements, plan-view TEM and electron channeling contrast imaging (ECCI), have been implemented and compared to obtain reliable defect densities. As a non-destructive and quantitative characterization technique capable of visualizing individual defects directly on the sample surface at a given diffraction condition, ECCI is especially useful for statistical analysis of defects over large areas. A threading dislocation density (TDD) of 7×10^7 cm^{-2} was measured from a 2 μm GoVS template. A lower TDD value of 6×10^6 cm^{-2} was measured from a 3.1 μm GoVS template with 3 sets of $10 \times$ {10 nm $In_{0.16}Ga_{0.84}As$/10 nm GaAs} strained layer superlattices (SLSs) filters. Fig. 3(b) displays one ECCI image captured from the GoVS template, in which 6 dislocations were identified from an area of 181 μm^2. For InP grown on top of the GoVS template, we have investigated both QDs and SLSs as dislocation filters [23]–[25]. The cross-sectional TEM image in Fig. 3(c) shows the defect trapping effect from a sample with 3 sets of 10 periods of $In_{0.6}Ga_{0.4}As$/InP (10/30 nm) SLSs. A surface defect density of 1.5×10^8 cm^{-2} was determined by plan-view TEM characterization (Fig. 3(d)). These templates form the basis for our research on QD laser growth on Si. Table I

summarizes GoVS and InP-on-Si templates undergoing various dislocation filtering approaches. Achieving a low dislocation density in InP-on-Si is more challenging due to several reasons. The smaller coefficient of thermal expansion (CTE) for InP/Si ($\sim$77%) hampers the effective operation of thermal cycle annealing (TCA) technique, which is expected to thermally propel the dislocations into coalescence. The dislocation filters in InP buffers is generally more challenging to grow due to issues such as phase separations in highly strained InGaAs or InGaP interlayers or superlattices with much larger indium compositions than those applied in GaAs/Si material system [26], [27]. The phase separation would consequently lead to indium clustering and degrade the efficiency of these dislocation filters.

B. Uncoalesced InP ridges on V-Grooved Si

Bypassing the complex buffer designs in coalesced thin film templates for laser integration, we have developed another integration scheme, uncoalesced InP ridge structures by SAG, for nano-lasers on Si. This is built on the process of GaAs SAG in V-grooves that is scalable from nanometer to micrometer scale length and extendable to InP and GaSb material families [28], [29]. In order to keep good optical mode confinement within III–V nano-cavities, V-groove trench patterns with width around 450 nm were chosen. As depicted in Fig. 4(a), the epitaxy started with a low-temperature GaAs stress relaxing layer, which is
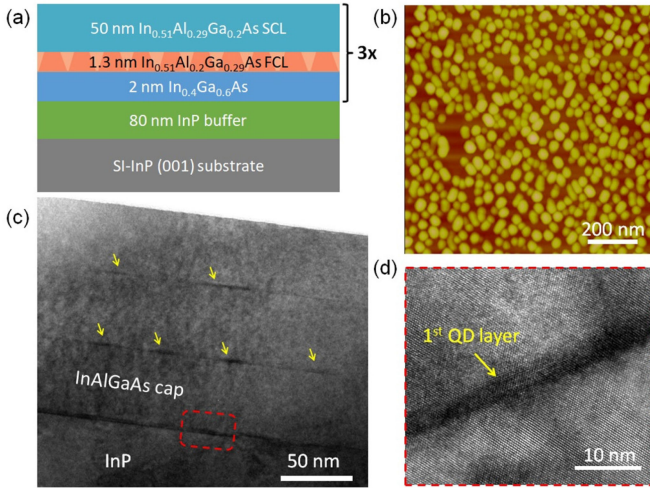
Fig. 5.   Schematic diagram of a three-stack InAs/InAlGaAs QD structure on InP (001) substrate. (b) 1×1 μm^2 AFM image of the uncapped single layer QDs on InP. (c) Cross-sectional TEM image of the stacked QDs (QDs indicated by yellow arrows). (d) High-resolution TEM of a single buried InAs QD.

essential to facilitate initial nucleation and accommodate the 8% lattice mismatch between InP and Si. This was followed by an InP nucleation layer grown at 430 °C. With the help of the GaAs initial layer, dense InP nano-islands instead of giant InP clusters were formed at this stage. These small InP islands then coalesced into continuous InP nano-ridges during the subsequent InP growth at 550 °C and 600 °C. The resultant InP ridge arrays show (111) top facets with high uniformity across large areas as indicated by the SEM photo in Fig. 4(b). Benefiting from the defect necking effect of the ART technique, the upper region of the InP nano-ridge is dislocation-free, and the density of planar defects is around 1.0/micron. These InP nano-ridge platform was initially developed on bulk (100) Si wafers, and recently demonstrated on SOI wafers. The InP ridges were combined with InGaAs quantum structures for telecom band nano-lasers, which will be detailed in Section IV.

III. C-BAND QD LASERS ON SI

Compared with the prevailing InAs/GaAs QDs, the small lattice mismatch (∼3.2%) and complex strain distribution in InAs/InP system introduce serious size and shape dispersions in QDs, leading to large inhomogeneous broadening [30]. We chose to develop MOCVD growth of InAs/InAlGaAs QDs on InP substrates before QD laser structures on Si substrates.

A. InAs/InAlGaAs QDs Growth by MOCVD

Fig. 5(a) shows the basic growth structure of a three-stack InAs/InAlGaAs QDs on semi-insulating InP (001) substrate. To improve the optical performance of the InAs/InAlGaAs QDs by MOCVD, a double-cap procedure was developed. Firstly, 3.6 monolayer (ML) InAs QDs were grown at a low temperature of 510 °C and a low V/III ratio of 0.4. After a 5 s growth interruption forming the self-assembled QDs, a very thin low temperature (LT) InAlGaAs cap was immediately deposited to preserve the QDs morphology. Subsequently, a thicker high

temperature (HT) InAlGaAs spacer was grown to minimize dot height dispersion and improve the material quality [31].

Fig. 5(b) shows a typical atomic force microscopy (AFM) image of the single layer of uncapped InAs QDs, revealing a density of ∼4.5 × 10^{10} cm^{-2} and an average diameter of ∼42 nm. Fig. 5(c) demonstrates the morphology of buried QDs by cross-sectional TEM. The buried QDs are truncated and their height is determined by the thickness of LT-InAlGaAs first cap layer. It is noteworthy to point out that the density for stacked QDs can be controlled by tuning the thickness and composition of the HT-InAlGaAs spacer. The high-resolution TEM image in Fig. 5(d) presents the dot-in-well (DWELL) structure, where the single buried InAs QD is surrounded by a top $In_{0.51}Al_{0.2}Ga_{0.29}As$ cap and a bottom $In_{0.4}Ga_{0.6}As$ strained buffer. No defects are observed in the QDs region, which is favorable for the QD laser operation.

B. 1.55 μm Optically Pumped QD Microdisk Lasers on Si

Direct epitaxy of 1.55 μm QD lasers on Si by MOCVD is one of the most desirable pursuits towards integrated silicon photonic circuits, particularly from the manufacturing perspective [32]. We first fabricated 1.55 μm continuous wave optically pumped QD microdisk lasers (MDLs) epitaxially grown on Si [33]. Different from the conventional FP lasers which generally have a large footprint, the microdisk lasers are promising compact light sources. Owing to the unique combination of high-quality whispering-gallery modes (WGMs) of the microdisks and the lesser sensitivity of QDs to side-wall defects, initial MDLs can successfully CW lase at liquid helium temperature with a low threshold of 1.6 mW. Further improving the material gain of the multiple QD stacks, we were able to realize room-temperature lasing with an ultralow threshold power of 2.73 μW from subwavelength MDLs (diameter of 1.5 μm) [34]. The complete growth structure is schematically shown in Fig. 6(a). An anti-phase boundary (APB)-free InP buffer was achieved on a nominal (001) Si by MOCVD. The GaAs buffer is helpful for accommodating both lattice and thermal expansion differences between InP and Si substrate and providing a smoother InP surface front with much reduced stacking fault density. Careful tuning of the nominal thickness and V/III ratio of InAs QDs led to a significant increase in the photoluminescence (PL) intensity as well as a remarkable reduction in the full-width at half maximum (FWHM) value. Here the 7-layer InAs/InAlGaAs QDs were optimized on InP substrates to achieve a desirable PL emission. The same QD structure was repeated on the InP-on-Si template for a direct comparison in terms of both optical emission and microdisk laser characteristics. As demonstrate in Fig. 6(b), the peak PL intensity of MDLs on Si is 3.5 times lower than those on the InP native substrate, while the FWHM values are comparable. The degraded PL intensity on Si is partially resulted from defective InAs clusters formed inside the active region (Fig. 6(c)), due to the bumpy surface areas of the InP-on-Si substrate. The QD density on InP-on-Si template is around 4 × 10^{10} cm^{-2}, slightly lower than that on InP native substrate (5 × 10^{10} cm^{-2}). A representative MDL is characterized by the 70° tilted scanning
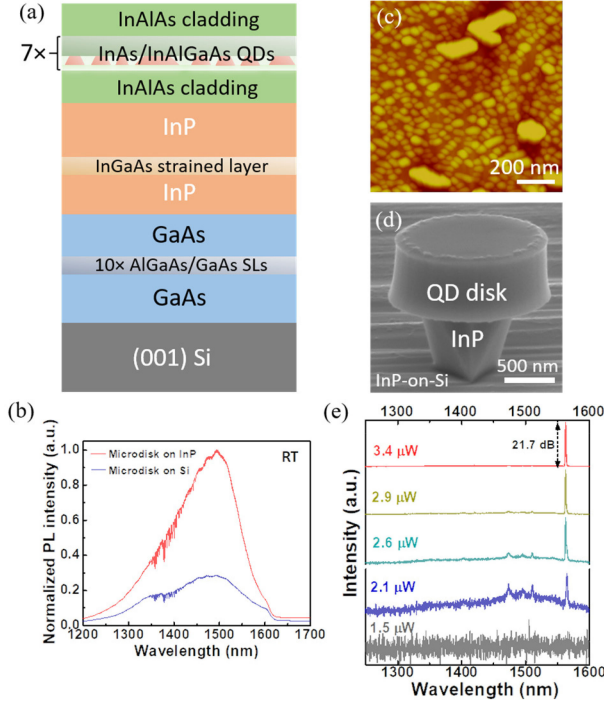
Fig. 6. (a) Schematic showing the complete 7-layer QD MDL epi structure on nominal (001) Si. (b) RT-PL spectra of MDLs on InP and Si. (c) Typical 1×1 μm^2 AFM image of the surface single layer QDs on InP-on-Si template. (d) 70° tilted SEM of one subwavelength MDL device. (e) Lasing spectra of the subwavelength MDLs at room temperature as a function of pump power.

electron microscope (SEM) in Fig. 6(d). Although nonradiative surface recombination and Auger recombination processes consume a larger percentage of generated carriers in small subwavelength lasers, gain in the InAs/InAlGaAs QDs active medium can effectively surmount the surface recombination. The subwavelength MDLs therefore yield a low threshold of 2.73 ± 0.23 μW with a high cold cavity quality factor (Q) value of 1563, as shown in the power-dependent PL spectra in Fig. 6(e). Moreover, the subwavelength MDLs can successfully operate above 60 °C with a characteristic temperature T_0 as high as 123 K, which is among the best reported T_0 values for QD MDLs on III–V substrates [35], [36].

C. Electrical QD Laser Diodes Directly Grown on (001) Si

We have grown and fabricated 1.5 μm room-temperature electrical QD lasers on CMOS-compatible (001) Si substrates [25]. Fig. 7(a) shows the cross-sectional SEM of the compete epi structure. A V-groove patterned Si (001) substrate was employed for the GaAs and subsequent InP buffers growth. To minimize the electrical contact loss and sidewall nonradiative recombination, the mesa dry-etching was carefully tuned to ensure a smooth sidewall and bottom surface, resulting in good n-metal contact with reduced series resistance of 5–8 Ω. A very clean and mirror-like facet (not shown here) is achieved for minimized cavity loss. The crystalline quality of InP-on-V-grooved Si with GaAs intermediate buffer was improved by inserting three sets of 10-nm In$_{0.6}$Ga$_{0.4}$As/ 30-nm InP strained layer superlattices (SLSs) as effective dislocation filters. The surface defect density
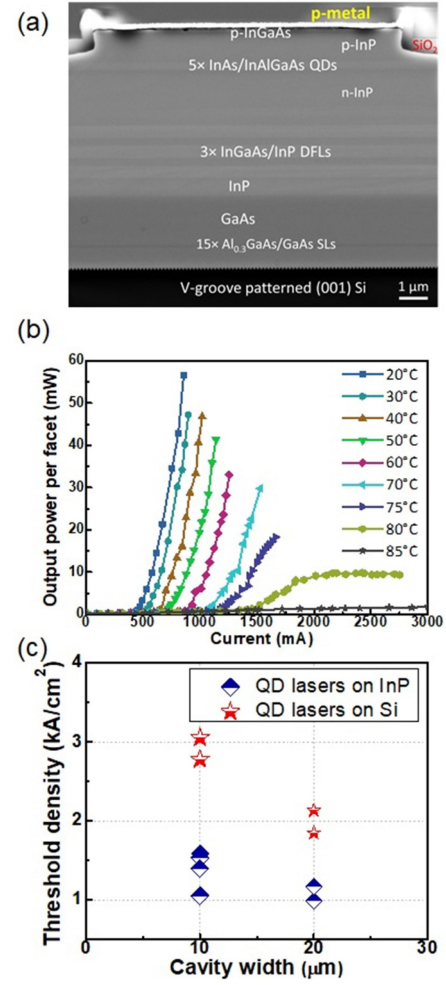

Fig. 7. (a) Cross-sectional SEM of the as-fabricated electrical QD laser diode on V-grooved Si. (b) Dependence of LI curves on temperature from 20 °C to 85 °C. (c) Threshold current density distribution of QD lasers on InP and Si, at varied cavity widths.

reaches 1.5×10^8 cm^{-2}, characterized by the plan-view TEM technique in Fig. 3(d). This helps reduce nonradiative free carrier recombination in the active region. A five-layer InAs/InAlGaAs QDs with improved optical performance was grown on the smooth InP buffer. The surface roughness for the 3-μm-thick InP buffer is reduced to 2 nm across a 10×10 μm^2 scan area. The inhomogeneous broadening associated with QDs was alleviated by optimizing the thickness of the double InAlGaAs cap layers, as evidenced by the reduced room-temperature PL FWHM value of 61.6 meV for the five-layer QDs. It is noteworthy that a 7-layer QD laser structure was grown on the InP substrate to enhance the material gain, yet for electrically-pumped lasers on Si, the QD layer number here is specifically optimized at 5 periods. This is due to the different effects of some crucial growth parameters (e.g., QD nominal thickness, V/III ratio, LT-InAlGaAs capping layer thickness) on the optical efficiencies of QDs grown on InP and Si, respectively. Further increasing the QD layer number on Si from five to seven periods would lead to the saturation of ground-state PL intensity and a more severe inhomogeneous broadening [25].
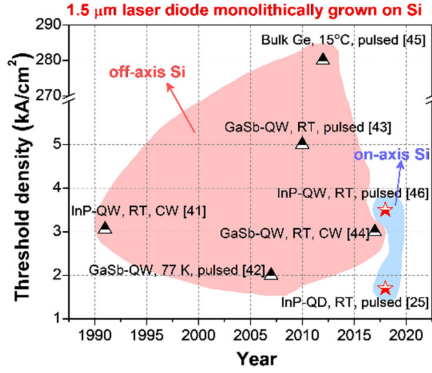
Fig. 8.   Benchmark of the 1.5 µm band laser diodes monolithically grown on Si.
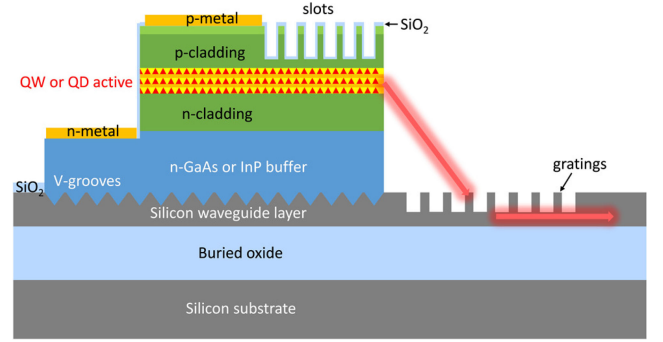

Fig. 9.   Schematic illustration of the proposed vertical divergent coupling by selective area epitaxy approach. The slots are formed on III–V top cladding and SOI waveguide is etched with surface gratings.

Ridge waveguide laser diodes were then fabricated using standard lithography, dry-etch and metallization techniques. The Si-based QD lasers exhibit decent lasing thresholds under pulsed current injection (1.6–3 kA/cm^2). Fig. 7(b) presents temperature-dependent LI curves for a 20 µm × 1 mm device, with the maximum operation temperature up to 80 °C. The characteristic temperature is calculated to be 58.7 K, which can be further improved by the p-type modulation doping of the QDs [37]. For reference, QD lasers grown on n-InP native substrate was fabricated simultaneously to evaluate the influence of defects in the InP buffer on the QD lasers. The lasers on InP (001) substrate can operate with CW electrical pumping condition. The dependence of lasing thresholds on the ridge cavity widths is summarized in Fig. 7(c). It is observed that the threshold density increases for narrower ridges due to a more severe sidewall roughness influence [38], as well as a larger thermal resistance as devices shrink [39]. Generally, the lasing thresholds on InP substrate (as low as ∼1 kA/cm^2) is half of those on Si under pulse current injection. This is ascribed to composite factors including a higher defect density and a rougher surface front of the InP-on-Si template, as well as a residual thermal strain in the InP buffer, which affects the QDs morphology and shifts the QDs peak wavelength. Meanwhile, compared with the state-of-the-art 1.55 µm QD lasers on InP substrates equipped with the lowest threshold of 190 A/cm^2 [40], the InAs/InAlGaAs QD active material grown on our InP substrates requires a further optimization by minimizing the impurity atoms such as carbon and oxygen inside the QD matrix.

Fig. 8 presents a comparison of 1.5 µm band laser diodes monolithically grown on Si. To ensure the full compatibility of III–V lasers with the silicon photonic components, it is necessary to grow lasers on an on-axis (001) Si or SOI substrate. The QD laser on InP-on-Si presented in this work demonstrated a low threshold and a good temperature stability, attributed to the utilization of QDs as the gain material. Future efforts should be focused on lowering the defect density of the InP buffer to realize CW operation.

D. Perspective: Light Coupling to Si Waveguide

Although present research has been concentrated on discrete lasers on the Si platform, integration of the active devices with passive Si waveguides is the ultimate goal. Several feasible approaches have been proposed leveraging selective epitaxial growth. In Ref. [47], a butt-joint coupling to Si rib waveguide and evanescent coupling to III–V waveguide layer were considered. The potential challenge of those methods is related with a highly resistive electrical injection through the defective III–V/Si interfaces.

Another promising approach, as we proposed here, is to combine the well-developed III–V lasers on V-grooved SOI substrates with the vertical divergent coupling [48]. The scheme is drawn in Fig. 9. First, a III–V buffer is selectively grown on the V-groove patterned trench region, while the nearby Si waveguide layer will be etched into surface grating structures for an effective coupling. The surface of the laser claddings is etched into slot structures for the vertical divergent beam output. The advantage of this method is that there is no critical limit on the thickness of III–V buffers. Moreover, different categories of laser structures can be implemented using this approach, leveraging standard laser fabrication techniques. Yet there remain some concerns related to the epitaxy process. Loading effects and parasitic hillocks might form during selective area epitaxy when the III–V trenches are separated far apart. This situation could become worse when the low-temperature QDs growth step is introduced. Further study is required to identify a compatible integration process to bring III–V laser structures on a SOI platform.

IV. NANO-LASERS ON SOI

Reducing the physical footprint of lasers on Si is highly desirable for low power consumption and compact photonic integrated circuits [49]. Research of III–V nano-scale light emitters flourished in the early 2010s, with stimulated emission demonstrated from various nanostructures such as GaAs, InP, InGaAs and GaSb [50]–[53]. To attain a strong mode confinement and sufficient optical feedback, these nano-lasers were usually removed from the as-grown substrate and transferred onto a low-index substrate for optical excitation. The length, position, and orientation of the transferred nano-lasers are completely random. Advanced growth techniques and cavity designs have been adopted later to realize direct on-chip laser emission from as-grown nanowires [6]–[8]. However, the use of (111)
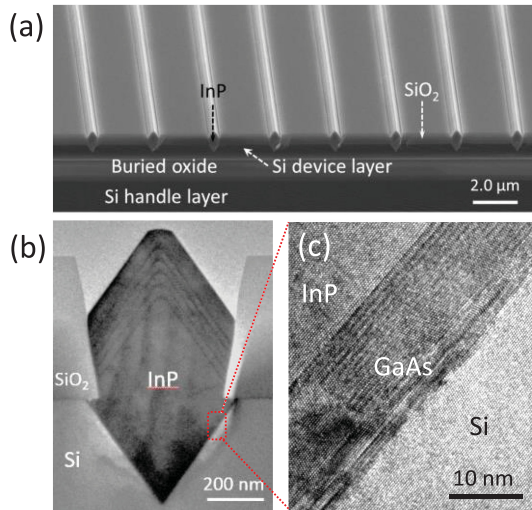
Fig. 10. (a) Tilted-view SEM image of well-aligned InP nano-ridges grown on SOI. (b) Cross-sectional TEM image of one InP nano-ridge. (c) High-resolution TEM photo of the III–V/Si interface with high density of planar defects.
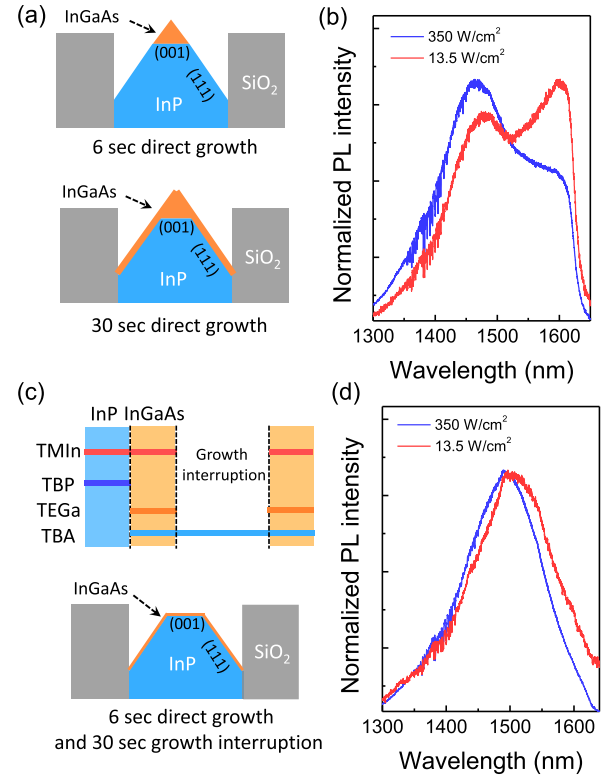

Fig. 11. (a) Schematic of InGaAs layer directly grown on multifaceted InP ridge buffer. The size of the (001) and {111} are not drawn in scale. (b) Room temperature PL spectra of directly grown InGaAs. (c) Schematic of InGaAs grown on multi-faceted InP ridge buffer with growth interruption. (d) Room temperature PL spectra of InGaAs layer grown with growth interruptions.

oriented Si substrates continues to present a barrier for industrial deployment. Additionally, applications in data communications requires laser emission at telecommunication wavelengths – the 1.3 μm and the 1.5 μm band. In this section, we will discuss 1.5 μm InP-based nano-lasers directly grown on (001) silicon-on-insulators. Our analysis will focus on the design of telecom nano-lasers and the implications on future Si based nano-scale PICs.

A. InP/InGaAs Nano-Ridges Grown on SOI

The growth of InP nano-ridges on commercial SOI was carried out using a similar process to those on other pre-patterned Si wafers (see Fig. 4(a)). To minimize light coupling between adjacent nano-ridges, the spacing between neighboring nano-ridges was increased from 550 nm to 2.35 μm (see the SEM image in Fig. 10(a)). Fig. 10(b) presents a cross-sectional TEM image of one InP nano-ridge grown on SOI. We observe a multi-faceted growth front consisting of two convex {111} side facets and one top {001} facet. Development of this ridge structure stems from the interfacial energy between InP and oxide sidewall and the tendency to minimize total surface energy [54]–[56]. Fig. 10(c) displays a high resolution TEM image of the InP/Si interface. High density planar defects are formed to relieve the strain induced by lattice mismatch. Consequently, the InP ridge buffer exhibits excellent crystalline quality (see Fig. 10(b)).

The multi-faceted InP buffer complicates the insertion of lattice-matched InGaAs QW structures to be used for lasing. As shown in Fig. 11(a), direct epitaxy of InGaAs on InP ridge leads to an initial growth at the tip region, followed by extended growth at the {111}-oriented ridges. This gives rise to carrier localization at the tip area due to composition inhomogeneity. Such a phenomenon can be explained by the different self-limiting growth profiles of InP and InGaAs [57]. Fig. 11(b) displays the room temperature PL spectra of InGaAs ridge QWs. The growth

time for a single InGaAs well is 30 sec. Under low excitation levels, the main peak at 1600 nm corresponds to light emission from the tip region, whereas the peak around 1450 nm indicates light emission from the ridge QWs. At increased excitation levels, the peak at 1450 nm become more pronounced due to the much larger material volume of the ridge QWs. Carrier localization at the tip region broadens the emission spectra, drains charged carriers from the ridge QWs, undesirable for achieving high material gain of the ridge QWs.

To grow InGaAs QWs without carrier localization, chemical mechanical polishing (CMP) could be used to smoothen the multi-faceted InP ridge buffer into a single (001)-oriented InP surface, as reported in Ref. [58]. However, in this case only one InGaAs flat QW could be formed, and the faceting process of stacking multi-QWs requires more CMP steps. Without using CMP, we developed a unique "cycled growth procedure" to minimize the carrier loss issue. The key is tailoring the self-limiting growth profile of InGaAs via introduction of growth interruptions. As shown by the growth sequence in Fig. 11(c), after the growth of the InP ridge buffer, TBP were switched off with TEGa and TBA introduced into the reactor to initiate the InGaAs growth for a duration of 6 sec. Then all the group-III precursors were switched off, leaving the ultra-thin InGaAs layer in a TBA ambient for 30 sec. Due to the cutoff of group-III precursors, the deposited InGaAs layer starts to migrate from the tip region

and redistribute uniformly along the {111}-oriented ridges. We found that 6 sec of InGaAs growth combined with 30 sec growth interruption results in a uniform InGaAs coverage at the {111} facets with a thickness around two atomic layers. Thicker In-GaAs and shorter growth interruption will inhibit the migration of InGaAs from the tip region to the ridge region and thereby lead to multi-peaked emission spectra. This process could be repeated for several cycles to reach the desired InGaAs well thickness. Fig. 11(d) presents the room temperature PL spectra of InGaAs ridge QWs grown using this "cycled growth procedure". The total growth time (the duration that TMIn, TEGa and TBA flowed into reactor) of the QW is the same as that shown in Fig. 11(b). Compared with the broad and double-peaked PL spectra obtained by continuous hetero-epitaxy, single-peaked PL spectra with a reduced line-width has been achieved using the cycled growth procedure. The emission peak hinges on the thickness of the InGaAs QW and thus depends on the overall growth cycles. We may also tune the emission wavelength by tailoring the indium fraction of the InGaAs QW.

B. Nano-Laser Array on SOI

Stimulated emission inside nano-cavities demands a tight mode confinement within the gain medium. Starting with the as-grown InP/InGaAs nanoridges on SOI substrates, we selectively removed the oxide spacers using a buffered oxide etch. To minimize light leakage into the underlying Si layer, a diluted KOH-based selective wet etch was carried out to undercut the Si and form a triangular-shaped post supporting the nano-ridges. We finalized the nano-lasers through etching the nano-ridges into different lengths using focused ion beam milling [59], [60]. The ability to precisely define the length and position of the nano-cavities through top-down lithography processes differentiates this work from most previous randomly transferred nano-lasers.

Figs. 12(a)–(c) display the calculated electrical field distribution inside different nano-laser configurations. We only show mode profiles of TE_{01} since this transverse mode exhibits the largest overlap with the InGaAs QWs and the largest optical feedback from the end-facets [59]. For as-grown InP nano-ridges, light is weakly confined with large leakage into the underlying Si device layer (see Fig. 12(a)). When the oxide spacers are removed and Si device layer is undercut, light is more confined within the nano-ridge and partially coupled into the supporting Si pedestal (see Fig. 12(b)). As the volume of the Si pedestal reduces, light is tightly confined within the nano-ridge. Although the design in Fig. 12(c) might be preferred for low threshold lasing, the one in Fig. 12(b) could enable light coupling into Si waveguides and thus possible integration with Si photonics on the same chip.

Fig. 12(d) presents a tilted-view SEM photo of the well-aligned and densely packed InP/InGaAs nano-laser array on SOI. Room temperature lasing at the 1.5 μm telecom band is achieved under optical excitation. Fig. 12(e) displays the PL spectra (plotted in a log scale) near threshold of one nano-laser with a length of 50 μm. We detected well-defined Fabry-Perot
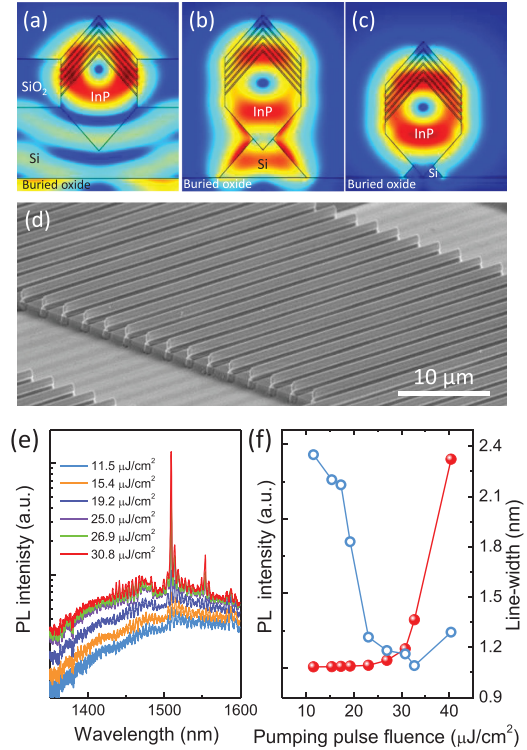

Fig. 12. (a)–(c) Calculated mode profiles of as-grown InP nano-ridge, InP nano-ridge with large Si pedestal, and InP nano-ridge with small Si pedestal. (d) Titled-view SEM image of InP/InGaAs nano-laser array on SOI. (e) Room temperature PL spectra of a nano-laser with a length of 50 μm. (f) The evolution of emission intensity (plotted in log scale) and line-width as pumping pulse fluence increases.

resonance peaks under low excitation levels. As the excitation increases, the mode at 1509 nm reaches threshold and stands out from the broad background emission. The lasing behavior also manifests itself by the clamping of spontaneous emission around threshold. Fig. 12(f) delineates the evolution of peak intensity and line-width at 1509 nm as the pumping levels strengthens. As a result of the carefully designed InGaAs active regions and nano-scale laser cavities, a low lasing threshold around 30 μJ/cm^2 is achieved.

C. Perspective: Nano-Photonic Integrated Circuits

The eventual Si based PICs require on-chip integration of coherent laser sources and Si optical components such as waveguides, splitters and (de)multiplexers [61]. Micro-scale III–V light sources need to be processed on planar III–V/Si complaint substrates with a buffer layer up to a few microns thick. While such a thick buffer is necessary for reducing defect densities, it also complicates the integration of lasers with other photonic devices fabricated on the underlying Si substrate. For III–V nano-lasers directly grown in a single trench on SOI by the ART approach, most of the defects are confined within an ultra-thin nucleation layer at the III–V/Si interface. The intimate placement of III–V nano-lasers with Si device layer can greatly simplify the integration process, and points to potential nano-PICs on SOI. As shown by the
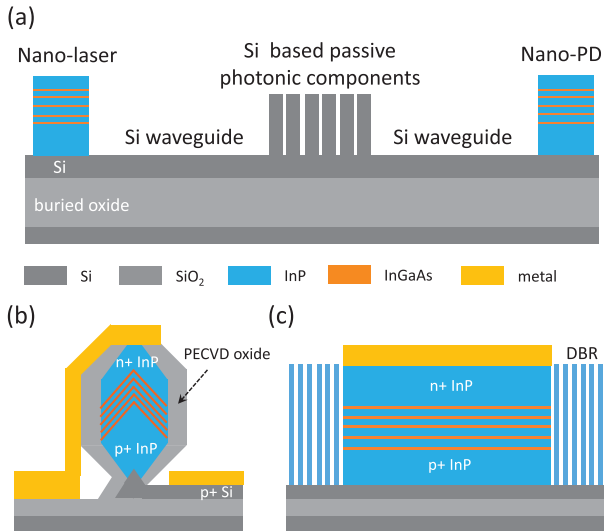
Fig. 13. (a) Schematic of the proposed nano-photonic integrated circuits on (001) SOI. (b) Cross-sectional schematic of the proposed electrically injected nano-laser on SOI. (c) Schematic of the nano-laser along the cavity direction.

proposed structure in Fig. 13(a), the envisaged nano-PICs consist of electrically driven III–V nano-laser, Si based passive photonic components, and III–V nano-photo-detectors. Light coupling between III–V lasers/detector and Si waveguides could be achieved through fabricating Si waveguides lying underneath the III–V lasers/detectors (see Fig. 13(a)), while other Si photonic elements could be produced nearby for on-chip light manipulation.

Similar to other nano-sized devices, it is extremely challenging to realize electrically driven nano-lasers on Si. First, III–V nano-structures must be highly doped for efficient carrier injection; Secondly, optical modes should be tightly confined within the nano-cavity. And finally, the metal pads must be routed in a way to avoid any overlap with the optical modes minimizing propagation loss [62], [63]. These requirements can be easily met in traditional micrometer/millimeter scale laser bars but become exceedingly difficult for nano-scale laser emitters. Based on our optically pumped nano-lasers on SOI, we have devised electrically driven nano-lasers directly grown on (001) SOI wafers. Fig. 13(b) delineates the cross-sectional structure of the proposed device, and Fig. 13(c) presents the schematic along the cavity direction. The InP nano-ridges can be readily doped into the PN junctions as the growth process resembles traditional planar epitaxy [64]–[66]. Oxide spacers could be employed to encapsulate the InP nano-ridge to achieve tightly confined light with minimized Si pedestals. Charged carriers are injected from openings (n-metal contact) atop the nano-ridge and collected via metal pads (p-metal contact) patterned on the highly doped Si device layer. Because there is no electrical field distribution at the nano-ridge tip (see Figs. 12(a–c)) and the p-metal on Si can be patterned far from the nano-cavity, propagation loss through metal pads could be minimized. Advanced cavity designs such as distributed Bragg reflectors, DFB lasers, and photonic crystal cavities can also be implemented to obtain low threshold lasing.

V. SUMMARY

Building on the V-grooved ART epitaxy platform, we have achieved high quality InP nano-ridges and thin films on (001) Si substrates. Electrically driven 1.55 μm QD lasers were demonstrated by engineering an InP/Si buffer technology and optimizing the MOCVD-grown InAs quantum dots. Additionally, we have developed a buffer-less epitaxial process to realize 1.55 μm InP/InGaAs nano-lasers on (001) SOI substrates. The material and device characteristics and possible integration approaches with Si photonics are discussed.

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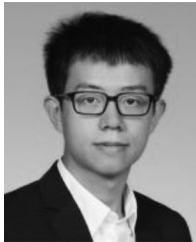
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