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Interface passivation and trap reduction via hydrogen fluoride for molybdenum disulfide on silicon oxide back-gate transistors

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Interface passivation and trap reduction via hydrogen fluoride for molybdenum disulfide on silicon oxide back-gate transistors

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Abstract

Layered semiconductor molybdenum disulfide (MoS_2) has recently emerged as a promising material for flexible electronic and optoelectronic devices because of its finite bandgap and high degree of gate control. Here, we report a hydrogen fluoride (HF) passivation technique for improving the carrier mobility and interface quality of chemical vapor deposited monolayer MoS_2 on a SiO_2/Si substrate. After passivation, the fabricated MoS_2 back-gate transistors demonstrate a more than double improvement in average electron mobility, a reduced gate hysteresis gap of 3 V, and a low interface trapped charge density of $\sim 5.8 \times 10^{11}\,cm^{-2}$. The improvements are attributed to the satisfied interface dangling bonds, thus a reduction of interface trap states and trapped charges. Surface x-ray photoelectron spectroscopy analysis and first-principles simulation were performed to verify the HF passivation effect. The results here highlight the necessity of a MoS_2/dielectric passivation strategy and provides a viable route for enhancing the performance of MoS_2 nano-electronic devices.

Supplementary material for this article is available online

Keywords: interface passivation, MoS_2, hydrogen fluoride, MoS_2/oxide interface, mobility, XPS, first-principles calculation

(Some figures may appear in colour only in the online journal)

1. Introduction

With a sizable bandgap and a high degree of electrostatic gate control, ultrathin two-dimensional transition metal dichalcogenides (TMDs) have recently gained tremendous interest for flexible electronics and optoelectronics applications [1–3]. Molybdenum disulfide (MoS_2), one of the most studied TMD materials, has shown outstanding device performances such as high on/off current ratios up to 10^8 [1, 2], a near-ideal subthreshold swing of 60 mV/decade [2, 4], and good carrier mobilities [5]. Previous studies have shown that the substrate and superstrate dielectrics can affect the properties of MoS_2, especially its device performances [1, 3, 6, 7]. As an example, the room temperature carrier mobility of chemical vapor deposited (CVD) monolayer MoS_2 field effect transistors (FETs) fabricated on SiO_2/Si substrates has been found to be

in the range of 0.1–30 cm^2 V^{-1} s^{-1} [8–10], and this value can be remarkably improved through high-k dielectric encapsulation [1, 7]. Coulomb scattering from the MoS_2/SiO_2 interface charges has been proposed as the primary cause for the low carrier mobility in unencapsulated devices and high-k dielectric encapsulation can screen this charged impurity scattering effectively [11]. Nevertheless, this determined mobility value is still lower than the theoretically predicted phonon-limited value [12], suggesting reduced level of Coulomb scattering remains. On the other hand, gate hysteresis has been commonly observed in MoS_2 FETs, which causes instability in threshold voltage and channel conductance [13–15]. Despite the origins of gate hysteresis vary depending on the substrate environment, measurement condition, or even MoS_2 itself [13, 14], charge trapping at MoS_2/dielectric interface always plays an important role in

the hysteretic behavior in MoS_2 devices [15]. It was suggested that chemical bonding present at the 2D semiconductor/dielectric interface accounts for the interface charge trapping which causes gate hysteresis, although the 2D material itself has an atomically smooth surface and lacks dangling bonds [3]. In order to integrate MoS_2 FETs into future electronics, it is of great importance to improve the electrical quality of the MoS_2/dielectric interface to preserve their intrinsic mobility as well as eliminate gate hysteresis.

In this work, we investigate MoS_2/dielectric interface properties and demonstrate improved device characteristics via interface passivation. We choose MoS_2/SiO_2 interface as our study system since this is widely used for MoS_2 FETs. CVD MoS_2 was used to obtain large-area MoS_2 monolayer as well as to take advantage of standard photolithography over e-beam lithography such as high throughput and low cost. A hydrogen fluoride (HF)-dipping treatment is used for SiO_2 surface passivation prior to MoS_2 growth. MoS_2 back-gate FET with HF-treatment passivation show a higher mobility μ of $\sim$42.2 $cm^2\,V^{-1}\,s^{-1}$ and improved MoS_2/SiO_2 interface quality, with less hysteresis gap (ΔV_T) of $\sim$3 V and interface trapped charge density (Q_{it}) of $\sim$5.8 $\times$ $10^{11}\,cm^{-2}$, compared to $\mu \sim$ 17.9 $cm^2\,V^{-1}\,s^{-1}$, $\Delta V_T \sim$ 8 V and $Q_{it} \sim$ 1.6 $\times$ 10^{12} for device without passivation. The enhanced mobility and suppressed gate hysteresis after HF passivation are attributed to the reduced interface trapped charges due to satisfied interface dangling bonds, which was further verified by x-ray photoelectron spectroscopy (XPS) analysis and first-principles calculation.

2. Experimental section

2.1. HF-treatment passivation

Our experiments started with two silicon substrates covered by silicon oxide, one with HF-dipping treatment and the other without. HF-dipping treatment was done by immerging the sample into HF solution (KMG Electronic Chemicals, 10 ml 49% solution in 200 ml H_2O) for 15 s at room temperature, followed by DI water rinse and N_2 blow dry. The oxide thicknesses before and after HF dipping treatment are measured by ellipsometry to be 330 nm and 300 nm, respectively. Monolayer MoS_2 was then grown on both samples using the CVD method reported in our previous work [16].

2.2. Device fabrication and characterization

After growth, the CVD monolayer MoS_2 films were processed to fabricate back-gate FETs. The source and drain electrodes were defined by standard lithographic patterning, followed by electron beam evaporation of 10/90 nm Ti/Au. The heavily doped Si substrate was used as the global back-gate electrode. Schematic illustration and optical image of a typical device are shown in figures 1(a) and (b), respectively. All electrical tests were carried out using an Agilent 4156C precision semiconductor parameter analyzer in a dark ambient setting at room temperature.

2.3. Density functional theory (DFT) calculations

The MoS_2/SiO_2 interface was theoretically characterized by first-principles simulation carried out at DFT level as implemented by Vienna *ab initio* simulation package (VASP) [17]. Stishovite SiO_2 (111) surface was chosen for its simple structure. To reduce the lattice mismatch, an interface model is created by placing a (3 × 3) MoS_2 monolayer onto a (2 × 2) nine atomic layers stoichiometric SiO_2 (111) surface, with three bottom layers fixed at bulk position. A 15 Å thick vacuum layer was inserted to decouple the adjacent atomic slabs. Generalized gradient approximation with van der Waals corrections (optimized Perdew–Burke–Ernzerhof–vdW) was used to account for van der Waals interactions between MoS_2 and SiO_2 [18, 19]. The Brillouin-zone sampling was done by the 3 × 3 × 1 Γ-centered Monkhorst−Pack scheme. All the structures were relaxed using conjugate gradient method with the convergence criterion of the force exerted on each atom less than 0.01 $eV\,Å^{-1}$. The converged energy criterion is 10^{-5} eV in the calculation of electronic properties.

3. Results and discussion

There have been previous reports of applying HF passivation to SiO_2 or high-*k* oxide to form an H-terminated surface [20–25]. In this work, with HF-dipping treatment prior to the MoS_2 growth, the introduced H to the interface region would presumably satisfy the SiO_2 dangling bonds and cleave the MoS_2/SiO_2 interface bonds. Hence, such treatment is anticipated to reduce scattering from the interface charges and improve the carrier mobility. The as-grown (without HF treatment) and HF-treated monolayer MoS_2 was characterized by Raman scattering and photoluminescence, as shown in figures 1(c) and (d). The observed frequency difference between in-plane (E_{2g}^1, $\sim$381.1 cm^{-1}) and out-of-plane (A_{1g}, $\sim$401.6 cm^{-1}) phonon modes in the Raman spectrum conforms that the deposited material is monolayer MoS_2 [26]. For the HF-treated sample, the E_{2g}^1 peak shows a stronger intensity, probably due to better optical quality. The photoluminescence spectrum of as-grown MoS_2 clearly shows the well-known A (1.85 eV) and B (1.99 eV) excitonic absorption peaks [27, 28], revealing the good uniformity and high optical quality of our CVD monolayer MoS_2 [29]. For the HF-treated sample, the absorption A shows a higher intensity and slight blue-shift in peak position, which again implies superior optical quality.

The mobility enhancement by HF passivation was investigated through electrical measurements of MoS_2 back-gate FETs. Figures 2(a) and (b) show the transfer and output characteristics of CVD monolayer MoS_2 back-gate FETs on both with and without HF passivated SiO_2/Si substrates. Both devices exhibit typical n-type conduction behaviors, with an on/off current ratio exceeding 10^6 on the HF passivated substrate and 10^7 on the unpassivated substrate. Given the thick gate oxide (300 nm) in our devices, the on/off current ratio can be further improved in future studies through the reduction of effective oxide thickness. We note that the
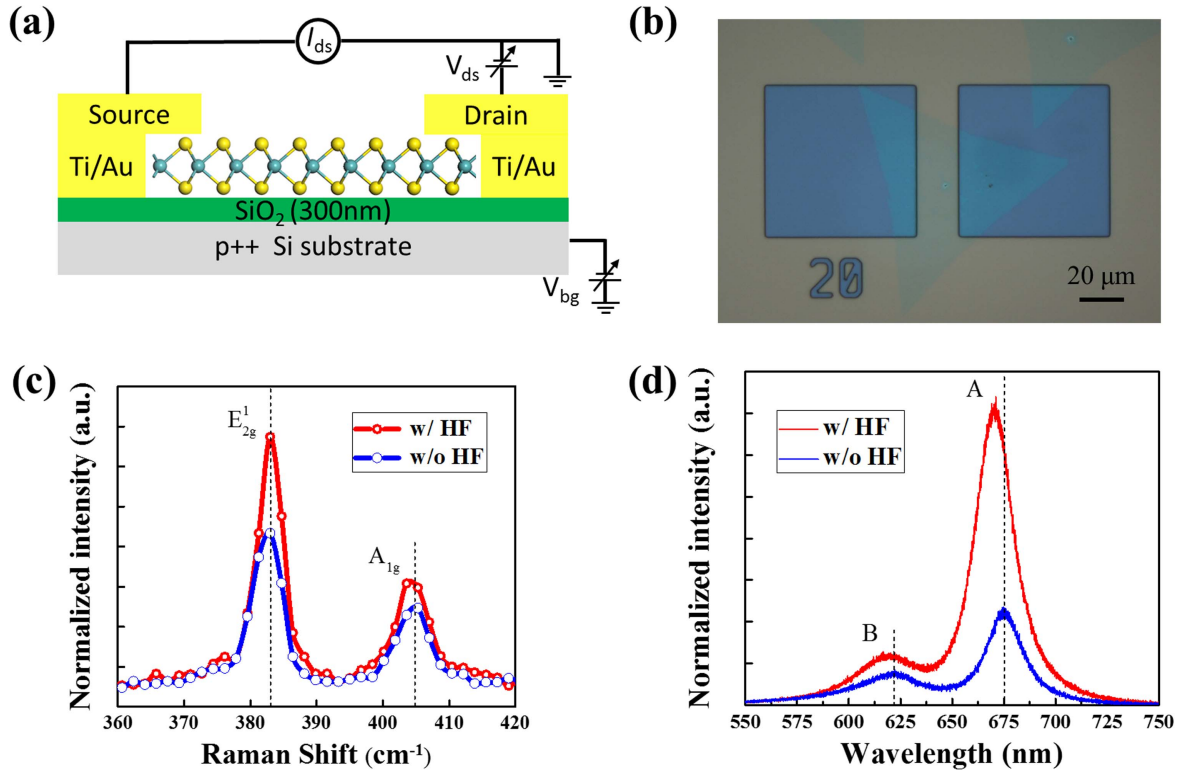
Figure 1. (a) Schematic illustration of a monolayer MoS_2 back-gate field-effect transistor. (b) Optical microscope image of a typical MoS_2 device. (c) Raman spectrum of monolayer MoS_2 film grown on the w/ and w/o HF-treated Si/SiO_2 substrate measured at room temperature. (d) Photoluminescence spectrum of monolayer MoS_2 film grown on the w/ and w/o HF-treated Si/SiO_2 substrate measured at room temperature. The laser wavelength for Raman and photoluminescence measurement is 514 nm.
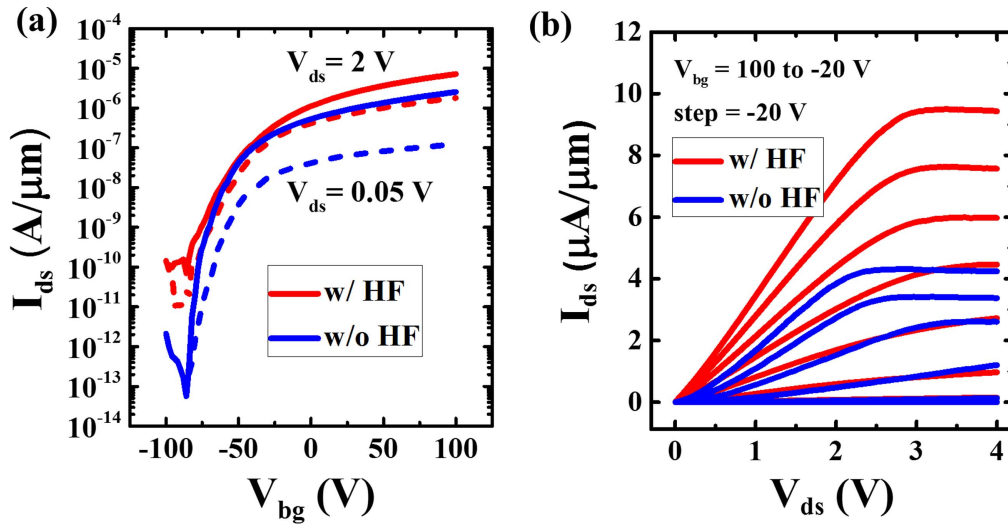

Figure 2. (a) Room-temperature transfer characteristics of CVD monolayer MoS_2 FET devices fabricated on w/ and w/o HF passivated SiO_2/Si substrate. (b) Room-temperature output characteristics of the two types of devices indicated in (a).

passivated device shows a higher off-state leakage. This could be attributed to the increased electron doping concentration after HF-passivation which we will discuss later [30, 31]. In figure 2(b), the drain current shows linear dependence at low drain-source voltage ($0 < V_{ds} < 2$ V), indicating good ohmic contact with the Ti electrode. As V_{ds} increases, the drain current starts to saturate in the high back-gate voltage (V_{bg}) range while remaining linear at lower gate voltages. This can

be explained by source/drain contact resistance modulation by gate voltage: at higher V_{bg}, the effective Ti/MoS_2 Schottky barrier height reduces [4]; the contact resistance is lowered and the drain current is limited by the intrinsic channel resistance. In this case, the $I_{ds}-V_{ds}$ curve shows a typical transistor's output feature; at lower V_{bg}, the effective Schottky barrier height is relatively higher, resulting in larger contact resistance and thus the drain current is limited by
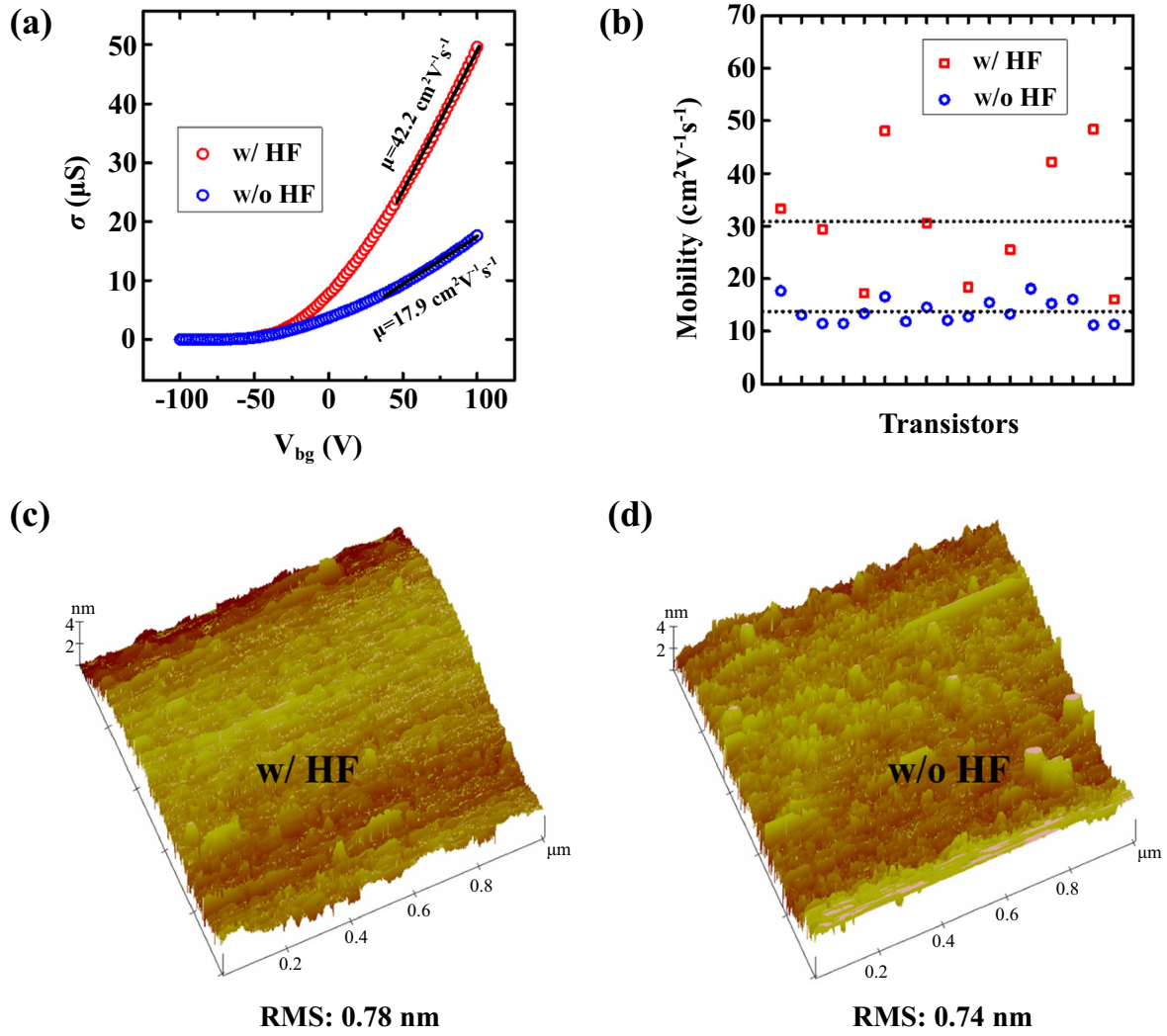
Figure 3. (a) Back-gate voltage dependence of the room-temperature conductivity for CVD monolayer MoS$_2$ FETs fabricated on SiO$_2$ with and without HF passivation. (b) Statistics of mobility extracted from σ versus V_{bg} curves in the linear region for MoS$_2$ FETs without (17 devices) and with (10 devices) HF passivation. (c), (d) AFM images of SiO$_2$ with and without HF-dipping treatment, respectively.

source/drain contact resistance. In this case, the I_{ds}–V_{ds} curve shows no sign of saturation and is more like a resistor's I–V curve. In addition, the HF passivated device shows more than doubled drive current level ($\sim 10^{-5} \, \mu$A μm^{-1}) than the unpassivated device ($\sim 4 \times 10^{-6} \, \mu$A μm^{-1}), implying mobility improvement after HF passivation.

To investigate the channel-limited electrical performance and the effect of HF passivation on the carrier mobility, we estimate the back-gate dependence of conductivity σ for our CVD monolayer MoS$_2$ devices both without and with HF passivation. The conductivity here is defined as $\sigma = (L/W) \times (I_{\mathrm{ds}}/V_{\mathrm{ds}})$, where L and W are the channel length and width of our devices, respectively. The field-effect mobility is then extracted from the σ versus V_{bg} curves in the linear region by using the expression $\mu = 1/C_{\mathrm{ox}} \times (\mathrm{d}\sigma/\mathrm{d}V_{\mathrm{bg}})$, where C_{ox} is the back-gate capacitance per unit area. The values of C_{ox} are 11.5 nF cm^{-2} and 10.5 nF cm^{-2} for passivated and unpassivated devices, respectively, by taking into account the reduced oxide thickness in HF etching. Figure 3(a) shows the back-gate

voltage dependence of the room-temperature conductivity for two representative MoS$_2$ devices. The mobility of the MoS$_2$ device with HF passivation (~ 42.2 cm^2 V^{-1} s^{-1}) has almost been doubled than that without HF passivation (~ 17.9 cm^2 V^{-1} s^{-1}). Though the value is still lower than that of mechanical exfoliation monolayer MoS$_2$ on SiO$_2$ substrate [1] or bulk MoS$_2$ [7], it is considerably larger than that of most reported CVD monolayer MoS$_2$ [8–10].

To reduce any possible device-to-device variations, we statistically measured 10 MoS$_2$ devices with HF passivation and 17 MoS$_2$ devices without HF passivation. Figure 3(b) shows the room-temperature field-effect mobility for all measured MoS$_2$ FETs devices with varied channel lengths and widths. The MoS$_2$ devices without HF passivation exhibit an average mobility value of ~ 13.9 cm^2 V^{-1} s^{-1} with slight fluctuation. In contrast, the room-temperature mobilities of all 10 MoS$_2$ devices with HF passivation range from ~ 16.4 to ~ 48.1 cm^2 V^{-1} s^{-1}, showing an average value of 30.9 cm^2 V^{-1} s^{-1}. This remarkable mobility enhancement after HF passivation suggests that the room-temperature

carrier mobility for CVD monolayer MoS_2 on SiO_2 substrate is largely limited by the MoS_2/SiO_2 interface.

To understand the $MoS_2/$substrate interface dependent carrier mobility in our MoS_2 devices, we consider various mobility-limiting scattering mechanisms as formulated by Matthiessen's rule [32]

$$\frac{1}{\mu} = \frac{1}{\mu_{ph}} + \frac{1}{\mu_{cl}} + \frac{1}{\mu_{sr}}, \qquad (1)$$

where μ_{ph}, μ_{cl}, μ_{sr} represent the motilies limited by phonon scattering, Coulomb scattering, and surface roughness scattering, respectively. Here we assume other contributions such as electron–electron scattering to be minor and thus negligible. The mobility limited by intrinsic phonon scattering and surface phonon scattering is expected to be comparable for MoS_2 FETs with and without HF passivation given that all monolayer MoS_2 films are synthesized by CVD using the same setup and that all devices are electrically characterized under same condition. Then we consider the effects of surface roughness scattering on the mobility. Figures 3(c) and (d) show AFM images of the SiO_2 surface with and without HF passivation. The obtained comparable root mean square values rule out surface roughness scattering as a cause for the difference in carrier mobility. Therefore, we can safely deduce that the mobility enhancement in MoS_2 devices on SiO_2 with HF passivation is likely due to the reduced interface Coulomb scattering.

At the surface of SiO_2 where atoms are missing, Si–O bonds abruptly terminate and dangling bonds take over, forming interface charges and traps at MoS_2/SiO_2 interface [15]. These charges present at the interface have been generally considered as the root cause for low room-temperature mobilities in MoS_2 devices [5, 11]. Radisavljevic et al have recently shown that a high-k top-gate dielectric can significantly enhance the MoS_2 channel mobility via screening Coulomb scattering from MoS_2/SiO_2 interfacial charged impurities. Nevertheless, the reported mobility for their MoS_2 FETs is still lower than the theoretically predicted phonon-limited value, suggesting Coulomb scattering still exists and that high-k dielectric alone cannot completely suppress the charged-impurity scattering from the interface charges. Indeed, significant mobility improvement was also observed in PMMA-supported MoS_2 FETs when the device surface was covered by an extra top layer of PMMA, while such effect is absent for SiO_2-supported MoS_2 devices [3]. This implies a dominance of Coulomb scattering at the MoS_2/SiO_2 interface due to chemical bonding which cannot completely be screened by dielectric capping layer.

To directly demonstrate the reduced interface Coulomb scattering is the origin of the mobility improvement for our MoS_2 devices on SiO_2 with HF passivation, we have systematically examined the nature of scattering of carriers by analyzing the electrical characteristics of our MoS_2 FETs. To correlate conductivity with Coulomb scattering, for single-layer MoS_2 which represents two-dimensional electron systems, we have [11, 33, 34]
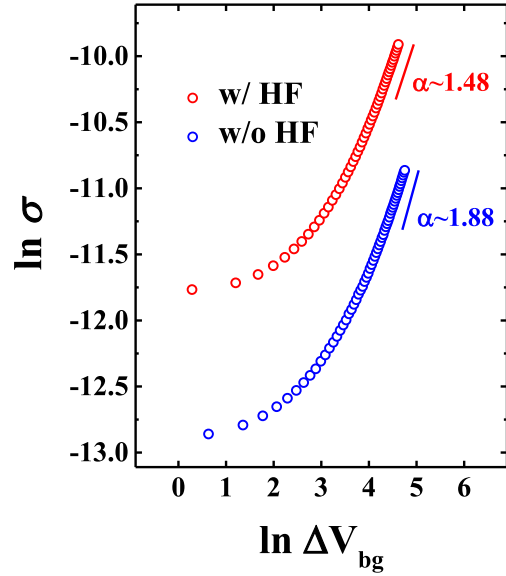
$$\sigma \propto n^{\alpha}, \qquad (2)$$

Figure 4. Variation of σ versus ΔV_{bg} for MoS_2 devices with and without HF passivation.

where n is the electron density as formulated by $n = \varepsilon_0\varepsilon_r(V_{bg} - V_t)/t_{ox}$, $1 \leqslant \alpha \leqslant 2$ is a parameter reflecting the screening of Coulomb scattering. For screened Coulomb impurity scattering, $\sigma \propto n$; for bare impurity Coulomb scattering, $\sigma \propto n^2$. In figure 4 we show the double logarithmic curve of I_{ds} ($\propto \sigma$) versus ($V_{bg} - V_t$) ($\propto n$) at room temperature for our MoS_2 FETs with and without HF passivation. In the MoS_2 device without HF passivation, we find $\alpha \sim 1.88$ approaching 2, indicating the charged-impurity scattering nearly the dominant mechanism. While for the HF passivated one, α is ~1.48, implying less charged-impurity scattering effect on electrons. More measurements (see figure S1 is available online at stacks.iop.org/SST/33/045005/mmedia in supporting information) show an average value of $\alpha \sim 1.87$ for the unpassivated devices and $\alpha \sim 1.55$ for the passivated devices. This directly links the HF passivation to reduced interface Coulomb scattering and thereby enhancements in carrier mobility. Note that α does not approach 1 suggests that Coulomb scattering originating from MoS_2/SiO_2 interface has not been eliminated and still degraded the channel mobility.

In addition to acting as Coulomb scatters, interface dangling bonds are also directly linked to interface trap states and therefore trapped charges [35]. The induced electrically active interface traps lead to degradation of device performance such as channel mobility reduction, threshold voltage instability, or leakage current [36]. We have further studied the impact of the HF treatment on the hysteresis in transfer characteristics. The hysteresis gap ΔV_T, defined as the difference of threshold voltages in forward and backward V_{bg} sweeps [37], is extracted in figure 5(a). It can be seen that the threshold voltage moves to the positive side in both two devices with backward sweeps, leading to a hysteresis gap of ~3 V for passivated device while a relatively larger hysteresis gap of ~8 V for the unpassivated device. Statistical measurements (see figure S2 in supporting information) show an
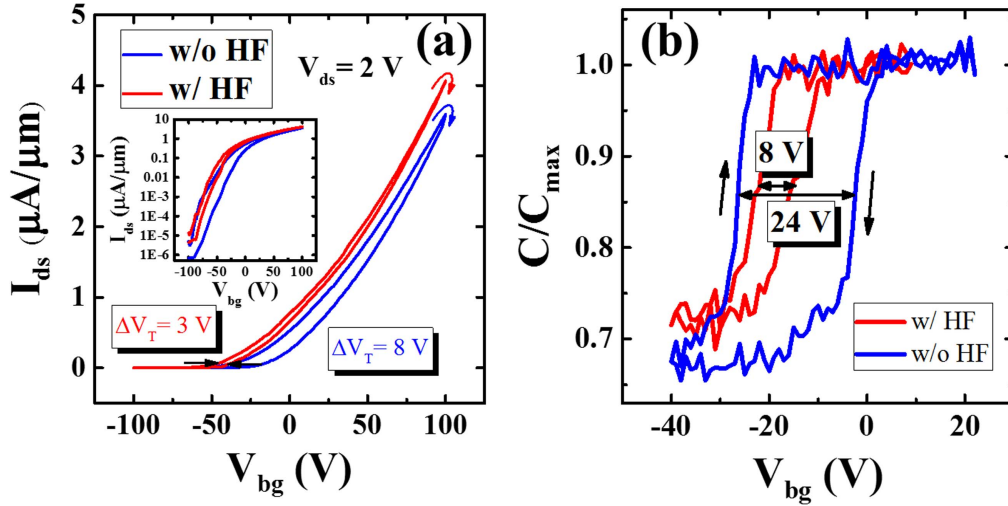
Figure 5. Hysteresis behavior of MoS$_2$ back-gate FETs with and without HF and with HF passivation. The inset shows the corresponding curve in log scale. (b) Hysteretic behavior of *C–V* curves for MoS$_2$ FET with and without HF passivation.

average ΔV_T of ~4 V for the passivated devices and ~7 V for the unpassivated ones. Generally, charge transfer between MoS$_2$ channel and surface adsorbents such as water and oxygen [14], charge trapping and detrapping at the MoS$_2$/SiO$_2$ interface [15], and charge polarization/redistribution due to the presence of sulfur vacancy [13] have been identified as three possible causes for hysteresis in MoS$_2$ FETs. However, considering the same material growth condition, devices fabrication process, and electrical characterization settings, charge trapping and detrapping at the MoS$_2$/SiO$_2$ interface is the most likely reason for the ΔV_T difference in our case. In fact, interface trapped charges has been studied for a long time to explain the hysteresis behavior in other novel low-dimensional semiconductor structures, like CNT [38, 39], ZnO nanowire [40], and graphene FETs [41, 42]. The less hysteresis gap in HF-passivated MoS$_2$ FETs here suggests reduced interface trapped charges due to the interface dangling bonds satisfaction.

We have extracted the MoS$_2$/SiO$_2$ interface trapped charge density using the *C–V* method [42]. Figure 5(b) present the room-temperature *C–V* characteristics measured on the two kinds of MoS$_2$ FETs at 200 Hz, respectively. The measurements were performed at 1 V s^{-1} sweep rate, scanning in both forward and backward directions. Both two samples show a positive flat-band voltage shift (ΔV_{FB}) when the sweep direction is reversed, resulting a hysteresis window of ~8 V for the passivated device and ~24 V for the unpassivated device. A larger ΔV_{FB} indicates more interface trapped charges. The corresponding interface trapped charge density is quantified using the following equation [43]:

$$N_{it} = \frac{C_{ox} \Delta V_{FB}}{q},\qquad(3)$$

where N_{it} is the number of charges trapped per unit area and $q = 1.6 \times 10^{-19}$ C is the elementary charge. The estimated interface charge density is about ~5.8×10^{11} cm^{-2} for HF-passivated device and 1.6×10^{12} cm^{-2} for unpassivated device. These values are lower than those of most three-
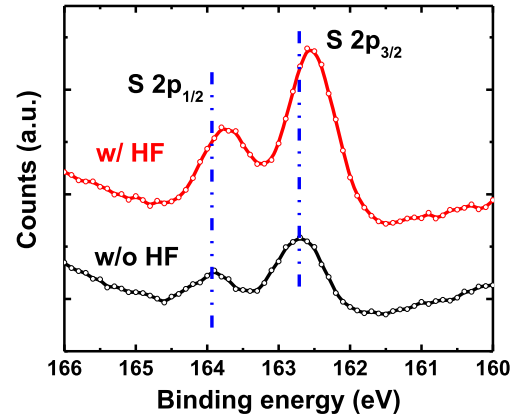
dimensional (3D) semiconductors and very close to other 2D materials like graphene [44, 45].

To verify the effect of HF treatment on the interface passivation, XPS surface analysis was performed. Figure 6 shows the high-resolution S 2p spectrum without and with HF treatment. After HF treatment, the S 2p peaks intensify while the position of their maxima shift towards lower values. Specifically, S 2p$_{3/2}$ shifts from 162.8 to 162.5 eV and S 2p$_{1/2}$ shifts from 163.9 to 163.7 eV. We should mention that we have repeated three XPS experiments independently and all of them show similar shift trend, which excludes the possibility of substrate charging causing the spectrum shift. The downshift of the peaks is directly attributed to the reduced interface charge transfer, i.e., reduced electrons transfer from sulfur to oxygen atoms after HF treatment. As discussed before, the MoS$_2$/SiO$_2$ interface dangling bonds cause S–O bonding and thus oxidation of sulfur, and H-atom passivation could weaken this bonding and lead to S less oxidized. The red shift is a direct indication of a reduced interface interaction due to HF treatment, in agreement with previous studies of SiO$_2$/MoS$_2$ interface by DFT [46].

Figure 6. XPS surface analysis of S 2p$_{1/2}$ and 2p$_{3/2}$ in MoS$_2$ w/o and w/HF treatment with binding energy peaks.
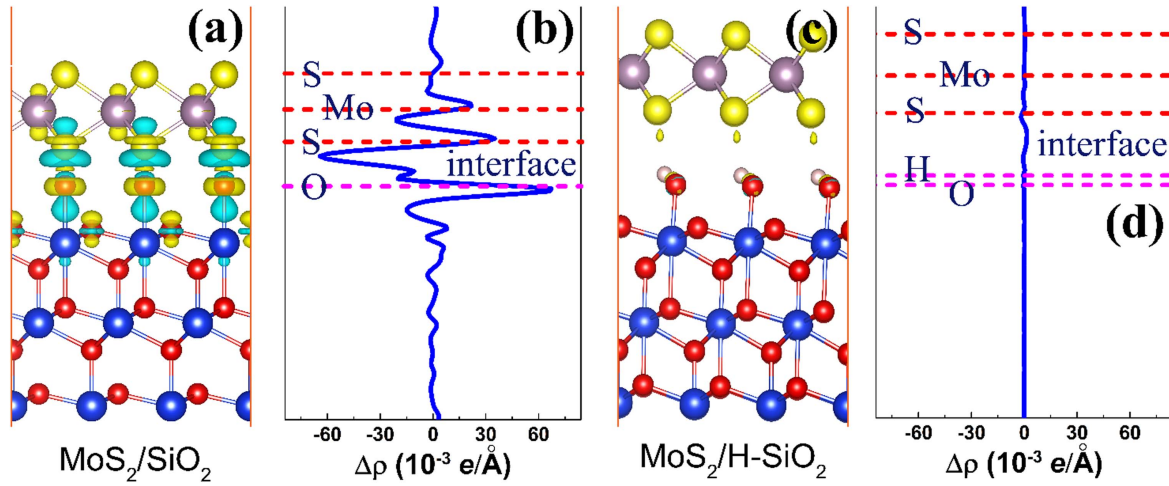
Figure 7. (a) Three-dimensional charge density difference for unpassivated MoS_2/SiO_2 interface. The yellow and green regions represent charge accumulation and depletion, respectively; the isosurface value is 0.05 e Å^{-3}. Obviously, the electron transferring occurs between MoS_2 and SiO_2. (b) The profile of the planar averaged charge density difference for MoS_2/SiO_2 interface as a function of position in the vertical direction. (c) Three-dimensional charge density difference for H-passivated MoS_2/SiO_2 interface (denoted as $MoS_2/H–SiO_2$); the isosurface value is 0.01 e Å^{-3}. (d) The profile of the planar averaged charge density difference for $MoS_2/H–SiO_2$ interface.

First-principles simulation was performed to further understand the interface interaction and passivation mechanism. The simulation was conducted by DFT as implemented by VASP [17]. Figures 7(a) and (c) depicts side view schematics of unpassivated and H-passivated MoS_2/SiO_2 interface, respectively. After geometry optimization, for the unpassivated system, the equilibrium distance between the monolayer MoS_2 and the top of the SiO_2 (111) surface is 1.60 Å. This small distance suggests strong electron orbital coupling between sulfur and oxygen atoms. Interestingly, the interface gap was found to increase to 2.60 Å after H passivation, implying a weaker interaction. To further shed light on the interface bonding, electron transfer between MoS_2 and SiO_2 was analyzed through 3D charge density difference $\Delta\rho = \rho(MoS_2/SiO_2) - \rho(SiO_2) - \rho(MoS_2)$, where $\rho(MoS_2/SiO_2)$, $\rho(SiO_2)$, $\rho(MoS_2)$ are the charge densities of the MoS_2/SiO_2 system, isolated SiO_2 (111) surface, and free standing monolayer MoS_2 in the same configuration, respectively. For the unpassivated system, obvious interfacial electron transfer at the interface can be observed while it becomes inconspicuous for the H-passivated system. Figures 7(b) and (d) plots the planar averaged charge density difference along the direction perpendicular to the SiO_2 (111) surface, which offers quantitative results of charge redistribution. The positive values represent electron accumulation, and negative values indicate electron depletion. It is clear that at the unpassivated interface electrons are accumulated around the O atoms and depleted around the S atoms, showing the electrons transfer from sulfur to oxygen while at the H-passivated interface, the amount of electron transfer becomes negligible. Further charge analysis based on the Bader method [47] reveals that on average, 0.079 electrons transfer from each S atom to O for the unpassivated interface and 0.005 electrons for the passivated interface.

Our passivation method could be potentially extended to other low-dimensional semiconductor/oxide system such as other TMDs [48, 49], CNT [38, 39], and graphene [41, 42]. Until now, for most of research studies, these low-dimensional semiconductors are either SiO_2-supported or high-*k*-covered. The electrical performances of corresponding transistors are more or less degraded by the low-dimensional semiconductor/dielectric interface due to the dielectric surface dangling bonds. As a matter of fact, many researchers have reported that CNT and graphene based transistors suffer from mobility degradation and gate hysteresis because of the semiconductor/dielectric interface trapped charges [38, 41, 50]. Our results show that a H-terminated oxide surface could be beneficial for achieving high-performance low-dimensional nano-electronic devices.

4. Conclusion

In conclusion, we have demonstrated that carrier mobility and MoS_2/SiO_2 interface electrical quality can be improved via interface passivation by HF-dipping treatment of the SiO_2/Si substrate. Specifically, the mobility of MoS_2 FETs after HF passivation was found to increase from ~17.9 to ~42.2 cm^2 V^{-1} s^{-1}, with the hysteresis gap reduced from 8 to 3 V and the interface trapped charge density decreased from 1.6×10^{12} to 5.8×10^{11} cm^{-2} eV^{-1}. The enhanced mobility and suppressed gate hysteresis are attributed to the reduced interface trapped charges due to the satisfied interface dangling bonds. The HF passivation effect is also verified by surface XPS analysis and first-principles simulation, which shows less interface bonding after HF treatment. Our work shows that a proper $MoS_2/$dielectric interface passivation is critical for further improving the performance of MoS_2 devices.

Acknowledgments

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