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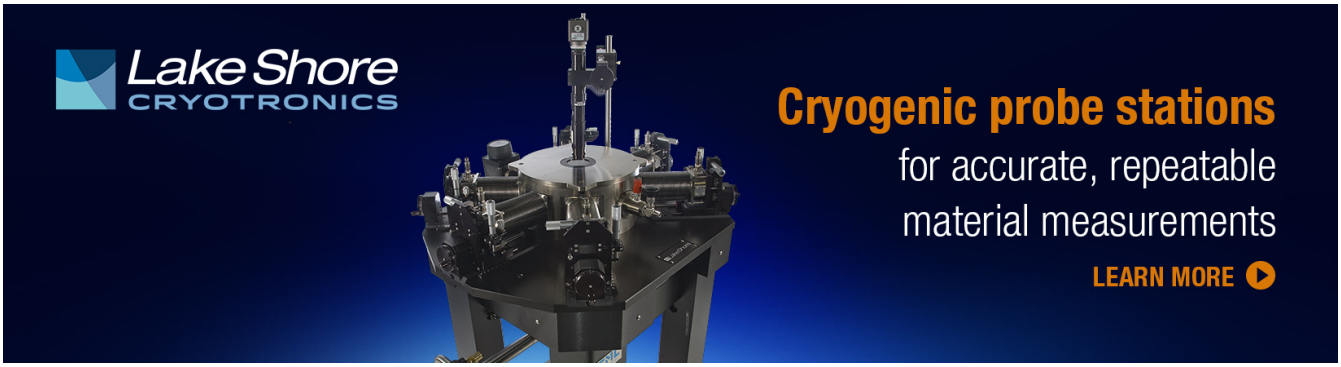

Enhanced gate stack stability in GaN transistors with gate dielectric of bilayer SiN_x by low pressure chemical vapor deposition

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We report enhanced gate stack stability in GaN metal insulator semiconductor high electron mobility transistors (MISHEMTs) by using a bilayer SiN_x as the gate dielectric. To obtain the bilayer gate dielectric scheme, a thin Si-rich SiN_x interlayer was deposited before a high-resistivity SiN_x layer by low pressure chemical vapor deposition. The Si-rich SiN_x can effectively suppress the trapping phenomenon at the interface of the dielectric/AlGaN barrier. The upper high-resistivity SiN_x layer can greatly block the gate leakage current to enable a large gate swing. Compared with the MISHEMTs using a single Si-rich or high-resistivity SiN_x layer, the MISHEMTs with a bilayer gate dielectric take the advantages of both, realizing a gate stack with a stable threshold voltage and low leakage current. These results thus present great potential for developing high-performance GaN MISHEMTs using the bilayer SiN_x gate dielectric scheme for highly efficient power applications. *Published by AIP Publishing.* https://doi.org/10.1063/1.5042809

GaN metal-insulator-semiconductor high electron mobility transistors (MISHEMTs) are emerging as one of the most promising candidates for next-generation high-efficiency power applications. By inserting a dielectric between the gate metal and semiconductor, the gate leakage current can be significantly suppressed and the gate voltage swing can be easily enlarged.[1] In particular, the electrical performance of MISHEMTs strongly depends on the chosen gate dielectric.[2] Among a variety of insulating dielectrics, SiN_x formed by low pressure chemical vapor deposition (LPCVD), has been extensively studied, exhibiting various advantages such as a high breakdown field and a low leakage current.[3–5] However, the properties of LPCVD SiN_x are greatly determined by the ratio of Si to N, which is further determined by the deposition conditions such as temperature and gas flow ratio. Previously, we have found that combining a Si-rich SiN_x (high Si to N ratio) and a high-resistivity SiN_x (low Si to N ratio) can effectively suppress the current collapse effect in GaN HEMTs,[6] exhibiting outstanding output power efficiency. Recently, Waller *et al.* have also found that the SiN_x stoichiometry can influence the effectiveness of the field plate in AlGaN/GaN HEMTs.[7] On the other hand, Zhang *et al.* observed a large threshold voltage (V_{th}) hysteresis under a large forward gate bias and Hua *et al.* observed significant current collapse under a high voltage off-state drain bias in GaN MISHEMTs using the LPCVD SiN_x gate dielectric.[8,9] The large V_{th} hysteresis and current collapse are mainly due to the trapping effect in LPCVD SiN_x or at the SiN_x/barrier interface. To date, very few studies have focused on the correlation between the SiN_x stoichiometry and the gate stack stability in GaN MISHEMTs using LPCVD SiN_x as the gate dielectric.

In this work, we comprehensively report the influence of SiN_x stoichiometry on the electrical properties of GaN MISHEMTs with SiN_x as the gate dielectric. MISHEMTs with a single layer of Si-rich SiN_x, a single layer of high-resistivity SiN_x, and a bilayer combining the former two types of SiN_x as the gate dielectric were fabricated and compared in detail. Direct and pulsed current-voltage characterization in conjunction with the capacitance-voltage measurement was performed to evaluate the bulk and interface properties of the SiN_x gate dielectric on the AlGaN barrier. The long-duration gate stress measurement was also used to evaluate the V_{th} stability.

A conventional $Al_{0.25}Ga_{0.75}N$/GaN heterostructure, with a barrier thickness of 25 nm and no cap layer, was grown on a semi-insulating 4H-SiC substrate by MOCVD. The device fabrication started with LPCVD SiN_x gate dielectric deposition at 820 °C using dichlorosilane (DSC) and ammonia (NH_3) as precursors. The LPCVD SiN_x deposition conditions were adjusted by varying the DSC to NH_3 gas flow ratio to obtain different Si/N ratios in the SiN_x dielectric. More details can be found in Ref. 6. Three samples were prepared in this study, named sample A, sample B, and sample C. For sample A, a layer of 15-nm Si-rich SiN_x (gas flow ratio of DSC:NH_3 = 220:30) was deposited as the gate dielectric. For sample B, a layer of 15-nm high-resistivity SiN_x (DSC:NH_3 = 180:50) was deposited. While for sample C, a bilayer SiN_x consisting of a first layer of 2-nm Si-rich SiN_x (the same deposition condition as sample A) and then a 15-nm high-resistivity SiN_x layer (the same deposition condition as sample B) was used as the gate dielectric. After removing the LPCVD SiN_x in the contact region, the source/drain

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ohmic metal was deposited using a Ti/Al/Ni/Au based metal stack and annealed at 850 °C in an N_2 ambient for 30 s. Then the Ni/Au based metal stack was deposited as the gate contact. In order to avoid any possible surface leakage current introduced by the dry-etching process during mesa isolation, the inter-device isolation was not performed. Instead, the devices were designed with a gate metal surrounding the source metal. After the device fabrication, no additional surface passivation was performed. Therefore, the LPCVD SiN_x served as both the gate dielectric in the gate stack region and the surface passivation dielectric in the access region. The devices described in the study feature a gate length of 3 μm, a gate-source distance of 3 μm, and a gate-drain distance of 10 μm. The length of each side of source/drain pads is 100 μm.

Double-sweep transfer characteristics of the three samples are compared in Fig. 1. Sample A shows the highest off-state leakage of $\sim 1 \times 10^{-7}$ A, which mainly comes from the gate leakage. In contrast, sample B shows a very low off-state leakage current of $\sim 2 \times 10^{-11}$ A, which is almost four orders of magnitude lower compared to sample A, resulting in a high on/off current ratio of $\sim 10^{10}$. Sample C shows a moderate leakage current of 2×10^{-9} A, suggesting that the insertion of a layer of 2-nm Si-rich SiN_x can increase the off-state leakage by around two orders of magnitude. On the other hand, the double sweep measurement, with V_{GS} swept from −15 V to 0 V and then back to −15 V, shows significant difference in the hysteresis. Sample A with an Si-rich SiN_x gate dielectric shows a negligible threshold voltage hysteresis (ΔV_{th}) of ∼0.05 V, which is negligible compared with $\Delta V_{th} = 1.3$ V in sample B. This indicates that Si-rich SiN_x can alleviate the surface trapping effect under a negative gate bias. Moreover, sample C with a bilayer structure also shows a minimal $\Delta V_{th} = 0.2$ V. Though the Si-rich SiN_x sandwiched between the AlGaN barrier and high-resistivity SiN is only 2-nm thick, the ΔV_{th} in sample C is much smaller compared to sample B, suggesting that the electron trapping effect during the double sweep measurement mainly occurs at the dielectric/barrier interface. On the other hand, we observed a $V_{th} \sim -12$ V in sample C, which is a large negative shift (∼−5 V) as compared with either sample A or sample B ($V_{th} \sim -7$ V). The slightly thicker gate dielectric, which will result in a minor reduced gate capacitance in sample C, is not a justifiable explanation for such a remarkable V_{th} shift. Owing to the same deposition condition, sample A and sample C are supposed to have the same interface properties between the AlGaN barrier and Si-rich SiN_x. While the upper layer of the gate dielectric in sample C is high-resistivity SiN_x, which should be similar to that in sample B. Therefore, high density positive charges are speculated to exist at the interface between the Si-rich SiN_x and high-resistivity SiN_x in sample C. The high density positive charges may occur due to the discontinuity deposition of SiN_x layers resulting in a high density of dangling bonds at the interface between the two SiN_x layers.

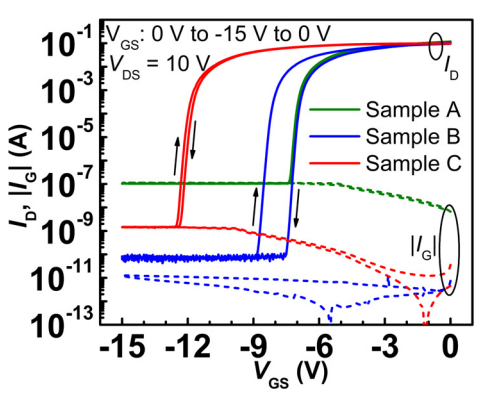

FIG. 1. Double-sweep transfer characteristics of MISHEMTs of sample A (Si-rich), B (high-resistivity), and C (bilayer).

Figure 2 compares the DC and gate pulsed output characteristics of the three samples. For the gate pulse measurement, the pulse width, the pulse period, and the quiescent gate bias (V_{GS0}) are 500 μs, 500 ms, and −15 V, respectively. Sample A with Si-rich SiN_x shows the highest maximum on-state current $I_{DS,max}$ (∼140 mA) at $V_{GS} = 2$ V and $V_{DS} = 15$ V, while the $I_{DS,max}$ values in samples B and C are ∼120 mA. Under the linear I_d-V_{gs} measurement at $V_{ds} = 10$ V, the peak transconductances (G_m) are 25 mS, 21 mS, and 19 mS for samples A, B, and C, respectively. The relatively low G_m in sample C is mainly caused by the relatively high ohmic contact resistance due to contact process variation. The variation in contact resistance does not affect the analysis of gate-stack stability. In contrast to a very severe gate lag effect in sample B, sample A with Si-rich SiN_x shows negligible trapping in the gate stack. The trapping effects in sample C with a thin Si-rich SiN_x interlayer are also slight. The results also suggest that the gate lag effect is mainly due to the surface trapping effect at the dielectric/barrier interface, and the traps inside the gate dielectric bulk have a limited impact. Furthermore, the dynamic on-resistance (R_{ON}) of each sample was also evaluated by a resistive-load hard switching test [Fig. 2(d)], where a 100 kHz pulse signal with a duty cycle of 50% is applied at the gate terminal with the off-state drain bias ranging from 10 V to 200 V. The results indicate that Si-rich SiN_x can maintain a considerably stable ratio of dynamic- to static-R_{ON} under an off-state drain bias up to 200 V. Both gate pulsed I_D-V_D and dynamic R_{ON} characterization prove that the Si-rich SiN_x can effectively

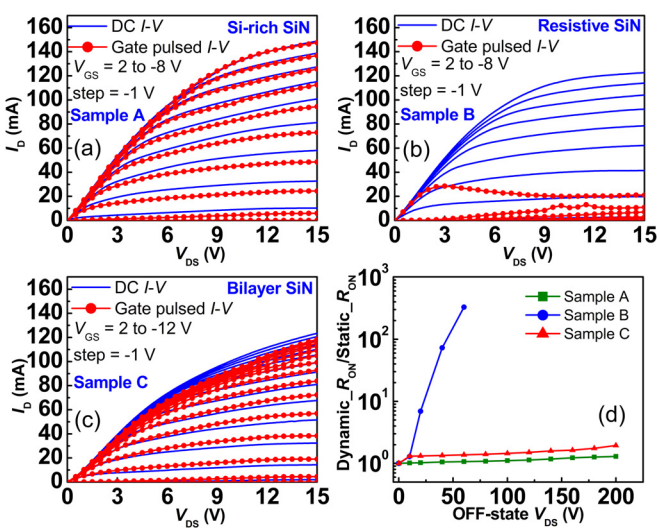

FIG. 2. (a)–(c) Comparison of dc and gate pulsed output characteristics of MISHEMTs of sample A, B, and C. (d) Dynamic- to static-R_{ON} ratio under different off-state drain voltages.

suppress the trapping effect on the AlGaN barrier. On the other hand, load-pull was measured for HEMTs passivated with Si-rich, high-resistivity, and bilayer SiN_x. More details on the load-pull measurement can be found in Ref. 10. The devices were biased at a quiescent current equivalent to ~30% of the maximum I_d and $V_{ds} = 20$ V. It had also been observed that devices passivated with Si-rich and bilayer SiN_x can deliver 30% higher output power than the device with high-resistivity SiN_x, indicating that Si-rich SiN_x can remove interface traps in the drift region. Therefore, judging from the above analysis based on different characterizations, Si-rich SiN_x is preferred for both gate dielectric and passivation.

To further evaluate the interface quality of the gate stack with different gate dielectric schemes, both the leakage current of the gate diode and the double-sweep capacitance-voltage (*C–V*) measurement were performed for the MIS diodes. Figure 3(a) shows the room temperature time-dependent dielectric breakdown (TDDB) performance of seven MISHEMTs on each of the three samples. Devices on sample A were stressed at a constant gate bias of 8 V, while devices on both sample B and C were stressed at a gate bias of 11 V, with the source and drain grounded. The bias points are chosen at ~80% of the maximal gate voltage. The gate leakage I_G was recorded with time and the time to breakdown (t_{BD}) was defined at the critical point when the gate leakage increased suddenly. Sample A showed the smallest average t_{BD} among the three samples, even though with the lowest gate stress (electric field). Compared to sample B with the same constant gate stress (similar electric field), sample C showed no obvious degradation in the forward breakdown after introducing a Si-rich interlayer. The slopes of the Weibull plot by linear fitting for Samples A, B, and C are 15.1, 4.5, and 1.8, respectively. The Sample C shows the smallest slope, which might be due to the non-uniformity of the thickness of the thin Si-rich SiN_x. Figure 3(b) shows the *C–V* curves of MIS diodes on the three samples at 1 kHz with a sweeping rate of 120 mV/s. All the MIS capacitors show a typical two-step C-V curve. The gate voltage at the first rising step corresponds to the pinch-off voltage of 2DEG, and the second rising step at a large positive gate bias indicates the barrier accumulation. Both samples A and C show a minimal hysteresis at both the pinch-off and barrier accumulation region, suggesting a low interface trap density at the dielectric/barrier interface. However, sample B with

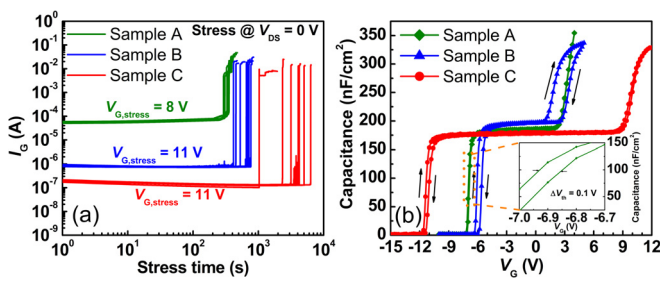

FIG. 3. (a) TDDB gate current monitored on seven MISHEMTs for each of the three samples at room temperature and (b) comparison of double-sweep *C-V* curves at 1 kHz of MIS diodes of samples A, B, and C. The inset shows the enlarged view of hysteresis in the *C-V* curve near the pinch-off region of sample A.

the high-resistivity SiN_x gate dielectric shows a large hysteresis of 1.6 V at the barrier accumulation region and 0.6 V at the pinch-off region. The existence of a large hysteresis confirms the high density of interface trap states with a long time constant at the dielectric/barrier interface. Since the barrier accumulation results in direct interaction of electrons at the AlGaN barrier surface and traps at the SiN_x/AlGaN interface, the hysteresis occurred at the barrier accumulation region can give an accurate estimation on the interface trap density (D_{it}). The D_{it} can be calculated from the measured hysteresis of on-set voltage ($\Delta V_{G,acc}$) using the following equation:[11]

$$D_{it} = \frac{C_D}{q}\Delta V_{G,acc}, \tag{1}$$

where C_D is the dielectric capacitance and q is the unit charge. The C_D can be calculated from the measured 2DEG accumulation capacitance C_{acc} given by[12]

$$\frac{1}{C_{acc}} = \frac{1}{C_{AlGaN}} + \frac{1}{C_{SiN}} = \frac{1}{C_{AlGaN}} + \frac{1}{C_D}, \tag{2}$$

where C_{AlGaN} is the capacitance induced by the AlGaN barrier. Provided that the AlGaN thickness is 25 nm and the dielectric constant of $Al_{0.25}Ga_{0.75}N$ is 9 ε_0 which is an average value for different dielectric constants found in literature studies,[12,13] the capacitance induced by SiN_x is estimated to be 443.5 nF/cm^2, 513.4 nF/cm^2, and 414.3 nF/cm^2 for Si-rich SiN_x, high-resistivity SiN_x, and bilayer SiN_x, respectively. Finally, the interface trap densities in the three samples are estimated to be 1.4×10^{11} cm^{-2}, 5.1×10^{12} cm^{-2}, and 5.2×10^{11} cm^{-2}, respectively. The calculated results suggest that the interface trap density at the Si-rich SiN_x/AlGaN interface is around one order of magnitude lower than that at the high-resistivity SiN_x/AlGaN interface. It should be noted that the extracted trap density values could still be underestimated due to the limited sweeping rate of the C-V measurement and the impact of traps with shorter emission time constants on the hysteresis may not be revealed by the C-V characterization here. Nevertheless, the underestimation does not affect the comparison of the three samples.

Both the threshold voltage V_{th} (~−6 to −7 V) to pinch off 2DEG and the on-set voltage $V_{G,acc}$ (~1–2 V) for barrier accumulation are similar for samples A and B. However, the MIS capacitor in sample C shows not only a much more negative V_{th} (~−12 V) but also a much more positive V_{on} (~+9 V). For a MISHEMT, V_{th} can be expressed as[14]

$$\begin{aligned} V_{th} = \frac{1}{q}(\phi_b - \Delta E_C^{AlGaN/GaN} - \Delta E_C^{SiN/AlGaN} - \phi_s) \\ + (\sigma_{GaN} - \sigma_{AlGaN})\left(\frac{t_{AlGaN}}{\varepsilon_{AlGaN}}\right) \\ + (\sigma_{GaN} - \sigma_{SiN,fix} - \sigma_{SiN,it})\left(\frac{t_{SiN}}{\varepsilon_{SiN}}\right), \end{aligned} \tag{3}$$

where q is the elementary charge, ϕ_b is the Ni/SiN surface barrier height (~+1.85 eV), $\Delta E_C^{AlGaN/GaN}$ is the AlGaN/GaN conduction band offset (~0.34 eV), $\Delta E_C^{SiN/AlGaN}$ (~+0.65 eV) is

the conduction band offset between SiN_x and $Al_{0.25}Ga_{0.75}N$, and ϕ_s is the distance between the Fermi level and GaN conduction band energy in the neutral region, which is ~0.3 eV.[14–16] Here, $\sigma_{AlGaN} = 4.2 \times 10^{-6}$ C/cm^2 and $\sigma_{GaN} = 2.9 \times 10^{-6}$ C/cm^2 are the absolute values of the polarization charges for the $Al_{0.25}Ga_{0.75}N$ barrier and the GaN channel,[14] respectively. $\sigma_{SiN,fix}$ is the fixed charge density at the SiN_x/AlGaN interface or inside the SiN_x bulk, $\sigma_{SiN,it}$ is the interface charge density at the SiN_x/AlGaN interface, and t_{AlGaN} and t_{SiN} are the thicknesses of the AlGaN barrier and SiN_x dielectric, respectively. ε_{AlGaN} (=9 ε_0) and ε_{SiN} (=7 ε_0) are the dielectric constants for the AlGaN and SiN_x, respectively.[14] As stated in the aforementioned analysis, the large deviation of V_{th} of sample C from samples A and B probably results from a high density of fixed positive charges at the interface between the two SiN_x layers in sample C, which is deduced to be ~1.1×10^{13} cm^{-2} from (3). The large positive turn-on voltage is suspected from the Fermi-level pinning due to the high density of fixed charges at the interface of two SiN_x layers. When V_{GS} is negative or close to zero, most of the fixed traps locate above the Fermi level of AlGaN (or GaN), so when the gate bias changes within a certain range, the surface potential of the AlGaN barrier hardly changes due to the high density of traps at the interface. When the gate bias reaches a critical point where the energy level of the interface charges is below the Fermi level of the SiN_x, the electrons will occupy these energy states and the traps become neutral. As a result, the surface potential will be modulated by the gate bias and barrier accumulation is realized.

To evaluate the gate stack stability, a positive gate bias stress measurement was performed.[17] A moderate forward gate stress of +4 V ($V_{stress} - V_{th} > 10$ V) was applied to the gate terminal at room temperature, with both the source and drain grounded. In this way, the V_{th} shift will be mainly due to the trapping process occurring at the dielectric/barrier interface or inside the dielectric. The total stress time was fixed to be 3000 s. The V_{th} shift was monitored by a fast I_D–V_{GS} measurement ($-15\,V \le V_{GS} \le 2\,V$ and $V_{DS} = 1$ V) after certain stress time intervals T_S (1, 3, 10, 30, 100, 300, 1000, and 3000 s). The time to perform the fast I_D-V_{GS} measurement is ~8 s. As shown in Fig. 4, a positive shift of V_{th} has been observed with the increase in stress time. When the total stress time reached 3000 s, samples A and C showed small V_{th} shifts of 0.3 V and 0.2 V, respectively, while a significant V_{th} shift of 1.3 V was observed for sample B. It suggests that Si-rich SiN_x on the AlGaN barrier can provide a gate stack with either a minimal trapping effect or a fast-recovery interface that the traps at the interface are with very small time constants.[6] In addition to the interface trapping effect, the large V_{th} shift in sample B may also result from bulk trapping (border traps) inside the gate dielectric.[18] Nevertheless, the large difference in the V_{th} shift between samples B and C reveals that it may be more important to control the trapping effect at the dielectric/barrier interface to achieve a stable gate stack. Compared with sample A, sample C shows a slightly smaller V_{th} shift even with a high-resistivity SiN_x as the major portion of the gate dielectric. This could be due to the Fermi level pinning effect which results from the high density charges at the interface between the two SiN_x layers in sample C. At V_{GS}= +4 V, the barrier accumulation in sample C is yet to be formed, as confirmed

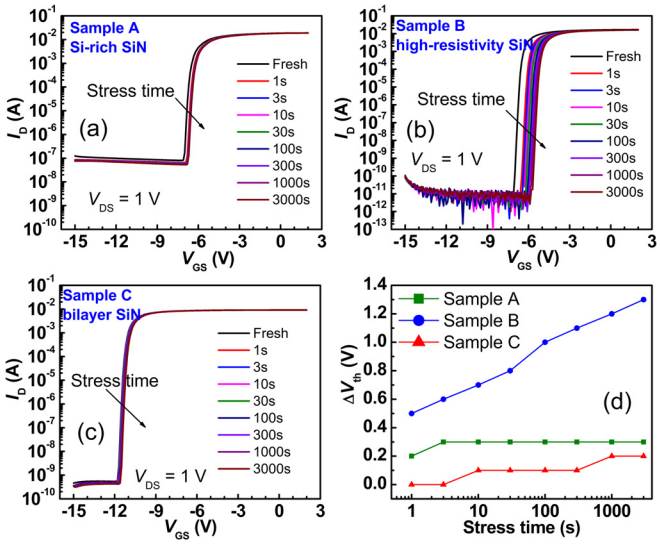

FIG. 4. Monitored transfer characteristics of MISHEMTs of (a) sample A, (b) sample B, and (c) sample C during the forward gate bias stress of +4 V. (d) Measured V_{th} shift during the gate stress.

by the *C–V* curves in Fig. 3. The high density interface charges can prevent the barrier accumulation thus suppressing interface trapping even at a relatively large positive gate bias. At a gate stress voltage of +8 V for 3000 s, the V_{th} shift in sample C is still as small as 0.5 V (not shown here), suggesting stable gate stack operation using the bilayer gate dielectric. Compared with sample A which used a single layer Si-rich SiN_x as the gate dielectric, sample C shows not only two orders of magnitude lower gate leakage current but also much more reliable gate stack operation. Therefore, the bilayer SiN_x scheme also can be a very promising option as the gate dielectric in enhancement-mode GaN MISHEMTs, which requires a large positive gate bias and stable V_{th}.

In conclusion, we have studied the impact of SiN_x stoichiometry on the electrical performance of GaN MISHEMTs. An Si-rich SiN_x is in favor of mitigating the trapping effect on the AlGaN barrier but can lead to high off-state leakage current. A high-resistivity SiN_x is beneficial for suppressing the gate leakage current but can result in a severe trapping effect when it was directly deposited on the barrier surface. A bilayer gate dielectric scheme consisting of a Si-rich SiN_x interlayer and a high-resistivity SiN_x leakage-current-blocking layer not only can suppress the trapping effect but also maintain a low leakage current and large gate swing. The results show great potential for using the developed bilayer LPCVD SiN_x scheme as the gate dielectric in both depletion- and enhancement-mode GaN MISHEMTs for highly efficient power applications.

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