GaAs Solar Cells on Nanopatterned Si Substrates

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***Abstract*—Integrating III–Vs onto Si is a promising route toward tandem photovoltaics and cost mitigation of III–V substrates. While many III–V/Si photovoltaic integration approaches have been studied, epitaxial growth on Si allows for fewer processing steps compared to other approaches. However, current epitaxial pathways utilize expensive techniques, such as thermal cycle annealing or thick buffer layers to control defect densities, undermining the low-cost goal of integrating III–Vs with Si. Here, we present single-junction GaAs solar cells grown directly on Si using selective area growth as an alternative low-cost technique to control material quality with a much thinner buffer. We demonstrate a 10.4%-efficient GaAs device grown on a V-grooved Si substrate, which achieved an antiphase domain-free III–V/Si interface and a threading dislocation density of 2×10^7 cm^{-2}, despite the lack of a graded buffer. We compare this growth on V-grooved Si to solar cells grown on polished Si with and without a patterned silica buffer layer, which demonstrate efficiencies of 6.5% and 6.8%, respectively; the polished Si was patterned using nanoimprint lithography, which is a low-cost patterning technique compatible with III–V selective area growth. Cracking is found to be a critical challenge that hinders solar cell performance and is exacerbated by the V-grooved Si surface topography. The results in this paper provide a promising pathway toward high-efficiency, low-cost III–V/Si tandem photovoltaics.**

***Index Terms*—III–V/Si photovoltaics (PV) and solar cells, metalorganic chemical vapor deposition (MOCVD), nanoimprint lithography (NIL), selective area growth (SAG).**

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I. Introduction

With a well-developed infrastructure, single-junction Si solar cells make up the majority of the commercial photovoltaics (PV) market [1]. As single-junction Si solar cell efficiencies (26.7%) [2] are quickly approaching their theoretical limit (29.4%) [3], multijunction approaches will be necessary to further improve PV performance. Currently, the most efficient multijunction devices are made of III–V materials grown on expensive GaAs and Ge substrates. The multijunction integration of III–Vs onto Si has resurged in recent years as a promising pathway to achieve high-efficiency solar cells at a low cost by benefiting from inexpensive, large-area Si substrates and the Si manufacturing infrastructure [4], [5].

While many III–V/Si integration approaches have been studied, bonding and mechanical stacking approaches do not benefit from the low cost and large area of Si substrates. This is because III–V top cells for these techniques are grown on III–V or Ge substrates, which are a few orders of magnitude more expensive than Si [6], [7]; such approaches require wafer reuse to be cost competitive [8]. On the other hand, epitaxial approaches (used interchangeably with monolithic hereon in) allow for III–V growth directly onto large-area Si substrates. However, current devices directly grown on Si use either thermal cycling [9] or thick graded buffers [10], [11] to control threading dislocation density (TDD) to the low $\times 10^6$ cm^{-2} range, which increases the growth time, and thus the cost, of both of these techniques, undermining the low-cost goal. $GaAs_yP_{1-y}$ and $Si_{1-x}Ge_x$ graded buffers are typically grown 3.6–10 μm thick [12], [13], with cost modeling predicting even thinner 3.0 μm buffers to constitute ~25% of total $GaAs_yP_{1-y}$/Si tandem manufacturing costs [6], [14]. If buffer thickness can be reduced to <3 μm, cost modeling has predicted that tandem GaAsP/Si devices could achieve a 61% decrease in growth costs [15]. Selective area growth (SAG) on the nanoscale offers a low-cost monolithic pathway to grow a high-quality III–V material on Si without the use of expensive, thick buffers [14]–[16]. SAG has been previously used in the cleavage of lateral epitaxial films for transfer [17] process as a means to enable lower-cost III–V thin film solar cells [18], though has not been previously utilized for III–V/Si direct growth. In this work, we use SAG to produce single-junction GaAs top cells on inactive Si substrates.

A variety of materials challenges hinder the growth of GaAs directly on Si. The difference in III–V and Si material polarity results in interfacial defects, and the large lattice mismatch between GaAs and Si causes an increased TDD compared to homoepitaxial growth. Furthermore, the large difference in thermal expansion coefficients of GaAs and Si can result in cracking for

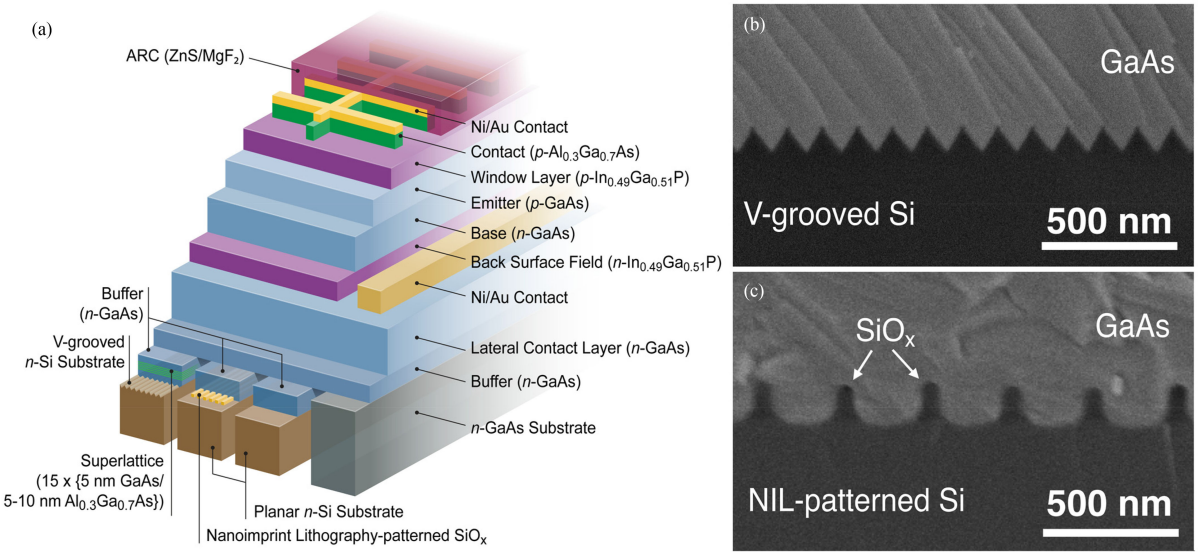

Fig. 1. (a) Device schematic of the GaAs solar cells grown on GoVS, NIL-patterned polished Si, unpatterned polished Si, and GaAs substrates and cross-sectional SEM images of the III–V/Si interface for the Gen 3 design grown on (b) the GoVS template [MP972] and (c) the NIL-patterned Si substrate [MQ059].

thick films, which can cause electrical shunting and resistance [19]. One GaAs on Si solar cell published recently achieved a very impressive 0.87 V open-circuit voltage (V_{OC}) and 18% efficiency (η) by controlling crack formation through millimeter-scale notches [20]. However, nanoscale approaches still remain mostly unexplored for III–V/Si PV applications. One report has described an uncoalesced nanoscale 0.9%-efficient GaAs device grown selectively on patterned Si [21]. Recent studies have demonstrated the use of nanoscale SAG and aspect ratio trapping to make impressive threading dislocation-free uncoalesced GaAs nanoridges on Si for laser applications [22], though PV will require coalesced, large-area devices to benefit from standard processing. The current state-of-the-art coalesced GaAs films grown on Si via SAG on V-grooved Si (GoVS) [23] have been utilized for laser devices [24] and photodetectors [25], achieving antiphase-domain-free III–V/Si interfaces [23] and TDDs of $0.4 - 2.1 \times 10^8$ cm^{-2} [26], [27].

In this work, we report on monolithic single-junction GaAs solar cells grown via SAG on Si. We develop GaAs solar cells on the state-of-the-art coalesced GoVS templates; the GoVS templates utilized in this work have been studied in depth previously [23], and the work in this manuscript focuses instead on the solar cells grown on these templates. On these V-grooved templates, our cells achieved a solar cell TDD of 2×10^7 cm^{-2}, V_{OC} of 0.77 V, and efficiency of 10.4%. We additionally present single-junction GaAs solar cells grown on polished Si substrates that were either unpatterned or patterned with nanoimprint lithography (NIL)—a scalable, low-cost nanopatterning technique compatible with III–V SAG and promising for commercialization, which may ultimately be able to replace the more expensive patterning techniques used to make the GoVS templates [15]. The solar cells described here exhibit challenges with cracking, which can be understood upon comparing results across the various Si substrates reported on here. This work demonstrates promising developments toward attaining commercially viable high-efficiency, low-cost III–V/Si PV.

II. Experimental Details

The GoVS templates were prepared as was previously described [23]. On-axis n-Si (001) substrates were first patterned with SiO_2 stripes along the [110] direction; the patterning was conducted by SEMATECH using immersion lithography, a patterning technique likely to be too expensive for most PV applications; an alternative low-cost patterning technique, NIL, is also explored in this work. The wafers were then cleaned via RCA [28] and dilute 1% HF wet chemical etches, followed by etching in 45% KOH at 70 °C to form (111)-facetted V-grooves. The initial GaAs nucleation was conducted in a low-pressure 0.1 atm metal–organic chemical vapor deposition (MOCVD) system with a horizontal reactor (AIXTRON 200/4) [23]. After nucleation, the SiO_2-patterned stripes were removed prior to bulk growth of the remainder of the 1.5 μm GaAs buffer, resulting in a V-grooved III–V/Si interface with 130 nm tip-to-tip width and 90 nm trench depth (see Fig. 1). This III–V/Si interface enables an APD-free film due to the growth on V-grooved (111) facets [23]. Furthermore, the "tiara-like" structures at each V-groove tip block most stacking faults and the high angle of the V-groove morphology allows most of those not blocked to self-annihilate on other stacking faults from neighboring V-grooves, as described in [23]. Included in the middle of the 1.5 μm GaAs buffer is a 15-repetition 5–10 nm/5 nm $Al_{0.3}Ga_{0.7}As$ (AlGaAs hereafter)/GaAs superlattice to help promote a smooth surface morphology [29]. These GoVS templates were shipped to the National Renewable Energy Laboratory (NREL) where they were precleaned for 5 s in 2:1:10 NH_4OH:H_2O_2:H_2O prior to cell growth in a custom-built atmospheric MOCVD system. NIL-patterned Si substrates were prepared at NREL using polydimethylsiloxane (PDMS) pattern-transfer stamps [30] and spin-coated sol–gel SiO_x resist [31]. Patterns were transferred into the resist by placing the PDMS stamp on the resist-coated (100) n-Si wafer offcut 4° toward (111) for 30–60 min. The pattern consisted of stripes oriented along the [110] direction.

TABLE I
DEVICE STRUCTURE DETAILS

Layer	Material	Doping (cm^{-3})[b]	Gen 1	Gen 2	Gen 3
Contact	AlGaAs: C		20 nm	20 nm	20 nm
Window Layer	InGaP: Zn	$<8\times10^{18}$	50 nm	50 nm	50 nm
Emitter	GaAs: Zn	$0.5\text{-}1\times10^{19}$	100 nm	100 nm	100 nm
Base	GaAs: Se	$1\text{-}3\times10^{17}$	2.5 µm	1.5 µm	2.0 µm
BSF	InGaP: Se		300 nm	150 nm	150 nm
LCL	GaAs: Se		2 µm	0.3 µm	0.5 µm
NREL-grown Buffer	GaAs: Se		200 nm	100 nm	100 nm
Total III-V Thickness[a]			6.7 µm	3.7 µm	4.4 µm

This table shows all layers above the GaAs substrate shown in Fig. 1, which were grown via MOCVD at the National Renewable Energy Laboratory.
[a]This row includes the thickness described in this table, plus the 1.5 μm III–V epitaxial thickness grown at the Hong Kong University of Science and Technology on the GoVS templates.
[b]Base doping levels were measured with capacitance–voltage measurements and emitter doping levels were measured with Hall effect measurement. The window layer doping level is reported as a maximum, as it is a convolution of both emitter and window layer doping as measured via Hall effect measurement.

Reactive ion etching was used to remove the thin layer of residual resist at the base of the vias, and a 45-s 1% HF preclean was conducted prior to MOCVD growth. The NIL-patterned SiO_x mask was laterally overgrown during III–V growth, which may introduce passivation and light trapping [32] for the underlying Si in future III–V/Si tandems. The pattern had a pitch of 300 nm, a height of 150 nm, and a wall-to-wall spacing of 230 nm. The unpatterned (100) n-Si wafer offcut 4° toward (111) used for GaAs solar cell growth was precleaned for 30 s in 10% HF immediately prior to MOCVD growth. The growths on planar Si substrates underwent a ~3 min AsH_3 anneal at 900–1000 °C similar to previous reports [33], followed by a two-step GaAs nucleation at 500 °C and 1.7 μm/h, and 650 °C and 5 μm/h. In addition to growth on Si, all structures were also grown on (001) n-GaAs substrates, which were precleaned for 60 s in 2:1:10 NH_4OH:H_2O_2:H_2O.

Devices were fabricated using photolithography, Ni/Au electroplating, and wet etching past the $In_{0.49}Ga_{0.51}P$ back surface field (BSF) for 0.12–0.25 cm^2 device mesas. A highly doped lateral conduction layer (LCL) below the solar cell layers facilitated a two top contact geometry (see Fig. 1) to deconvolve cell results from possible complications from the III–V/Si interface. All solar cells in this study employed optimized ZnS/MgF_2 antireflection coatings with approximate thicknesses of 50 nm/100 nm. Lighted current–voltage (LIV) measurements were conducted under one-sun AM1.5G illumination using a custom-built Xe lamp solar simulator. External quantum efficiency (EQE) measurements were taken with a custom-built tool under chopped, monochromatic light. The solar cell structures are described in Fig. 1 and Table I.

III. RESULTS AND DISCUSSION

A. Solar Cell Development

The first structure grown (Gen 1 in Table I) was selected upon comparing multiple homoepitaxial structures previously

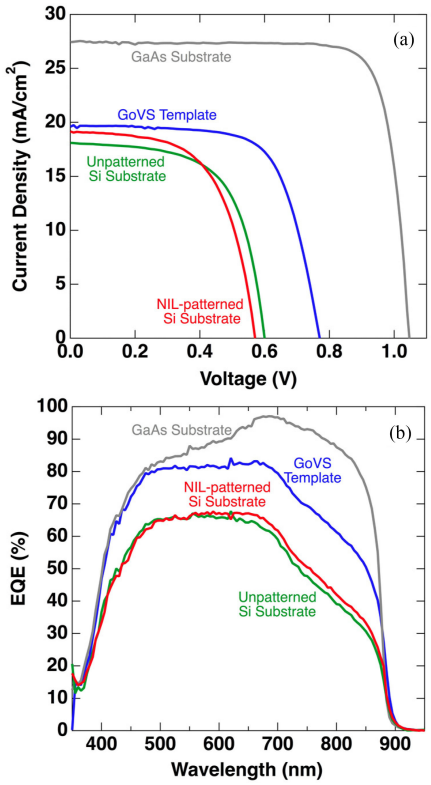

Fig. 2. (a) LIV and (b) EQE of the Gen 3 solar cell design grown on GaAs (gray, MP767B), GoVS (blue, MP767A), NIL-patterned polished Si (red, MQ059), and unpatterned polished Si substrates (green, MQ057).

reported [14]. The device design was optimized to the Gen 3 design (see Table I) by reducing total epitaxial thickness while avoiding transmission losses; the device development is described in more detail in the Supplementary Information (see Fig. S1, Table S1, and Fig. S2). A p-on-n design was chosen for enhanced defect tolerance in our upright structure [34]. An upright solar cell design was chosen for this study to best suit a monolithic multijunction design on Si and is not ideal for a homoepitaxial single-junction device. While the current record single-junction homoepitaxial GaAs solar cell achieves 28.8% efficiency [35], it does so with the use of photon management techniques [36], [37], such as a back reflector, which cannot be implemented in monolithic multijunction structures. A more appropriate comparison for our homoepitaxial control is the record upright GaAs single-junction, which achieved 26.4% efficiency [38]. Our upright Gen 3 design enabled a high 23.3% efficiency on a homoepitaxial control device (see Fig. 2 and Table II), which compares quite well to this upright record, given that our cell utilizes a nonoptimal p-on-n polarity and on-axis growth substrate, unlike the record device.

This third generation design enabled a 10.4%-efficient solar cell on the GoVS template. The TDD of the Gen 3 solar cell on a GoVS template was measured by electron beam induced current mapping (EBIC) to be 2.6×10^7 cm^{-2} (see Fig. S3); the TDD was further characterized by x-ray diffraction and the full width at half maxima of 99–154 arcsec of rocking curves taken at five different reflections were used to extract a TDD of 4.5×10^7 cm^{-2} based on Ayers' method [39]. This agrees

well with EBIC but may be a slight overestimate due to the system's double-crystal set-up. The TDD level in this device on a GoVS template contributes to a reduced minority carrier diffusion length and the lower long wavelength EQE seen in Fig. 2 compared to the control device. While this Gen 3 design enabled the highest fill factor (FF) of all the device design generations (see Table S1), series resistance and FF of all cells grown on GoVS templates are limited by the emitter and window layer sheet resistances (670–994 Ω/□ as measured by transmission line measurement); given the high $\times 10^{18}$ cm^{-3} doping levels of the emitter and window layer of these structures (see Table I), the sheet resistance of these layers may instead be hindered by the severe cracking and poor diffusion lengths in these materials. While the thick 50 nm window layer helps enhance the FF, the parasitic absorption in the window likely contributes to the limited short-wavelength EQE of this cell design. These solar cells grown on GoVS templates are ultimately limited by a combination of high series resistance (3–5 Ω·cm^2), low diffusion lengths due to the large TDD, and cracking, as seen in EBIC (see Fig. S3).

The record single-junction GaAs solar cell grown monolithically on Si [9], [40], [41] performed 2× better than the best device on GoVS reported here; however, the record cells use expensive thermal cycle annealing to achieve low defect densities of 3.7×10^6 cm^{-2}, whereas the techniques in our work offer a low-cost alternative to minimize growth thickness. Modeling of single-junction GaAs cells on Si suggests that our device TDD of 2.6×10^7 cm^{-2} should enable efficiencies of 10.1–17.8%, depending on the assumptions in the model [42], [43]. Our best 10.4%-efficient device agrees with Yamaguchi's model [42]. However, this model assumes a structure lacking cladding, unlike our cells. Jain's model [43] uses a cladded structure more similar to ours, though this model acts as an upper bound given the optimistic modeling assumptions. These models do not account for the effect of cracking on cell performance, which likely helps explain the lower efficiency of our cell compared to Jain's model.

B. Effect of Different Substrates

To investigate lower cost nanopatterning techniques, we grew the Gen 3 design on polished Si substrates, both unpatterned and patterned with silica stripes using NIL. On these two samples, a ~1.6 μm n-GaAs buffer layer was grown underneath the layers outlined in Table I to match the structure used in the GoVS templates; however, no AlGaAs/GaAs superlattice was employed, so both of these samples exhibited rougher surfaces than the growths on the GoVS templates. As anticipated, the solar cell grown on unpatterned polished Si performed poorly relative to the growth on GoVS, as no technique was used to improve the III–V crystalline quality (see Fig. 2 and Table II). The growth on NIL-patterned Si performed similarly and had an even lower V_{OC} by 30 mV (see Table II). With TDD values $>10^9$ cm^{-2}, these growths on polished Si exhibited reduced V_{OC} and EQE across all wavelengths relative to the growth on GoVS, which substantiates the idea that the V-grooved surface topography in the GoVS templates plays an important role in dislocation reduction. However, the low long-wavelength EQE of all of the cells grown on Si suggests that all suffer from significantly reduced minority carrier diffusion lengths compared to the homoepitaxial control. Note that the difference between the measured J_{SC} and the integrated EQE of the Gen 3 cells grown on polished Si and GoVS likely results from the difference in apparent metal grid shadowing between the LIV and EQE measurement techniques. Additionally, the III–V nucleation and coalescence on the NIL-patterned Si substrate likely resulted in defects at the III–V/Si interface and at the points of coalescence above the silica mask [44]. However, the slightly higher current in the NIL-patterned sample suggests that nanopatterning may contribute light trapping benefits [32], [45], [46]. At present, the GoVS nucleation technique yields a higher quality material, and future improvements to the nucleation on polished Si substrates may yield interesting comparisons.

TABLE II
GEN 3 SOLAR CELL PARAMETERS

Substrate	V_{OC} (V)	J_{SC} (mA/cm^2)	FF (%)	η (%)
GaAs	1.05	27.4	81.3	23.3
GoVS	0.77	19.6	68.7	10.4
Unpatterned Si	0.60	18.1	62.6	6.80
NIL-patterned Si	0.57	19.2	59.9	6.54

Sample numbers: MP767, MQ057, MQ059.

These two growths, in conjunction with a previously published theoretical and empirical study of critical thickness for crack formation in GaAs/Si epitaxial growth [19], offered a better understanding of the cracking phenomenon. Cracking is affected by the change in temperature upon cooling and the total III–V thickness. Our samples experienced a 625–675 °C change in temperature upon cooldown to room temperature. We adjusted the LCL thickness of each device design to vary the total III–V epilayer thickness among generations: 6.7, 3.7, and 4.4 μm, from Gen 1 to 3, respectively (see Table I). Based on these growth conditions, according to Yang's empirical results [19], the Gen 1 design should be the only one to exhibit cracking, while Yang's theoretical results suggest both Gen 1 and Gen 3 should exhibit cracking [see Fig. 3(a)]. However, all growths on GoVS substrates exhibited severe cracking, and the majority of cracks propagated in the same direction as the V-grooves [see Fig. 3(b) and (c)]. It was particularly interesting to compare the Gen 3 structure across substrates, which should not have exhibited cracking according to Yang's empirical results and should have cracked according to Yang's theoretical critical thickness calculations [19]. The Gen 3 growth on the GoVS template exhibited severe cracking, though showed no sign of cracking on the unpatterned Si substrate and only minimal cracking on the NIL-patterned Si substrate. These observations suggest that the V-grooved Si surface topography may have acted as a stress concentrator [47], [48] to exacerbate cracking compared to planar Si, the latter of which was the basis for Yang's study [19]. This hypothesis is corroborated by the observation that most cracks appeared to propagate from the tip of the V-grooves (see Fig. S4).

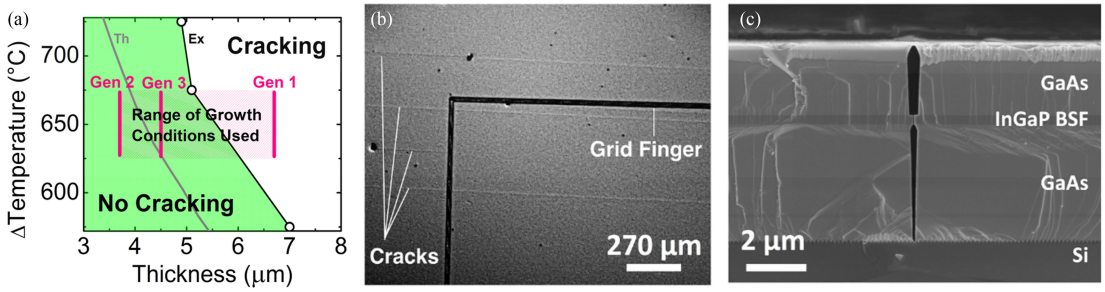

Fig. 3. (a) Graph of critical thicknesses for crack formation on GaAs/Si epitaxial growth on polished Si determined empirically (black) and theoretically (gray) and reproduced based on previously published data [18] with the permission of AIP Publishing. The Gen 1–3 growth conditions employed in the solar cell devices reported in this work are overlaid in magenta. The Gen 1–3 growths on GoVS templates in this work demonstrated severe cracking, while the Gen 3 growth on polished Si with and without a patterned silica buffer layer exhibited minor cracking and no cracking, respectively. (b) Nomarski microscope image of the Gen 2 design (MP913). (c) Cross-sectional SEM image of the Gen 1 design on a GoVS template (MP567), showing cracking after fabrication.

Device fabrication also appeared to contribute to crack exacerbation. Nomarski images [see Fig. 3(b)] showed more cracks after fabrication when compared to images taken after device growth. Furthermore, cracks appeared to have widened after fabrication, as seen in scanning electron microscopy (SEM) images [see Fig. 3(c)]. To identify the source of the crack widening, we took optical image maps of a sample grown on a GoVS template after every critical step of fabrication. During fabrication, cracks appeared to become more prominent immediately after the GaAs solar cell active layers were etched (see Figs. S5 and S6). We hypothesize that cracks are being widened as the GaAs etchant seeps into the solar cell area through the cracks at the mesa sidewalls during the GaAs mesa etch. This hypothesis is corroborated by the fact that the cracks were not widened at the $In_{0.49}Ga_{0.51}P$ (InGaP hereafter) BSF [see Fig. 3(c)], given that the mesa etch chemistry (3:4:1 H_3PO_4:H_2O_2:H_2O) selectively etches GaAs and not InGaP; furthermore, a lesser degree of widening is observed in Fig. 3(c) in the GaAs buffer below the InGaP BSF, which could be because the GaAs etchant had to seep through the thin crack at the InGaP BSF in order to reach the underlying GaAs buffer. Future improvements to device processing may help mitigate crack widening.

IV. Conclusion

Overall, the work presented in this paper establishes SAG as a low-cost platform for monolithic III–V/Si PV by demonstrating promising results on both state-of-the-art GoVS templates and low-cost NIL-patterned polished Si substrates. We developed the upright GaAs solar cell design to enable a 10.4% efficiency on a GoVS template, despite severe cracking and a TDD of 2.6×10^7 cm^{-2}. The comparison between our devices grown on V-grooved Si and planar NIL-patterned Si suggests that V-grooves likely exacerbate cracking, while conversely maintaining the patterned masking material potentially helps alleviate cracking. The results here suggest that a more thorough investigation into the benefits of using planar or V-grooved III–V/Si interface topographies is warranted, along with a rigorous study into the potential relationship between TDD and crack density, as both contribute to stress relief in these films. While the device results on the GoVS templates provide a baseline expectation for what PV performance is possible with a SAG-based approach, replacing immersion lithography with NIL as the patterning technique can better enable commercialization; to this end, a clear next step for this work is to reproduce the presented solar cells but instead on V-grooved Si, which has been patterned with NIL. Additionally, shifting toward the use of unpolished Si substrates is important to further reduce cost [49]. Our structures utilized thinner buffers (2.1–3.7 μm, including the LCL) than metamorphic $GaAs_yP_{1-y}$ (3.6–7.4 μm [10], [12]) and $Si_{1-x}Ge_x$ ($\sim$9 μm [11]) pathways for low-cost III–V/Si PV. TDD of our cells may be reduced with strained layer superlattices [9], [40], [41], [50], and the severity of cracking may be reduced with thinner structures grown at lower temperatures. In a realistic two-terminal tandem GaAs/Si device, a very thin tunnel junction would replace the thick 0.3–2 μm LCL in our current layer structure, which would reduce costs and mitigate cracking. If cracking cannot be entirely suppressed, it will be critical to investigate the impact of cracking on the reliability of GaAs/Si PV. Cost could further be reduced through the use of very high growth rates, which have been previously shown to enable comparable cell performance to more typical low growth rates like those used in this work [51]. Adjusting the cell design could further reduce the large series resistance in our cells. Overall, this work demonstrates promising developments toward achieving commercially viable low-cost, high-efficiency III–V/Si PV.

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Authors' photographs and biographies not available at the time of publication.