High-Performance AlGaN/GaN/Si Power MOSHEMTs With ZrO_2 Gate Dielectric

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***Abstract*— We report on the power performance of GaN-on-Si metal–oxide–semiconductor high electron mobility transistors (MOSHEMTs) with a high-*k* ZrO_2 gate dielectric formed by atomic layer deposition. As a result of the high-quality ZrO_2 and ZrO_2/AlGaN interface, the MOSHEMTs demonstrate an excellent ON/OFF current ratio of 5×10^{10}, a steep subthreshold slope of 66 mV/dec, a small hysteresis of ~0.05 V, and a high breakdown voltage of 1084 V at 1 μA/mm. Effective suppression of current collapse with a dynamic-to-static ON-resistance ratio of 1.78 at a drain bias of 600 V is also achieved in the device. Benefiting from the highly uniform gate stack, large-area devices with a gate width of 20 mm were also demonstrated using the ZrO_2 gate dielectric, exhibiting a maximum output current of 7.4 A, a low ON-resistance of 0.66 Ω, and a high breakdown voltage of 650 V at an OFF-state drain current of 1 μA/mm.**

***Index Terms*— III-nitride, gate dielectric, leakage, metal–oxide–semiconductor high electron mobility transistors (MOSHEMTs), power, ZrO_2.**

I. Introduction

HIGH electron mobility transistors (HEMTs) based on AlGaN/GaN heterostructures are promising candidates for high-frequency power switching applications [1]. To block the gate leakage and enhance gate swing in the HEMT devices, metal–oxide–semiconductor HEMT (MOSHEMT) structures with a gate dielectric have been extensively investigated [2], [3]. To ensure reliable and energy-efficient power-switching operation, the use of high-quality gate dielectric in III-nitride MOSHEMTs is of great importance.

In selecting the gate dielectrics, a thick insulating material with a high dielectric constant is desired to achieve a minimal gate leakage and excellent electrostatic control over the channel. Most of the conventional dielectric materials (e.g., SiO_2, SiN, and Al_2O_3) with relatively low dielectric constant $\varepsilon < 10$ are not ideal [4]. In contrast, ZrO_2, a dielectric with $\varepsilon > 20$, is very attractive to serve as a gate insulator material [5]. In the past decade, ZrO_2 formed by several methods such as e-beam evaporation [6], metal-organic chemical vapor deposition (MOCVD) [7], and plasma-assisted or thermal atomic layer deposition (ALD) [8]–[10] has been studied as the gate dielectric for GaN MOSHEMTs. Generally, the ALD approach can deliver a better film quality. However, unlike the ALD-deposited Al_2O_3 that is usually amorphous, ZrO_2 tends to be polycrystalline with increased deposition thickness and the film quality highly depends on the deposition conditions [5], [11]. Challenges such as large gate leakage and high interface trap density are still present in GaN MOSHEMTs using a ZrO_2 gate dielectric. Moreover, most of the reported devices to date were focused on low-voltage device characterization. Studies on the high voltage and dynamic performance of GaN MOSHEMTs using ZrO_2 gate dielectric are still missing. In addition, ZrO_2-gated MOSHEMTs with low leakage current, high ON/OFF current ratio, small gate lag, minimal hysteresis, high breakdown voltage, and low current collapse are yet to be demonstrated simultaneously.

In this paper, we report GaN MOSHEMTs on Si with an ALD ZrO_2 gate dielectric, exhibiting a high breakdown voltage (V_{BR}) over 1 kV at I_D of 1 μA/mm. A low dynamic-to-static ON-resistance (R_{ON}) ratio of 1.78 at an OFF-state V_{DS} of 600 V was achieved. A superior gate stack has been implemented incorporating the high-quality ZrO_2, leading to a high ON/OFF current ratio of 5×10^{10}, a steep subthreshold slope (SS) of 66 mV/dec, and a minimal hysteresis of 50 mV.

II. Heterostructure Design and Device Fabrication

The AlGaN/GaN HEMT structure was grown on a 6-in n-type Si (111) substrate by an MOCVD. The epitaxial structure, from bottom to top, consists of a composite buffer of 0.3-μm AlN, followed by a 1-μm step-graded AlGaN and a 2.5-μm carbon-doped GaN, a 0.5-μm unintentionally-doped GaN channel layer, a 1-nm AlN spacer, a 20-nm $Al_{0.25}Ga_{0.75}N$ barrier, and a 5-nm *in situ* SiN cap, as shown in Fig. 1(a). The Hall-effect measurement showed a sheet resistance of ~344 Ω/sq, a 2-D electron gas density of 1.05×10^{13} cm^{-2}, and an electron mobility of 1730 cm^2/V·s. The device fabrication started with source/drain ohmic metallization [12], [13], followed by a 100-nm plasma enhanced chemical vapor deposition (PECVD) SiN passivation. The device isolation was performed using argon ion implantation. The gate window was

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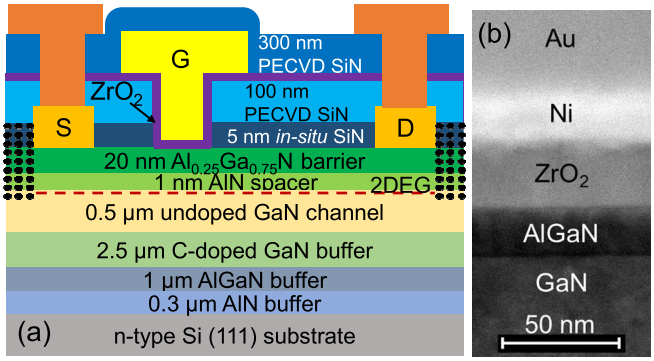

Fig. 1. (a) Cross-sectional schematic of fabricated GaN MOSHEMTs on Si with a 28-nm ZrO_2 gate dielectric. (b) Cross-sectional TEM image of the gate stack.

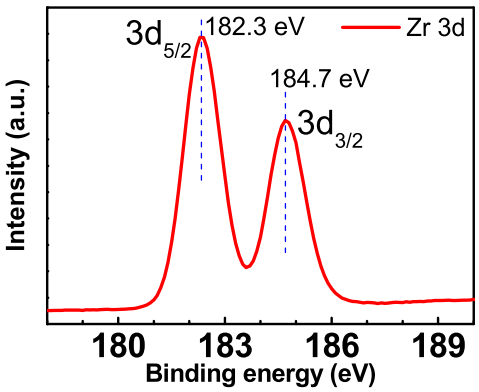

Fig. 2. XPS spectrum of Zr 3d core level of 28-nm ZrO_2 on AlGaN/GaN HEMT on Si.

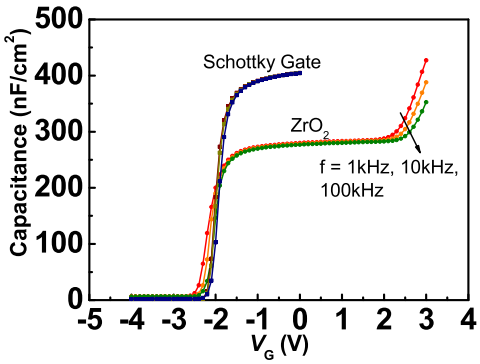

Fig. 3. Multifrequency C–V characteristics of circular-shaped MOS diodes with ZrO_2 gate dielectric and SG.

opened by removing both the PECVD and *in situ* SiN using a low-power (20 W) SF_6-based inductively coupled plasma dry etch. After the barrier surface was cleaned by a diluted HCl solution (HCl:H_2O = 1:3), a 28-nm ZrO_2 dielectric was deposited at 200 °C by ALD, using Tetrakis (ethylmethylamino) zirconium and H_2O vapor as precursors. Then, the Ni/Au-based gate metal was formed. After deionized water cleaning, the devices were passivated with another 300-nm PECVD SiN. Finally, the Al-based pad metal was deposited. For comparison, a reference sample of HEMT with a Schottky gate (SG) was also fabricated using the same epi structure and process except for the gate formation. Unless otherwise specified, the devices in this paper feature a T-shaped gate structure with a gate foot length (L_G) of 2 μm and a gate overhang of 2 μm on both the source and drain sides, a gate–drain distance (L_{GD}) of 14 μm, a gate–source distance (L_{GS}) of 4 μm, and a gate width of 200 μm. The gate overhang on the drain side naturally serves as a gate-connected field plate, reducing the peak field at the gate foot edge. Fig. 1(b) shows the cross-sectional transmission electron microscope (TEM) image of the gate stack with ZrO_2 gate dielectric, depicting an abrupt interface between ZrO_2 and AlGaN barrier.

III. Device Results and Discussion

A. High-k ZrO_2 and Interface Characterization

The chemical composition of the ALD ZrO_2 gate dielectric was investigated by the X-ray photoelectron spectroscopy (XPS) measurement on an as-grown GaN HEMT sample covered by 28-nm ZrO_2. The atomic concentration analysis revealed an O/Zr ratio of 1.79. Fig. 2 depicts the XPS spectrum of Zr 3d core level of the ZrO_2. The spectrum shows doublet peaks with the centered binding energy of 182.3 and 184.7 eV, corresponding to Zr $3d_{5/2}$ and Zr $3d_{3/2}$, respectively. The binding energy of Zr $3d_{5/2}$ in ZrO_2 (oxidation state Zr^{4+}) is close to the reported value [14].

Fig. 3 shows the multifrequency capacitance–voltage (C–V) curves for the two samples, which were measured on circular MOS capacitors (MOSCAPs) with a diameter of 200 μm. The C–V curves of the MOSCAP with ZrO_2 gate dielectric show minimal frequency dispersion, suggesting a low interface trap density. By using a parallel conductance method [13], the interface trap density was extracted to be $\sim 1.2 \times 10^{12}$ $cm^{-2}eV^{-1}$. Correlating the accumulation capacitance of the HEMT to that of the MOSHEMT, the relative dielectric constant of ZrO_2 in this paper was estimated to be as high as ~29, which is much higher than that in [9] and [10]. The dielectric constant of ZrO_2 is a function of its crystalline structure [5]. The high dielectric constant in this paper could be due to the partial formation of tetragonal and/or cubic phase ZrO_2 during the ALD [15]. To verify the speculation, we examined the crystal quality of the ALD ZrO_2 with high-resolution TEM and X-ray diffraction (XRD). Fig. 4(a) shows the cross-sectional high-resolution TEM image of ZrO_2 on AlGaN barrier. In addition to the abrupt interface between ZrO_2 and AlGaN, the ZrO_2 is found to be polycrystalline with observable lattice fringes. The appearance of Moiré fringes indicates the overlapping of crystal grains with different orientations. The XRD measurement for a 28-nm ZrO_2 on Si (001) substrate clearly depicts peaks at ~30.4 and ~35.2 arcsec [Fig. 4(b)], which corresponds to certain crystal planes of tetragonal phase and cubic phase ZrO_2, confirming the existence of tetragonal and/or cubic phase of ZrO_2 in this paper [16]. Gate dielectrics with such a high dielectric constant can result in effective coupling of the gate bias to the surface potential of the barrier; thus, the negative shift in the threshold voltage of the MOSHEMT with such a thick ZrO_2 gate dielectric is rather limited. On the other hand, negative charges from F^- residual due to the gate window opening might exist at the ZrO_2/AlGaN interface, which could reversely shift the threshold voltage to the positive direction. As a combined effect, only a small difference in the threshold voltage of C–V curves for the SG HEMTs and ZrO_2-gated MOSHEMTs is observed.

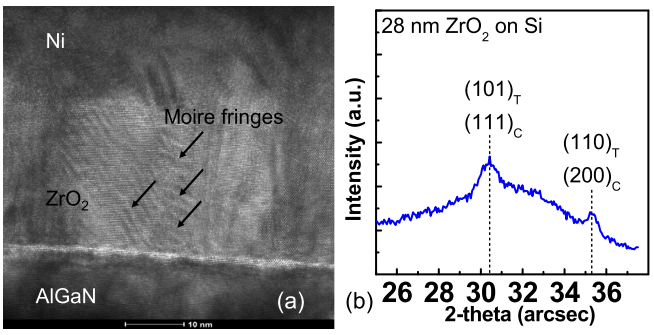

Fig. 4. (a) Cross-sectional TEM image of the ZrO_2 in this paper. (b) XRD pattern of 28-nm ZrO_2 on Si.

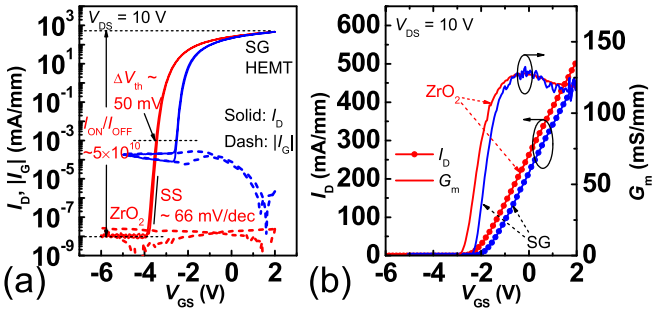

Fig. 5. Comparison of transfer characteristics of MOSHEMTs with ZrO_2 gate dielectric and HEMT with SG (a) in semilog scale and (b) linear scale.

B. DC and Gate-Lag Performance

Fig. 5 shows the comparison of the double-sweep transfer characteristics of representative devices from the sample with ZrO_2 gate dielectric and from the reference sample. The ZrO_2-gated device exhibits a very low OFF-state leakage of 1×10^{-8} mA/mm at V_{DS} of 10 V, which is four orders of magnitude lower than that of the SG HEMTs. The low OFF-state leakage current results in an extremely high ON/OFF current ratio of $\sim 5 \times 10^{10}$, which is the highest value achieved in any reported GaN MOSHEMTs with ZrO_2 gate dielectric, to the best of our knowledge. Even though the ZrO_2 gate dielectric is 28 nm thick, the SS is still as small as 66 mV/dec, indicating efficient gate control over the channel. The nearly ideal SS is also the lowest value among all the ZrO_2-gated GaN MOSHEMTs ever reported. For comparison, the SS is 94 mV/dec for the SG HEMTs. The double-sweep transfer characteristics of the device with ZrO_2 also exhibit a negligible hysteresis of 50 mV (at a sweeping rate of 800 mV/s). The forward breakdown voltage of the MOS gate stack is 11.8 V, revealing a breakdown strength of 4.2 MV/cm for the 28-nm ZrO_2 gate dielectric in this paper. The breakdown field can be further improved by optimizing the ZrO_2 deposition conditions. Moreover, the MOSHEMT with ZrO_2 gate dielectric shows a high peak transconductance of 127 mS/mm, which is very close to that (132 mS/mm) of the SG HEMT, even though the gate-to-channel distance in the MOSHEMTs is 28 nm larger than that of the HEMTs.

Fig. 6 shows the comparison of the output characteristics of the ZrO_2-gated MOSHEMTs and SG HEMTs under both dc and gate-pulsed conditions. The saturation drain current at V_{GS} of 2 V is 550 and 415 mA/mm for the MOSHEMT and HEMT, respectively. The slightly higher maximum drain current in the output curve measurement of the MOSHEMT than that in the transfer measurement may be due to the alleviated trapping effect or neutralized negative charges in the gate stack by the prolonged ON-state positive-gate bias stress time during the V_{DS} sweeping. The specific ON-resistances ($R_{ON,sp}$) of the MOSHEMT and HEMT are calculated to be 2.3 and 3.1 m$\Omega \cdot$ cm^2, respectively, taking a 1.5-μm transfer length for each ohmic contact into account. The enhanced drain current and reduced ON-resistance in MOSHEMTs signify the passivation effect of ZrO_2. For the gate-pulsed measurement, the quiescent gate bias V_{GS0} was -10 V, the pulsewidth was 500 μs, and the pulse period was 500 ms. The dc and pulsed output characteristics of the MOSHEMTs show minimal dispersion, revealing little gate-lag effect in the device. In contrast, the SG HEMT exhibits considerably larger dispersion between the dc and gate-pulsed measurements. The suppressed gate-lag effect in the MOSHEMTs implies effective surface passivation of ZrO_2 gate dielectric to mitigate the electron trapping in the gate stack under OFF-state gate stress.

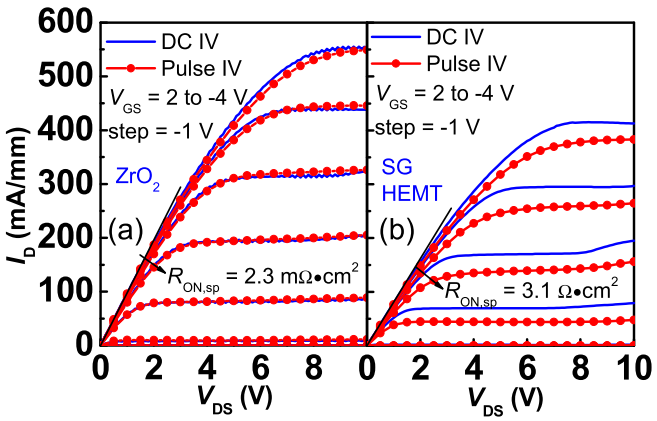

Fig. 6. Comparison of dc and gate-pulsed output characteristics of (a) ZrO_2-gated MOSHEMTs and (b) SG HEMTs.

C. OFF-State Performance

Fig. 7(a) plots the OFF-state I_D versus drain bias for the MOSHEMTs with ZrO_2 gate dielectric. V_{BR} is as high as 1084 V when I_D reaches 1 μA/mm with the substrate floating, resulting in a high-power figure of merit (FOM $= V_{BR}^2/R_{ON,sp}$) of 511 MW/cm^2. The OFF-state I_D shown in the inset is as low as 1.5 nA/mm at V_{DS} of 200 V. Benefiting from the high-quality ZrO_2, the drain-to-gate leakage under reversed V_{GD} has been greatly suppressed. The eventual OFF-state I_D arises from the source terminal. The high breakdown voltage with a low leakage current suggests the excellent current-blocking capability of the MOS gate stack and good management of peak electric field at the gate edge on the drain side. However, V_{BR} of the MOSHEMTs will be decreased to 570 V defined at I_D of 1 μA/mm when the substrate of the sample is grounded. The drain leakage current mainly comes vertically from the substrate terminal. The breakdown voltage can be further improved with thicker carbon-doped buffer. Since the HEMT shows a high OFF-state leakage current from the beginning

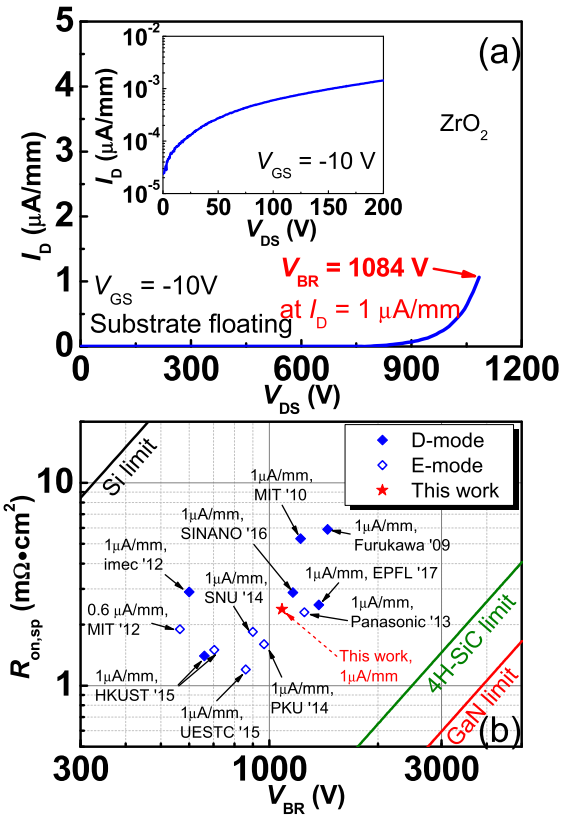

Fig. 7. (a) OFF-state drain leakage current versus drain bias. Inset: semilog plot of I_{DS} for V_{DS} under 200 V. (b) Benchmarking of $R_{ON,sp}$ versus V_{BR} of GaN MOSHEMTs in this paper with the state-of-the-art GaN E/D-mode (MOS)HEMTs on Si by defining V_{BR} at $I_{OFF} \leq 1$ μA/mm.

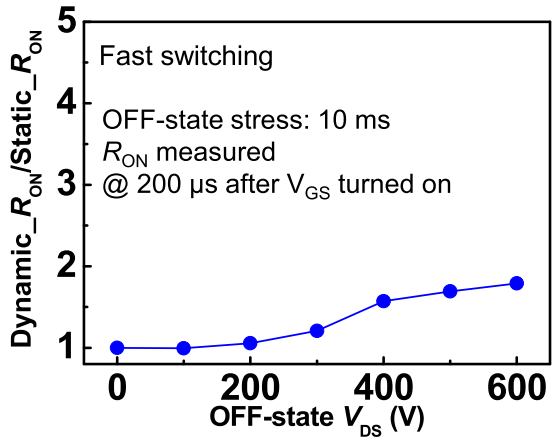

Fig. 8. Dynamic R_{ON} over static R_{ON} ratio as a function of OFF-state drain bias. The substrate was floating during the measurement.

due to the high gate-leakage current, the breakdown voltage is even less than 100 V defined at I_D of 1 μA/mm. Fig. 7(b) benchmarks $R_{ON,sp}$ versus V_{BR} of the GaN MOSHEMTs using ZrO_2 gate dielectric in this paper with the state-of-the-art GaN E/D-mode (MOS)HEMTs on Si by defining V_{BR} at I_{OFF} of 1 μA/mm. The MOSHEMT in this paper shows a well-balanced relationship between $R_{ON,sp}$ and V_{BR}, which is comparable to the best device results reported recently.

D. Dynamic ON-Resistance Characterization

The dynamic R_{ON} for the ZrO_2-gated MOSHEMT was evaluated using a fast switching high-voltage measurement.

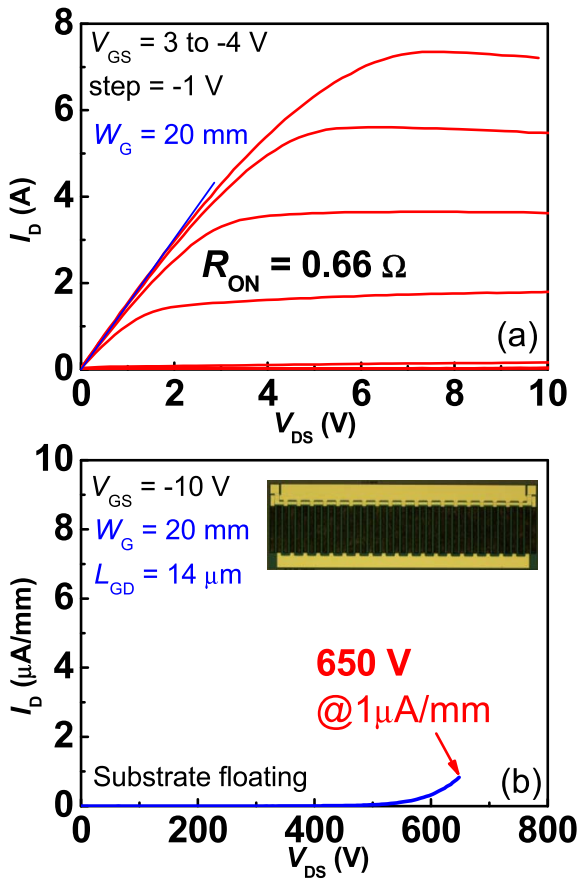

Fig. 9. (a) Output characteristics and (b) OFF-state leakage current of large-area GaN MOSHEMTs with 20-mm gate width. The inset in (b) shows the top-view optical microscope image of the large-area device.

The measurement setup is similar to that described in [17]. The ON-state was set as $V_{GS} = 2$ V and $V_{DS} = 1$ V. At the OFF-state, V_{GS} was fixed at -5 V and the OFF-state stress time was 10 ms. The dynamic R_{ON} was measured at 200 μs after switching from OFF- to ON-state. The substrate of the sample was floating during the measurement. Fig. 8 plots the dynamic R_{ON} to static R_{ON} ratio under various OFF-state drain voltages. A slight degradation of R_{ON} is observed with the increase in drain bias. Nevertheless, the dynamic R_{ON} is maintained to be only 1.78× the static value at V_{DS} of 600 V, indicating effective suppression of current collapse. In addition to the effective surface passivation of bilayer SiN in the access region and reduction of peak electric field using gate-connected field plate, the low dynamic-to-static R_{ON} ratio also reveals the stable gate stack with mitigated electron trapping and robust device operation under high-voltage stress using the ZrO_2 gate dielectric. Due to the low breakdown voltage of the SG HEMTs, the high-voltage dynamic R_{ON} measurement was not performed. Given the severe gate lag in the HEMT shown in Fig. 6(b), the peak electric field at the gate edge will aggravate the trapping effect in the gate stack if it is under high-voltage OFF-state V_{DS} stress. As a result, more serious degradation in dynamic R_{ON} can be anticipated in the HEMT when compared to the ZrO_2-gated MOSHEMT. Hence, it would be beneficial to use gate dielectrics to passivate the barrier surface in the gate stack and suppress the dynamic R_{ON} degradation.

E. Large-Area GaN MOSHEMTs

After validating the high-k ZrO_2 as an excellent gate dielectric, we also fabricated large-area ZrO_2/AlGaN/GaN MOSHEMTs with a maximum gate width of 20 mm. The devices featured a multifinger layout to reduce the gate resistance with each finger width of 500 μm. The final power metal layer for interconnection is 800 nm in thickness. Other device dimensions are the same as the aforementioned small ones. A top-view microscope image of the device with 20-mm gate width is shown in Fig. 9 (inset). The large-area device exhibited a maximum pulsed output current of 7.4 A and a low accompanied R_{ON} of 0.66 Ω, as shown in Fig. 9(a). The current density at V_{GS} of 2 V is only 280 mA/mm, which is relatively low compared to that of the small devices, probably due to the large contact resistance resulted from the long and thin power metal bar for the source/drain contact in the large-area devices. Taking the whole active area of the device into account along with the exclusion of the bonding pad area, $R_{ON,SP}$ is calculated to be 2.64 m$\Omega \cdot$ cm^2. Fig. 9(b) shows the OFF-state drain leakage current of the large-area device. The substrate is floating during the OFF-state measurement. Attributed to the excellent leakage-blocking capability of the MOS gate stack and high-resistivity GaN buffer, the device with 20-mm gate width exhibited a high breakdown voltage of 650 V defined at an OFF-state I_D of 1 μA/mm. The OFF-state I_D mainly arises from the source terminal. Although the breakdown voltage of the large devices is degraded compared to that of the small ones, resulting from the uniformity concern from multiple factors including epilayers, passivation technology, and line edge roughness of gate and drain metal fingers (local high electric field might exist due to the nonsmooth metal edge by the liftoff process), the value of 650 V is still decent to suggest the uniform gate control over the channel for the 20-mm-wide MOSHEMTs using the ZrO_2 gate dielectric in the MOS stack. To the best of our knowledge, this is also the first demonstration of large-area GaN MOSHEMTs on Si with a high-k ZrO_2 gate dielectric.

IV. Conclusion

In conclusion, we have demonstrated high-performance GaN power MOSHEMTs on Si with an ALD ZrO_2 gate dielectric. The gate control over the channel can be greatly enhanced by implementing the high-k ZrO_2 in the gate stack. OFF-state leakage current can also be significantly suppressed; thus, a high breakdown voltage is achieved. The high-quality gate stack also facilitates stable device operation, as evidenced by the small dynamic-to-static ON-resistance ratio. The successful demonstration of large-area devices reveals excellent uniformity of the MOS gate stack. The results show the enormous potential of using high-k ZrO_2 as a gate dielectric in GaN MOSHEMTs for efficient power-switching applications.

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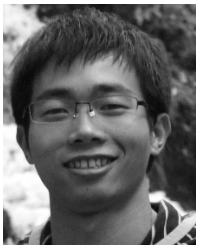

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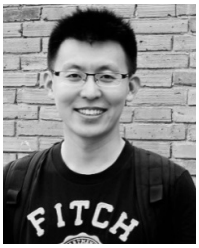

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