Enhancement-Mode GaN MOS-HEMTs With Recess-Free Barrier Engineering and High-k ZrO₂ Gate Dielectric

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Abstract—Enhancement-mode GaN MOS-HEMTs with a uniform threshold voltage ($V_{th} \sim 2.2 \pm 0.25$ V at $I_D = 1 \, \mu A/mm$) have been achieved by a recess-free barrier engineering technique in conjunction with a high-κ dielectric. The design includes an ultrathin (~6 nm) Al$_{0.2}$Ga$_{0.8}$N barrier preserving the two dimensional electron gas (2DEG) mobility underneath the gate and a selective area barrier regrowth to restore the 2DEG at the access regions. A high-κ ZrO$_2$ gate dielectric was employed to enhance the gate control over the channel. The common issue of recess-induced damage was mitigated. The high-quality gate stack results not only in a highly uniform and large $V_{th}$, but also small hysteresis, minimal gate lag, low on-resistance, and high output current in the E-MOS-HEMTs.

Index Terms—Enhancement-mode, ZrO₂, GaN, MOS-HEMTs, barrier, regrowth.

I. INTRODUCTION

GaN metal-oxide-semiconductor high electron mobility transistors (MOS-HEMTs) with normally-off property are highly desired for efficient power switching applications to simplify circuit design and to ensure fail-safe operation [1]. Compared to p-GaN gate structures in commercialized enhancement-mode (E-mode) transistors, the MOS gate structure described here can greatly enlarge the forward gate voltage swing, enhancing the immunity to large gate voltage overshoot spikes, thus improving system reliability [2]–[10]. Over gate recess (i.e. complete removal of the barrier layer) is often performed in MOS-HEMTs to achieve a positive threshold voltage ($V_{th}$), forming a MOSFET structure where the gate dielectric directly contacts the channel [5], [6], [10]–[13]. However, the carrier mobility can be severely degraded due to severe scattering effect in the etch-exposed channel, increasing the device on-resistance ($R_{on}$). Moreover, high density trap states (in the order of $10^{13} \sim 10^{14}$) are usually present at the dielectric/channel interface, which is detrimental to the $V_{th}$ uniformity and device reliability [14].

Alternatively, partial gate recess (i.e. leaving a few nm of the barrier layer) keeps the heterojunction intact, maintaining relatively high carrier mobility needed for low $R_{on}$ [7], [8], [15]. However, the reduced $R_{on}$ comes with the disadvantage of a compromised $V_{th}$, typically $\sim +0.5$ V, because of weakened gate control over the channel. The undermined gate control is partially a result of increased gate-to-channel distance. More importantly, it is a consequence of both high density of electrically active traps at the interface introduced by the recess process, together with the thick gate dielectric with a relatively low dielectric constant ($\varepsilon_r < 10$). Despite great improvements on recessed-gate MOS-HEMTs, this approach still shows some limitations in obtaining devices with a $V_{th} > 1.5$ V combined with $R_{on}$ below 10 $\Omega \cdot$ mm [16]. Another approach to achieve E-mode operation maintaining the AlGaN/GaN heterojunction is the introduction of negative charges (e.g., F~) at the gate stack [17]–[19]. Relatively high threshold voltages have been achieved. However, the thermal stability of the introduced negative charges remains a concern in such a device structure.

To mitigate the etching induced damages from the gate recess process, selective area regrowth techniques have been employed to reconstruct the barrier layer in the access region by both our group and other researchers [20]–[22]. On the other hand, E-mode MOS-HEMTs with ultrathin barrier AlGaN/GaN heterostructure were also demonstrated recently [9], [23]. Excellent gate stacks with uniform threshold voltages were achieved using these approaches.

In this work, we demonstrate an E-mode GaN MOS-HEMT with a novel recess-free barrier engineering technique and a high-κ ZrO₂ gate dielectric. The new gate design and process enabled a truly normally-off MOS-HEMT with large and uniform $V_{th}$ over 2 V at a drain current ($I_D$) of 1 $\mu A/mm$, a low $R_{on}$ of 9.2 $\Omega \cdot$ mm, and a high output current of 590 mA/mm.

II. HETEROSTRUCTURE DESIGN AND DEVICE FABRICATION

The AlGaN/GaN heterostructure was grown on a 6-inch n-type Si (111) substrate using an Aixtron MOCVD system. The epilayers, shown in Fig. 1(a), consist of a composite buffer including a 1.2-μm step-graded AlGaN and a 2.5-μm C-doped GaN, a 500-nm undoped GaN channel, a 1-nm AlN spacer, and a 6-nm Al$_{0.2}$Ga$_{0.8}$N barrier. The ultrathin barrier and relatively low Al composition prevent the formation of two dimensional electron gas (2DEG) at the Al$_{0.2}$Ga$_{0.8}$N/GaN hetero-interface without any gate bias. The fabrication process started with dummy gate formation

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using 100 nm PECVD SiO$_2$ as the regrowth mask. The region outside of the dummy gate was exposed by selectively removing SiO$_2$ using buffered oxide etch (BOE). Additional 20 nm of Al$_{0.3}$Ga$_{0.7}$N was selectively grown on the exposed Al$_{0.2}$Ga$_{0.8}$N surface. Higher Al composition was chosen for the regrown barrier to achieve higher carrier concentration thus lower sheet resistance in the access region [24]. Afterwards, source/drain (S/D) Ohmic metal of Ti/Al/Ni/Au was formed and followed by a 100 nm PECVD SiN passivation. PECVD SiN in the gate region was then selectively removed using low power dry etching and BOE wet etching, and the exposed barrier surface was cleaned by an O$_2$-plasma/HCl treatment [25].

A 23 nm ZrO$_2$ was then deposited at 200 °C by atomic layer deposition (ALD) as the gate dielectric. Ni/Au-based metal stack was used to form the gate contact. Afterwards, another 300 nm PECVD SiN was deposited for device passivation. After opening the contact holes, probing pad metal was finally deposited. In contrast to the conventional recessed-gate E-mode technology, the barrier layer in this design was never attacked by any dry/wet-etching during the whole device fabrication process. Therefore, process-induced damage to the barrier was minimized and a high-quality interface between ZrO$_2$ and Al$_{0.2}$Ga$_{0.8}$N can be achieved. Fig. 1(b) depicts a cross-sectional transmission electron microscope (TEM) image of the as-grown heterostructure covered by 23 nm ZrO$_2$, showing an atomically abrupt interface. The ALD ZrO$_2$ is amorphous for the first ~4 nm at the beginning of the deposition and then becomes polycrystalline with the increase of deposition cycles. The atomic force microscope image of the gate trench and adjacent regrown barrier after the SiO$_2$ dummy gate removal is shown in Fig. 1(c). The root mean square roughness of the Al$_{0.2}$Ga$_{0.8}$N surface in the gate trench remains to be 0.8 nm across a 5 μm × 5 μm scanned area and the regrown Al$_{0.2}$Ga$_{0.8}$N barrier in the access regions also shows smooth surface morphology. Fig. 1(d) displays the cross-sectional gate trench profile, showing a regrown barrier thickness of ~19.5 nm. Unless otherwise specified, the devices reported in this letter feature a gate length ($L_G$) of 1.5 μm, both a gate-source ($L_{GS}$) and a gate-drain ($L_{GD}$) distance of 3 μm, and a gate width ($W_G$) of 10 μm.

### III. DEVICE RESULTS AND DISCUSSION

Before SiN passivation, the carrier transports of the 2DEG channel in the Al$_{0.2}$Ga$_{0.8}$N/GaN heterostructure with and without the added 20 nm regrown Al$_{0.3}$Ga$_{0.7}$N barrier are compared in Fig. 2. The current measured between two Ohmic pads with a 16-μm space for the as-grown heterostructure is in the order of several nA/mm at a bias of 10 V, suggesting no 2DEG formation at the hetero-interface. While, for the heterostructure with the 20 nm regrown Al$_{0.3}$Ga$_{0.7}$N barrier, the current became as high as 650 mA/mm. The dramatic increase of the output current suggests successful recovery of the 2DEG at the Al$_{0.2}$Ga$_{0.8}$N/GaN heterojunction in the access region after barrier regrowth. It should be noted that, the difference of the Al composition in the regrown Al$_{0.3}$Ga$_{0.7}$N barrier and the as-grown Al$_{0.2}$Ga$_{0.8}$N is not large enough to induce high density sheet carriers at the interface of two AlGaN layers. In addition, due to the severe alloy scattering and interface scattering, the electron mobility at the Al$_{0.3}$Ga$_{0.7}$/Al$_{0.5}$Ga$_{0.5}$N interface will be very low, compared to that of the 2DEG at the AlGaN/GaN heterojunction. Therefore, the 2DEG at the AlGaN/GaN heterojunction will be the dominated current conduction path between the drain and source after the barrier regrowth.

Fig. 3(a) plots the double sweep $I_D$ and $I_G$ versus $V_{GS}$ at a $V_{DS}$ of 10 V for the fabricated E-mode MOS-HEMTs. The device shows a $V_{th}$ as large as 2.1 V defined at $I_D$ of 1 μA/mm, which is in the range of the non-fluorinated GaN MOS-HEMTs to date. Moreover, the device shows a small subthreshold slope (SS) of 95 mV/dec, negligible $V_{th}$ hysteresis ($\Delta V_{th}$) of ~0.1 V, and a high on/off ratio.
current ratio of $\sim 10^9$. Even at a large forward $V_{GS}$ bias of 8 V, the $I_D$ to $I_G$ ratio is still more than $10^7$, suggesting excellent current-blocking capability of the MOS gate stack. Fig. 3(b) depicts the transfer characteristics of the device in linear scale. The $V_{th}$ is as high as 3 V by linear extrapolation. The peak transconductance $G_{max}$ is as high as 35 mS/mm, suggesting efficient gate modulation over the channel using the high-$k$ ZrO$_2$ gate dielectric.

Fig. 4 shows the DC and gate pulsed output characteristics. For the gate pulsed measurement, the pulse width is 500 $\mu$s, the pulse period is 1 s, and the quiescent gate bias is 0 V. Minimal dispersion between DC and gate pulsed $I_{DS}$-$V_{DS}$ suggests little gate lag effect. The maximum saturation drain current ($I_{DS,max}$) is 590 mA/mm. The static $R_{on}$ is 9.2 $\Omega$·mm at $V_{GS}$ of 8 V, corresponding to a specific $R_{on}$ of 0.96 m$\Omega$·cm$^2$, with 1.5 $\mu$m transfer length of each Ohmic contact taken into account for the calculation of device area. The low $R_{on}$ is attributed to the buried channel that maintains high field-effect mobility $\mu_{FE}$, which is extracted from a long-gate MOS-HEMT with $W/L$ of 100 $\mu$m/50 $\mu$m biased at $V_{GS}$ of 0.1 V, as shown in Fig. 4(b). The peak $\mu_{FE}$ is determined to be 850 cm$^2$/V·s, which is $\sim 5$ times higher than that of the state-of-the-art fully recessed GaN MOSFETs [26]–[28]. As a result of the yet to be optimized SiN passivation process, the breakdown voltage of the E-mode MOS-HEMTs is still relatively low.

Fig. 5(a) plots the $V_{th}$ distribution measured on 46 fabricated devices. The $V_{th}$ shows a narrow distribution with an average value of 2.19 V and a standard deviation of 0.25 V, suggesting excellent gate stack uniformity. Parallel conductance method was employed on a circular-shaped MOS capacitor with a diameter of 200 $\mu$m to map the interface trap density ($D_i$) in the gate stack, as shown in Fig. 5(b) [29]. Benefiting from the recess-free barrier engineering technique and high quality ZrO$_2$ gate dielectric, the $D_i$ was extracted to be only $\sim 3 \times 10^{12}$ cm$^{-2}$eV$^{-1}$, which is also much lower than that of the state-of-the-art recessed-gate interfaces [8].

Fig. 6 benchmarks the $I_{DS,max}$ versus $V_{th}$ (defined at $I_D$ of 1 $\mu$A/mm) of devices in this work with other state-of-the-art E-mode GaN FETs with a MOS gate structure. Most of the reported devices show a small $V_{th}$ less than 1.5 V. The device in this letter shows not only a larger $V_{th}$, but also delivers a competitive $I_{DS,max}$, suggesting the advantages of the device structure and techniques developed in this work.

IV. CONCLUSION

This work demonstrates an E-mode GaN MOS-HEMT with a large $V_{th}$ using a novel recess-free barrier engineering technique and a high-$k$ ZrO$_2$ gate dielectric. The heterostructure design includes an ultrathin (6 nm) AlGaN barrier with 20% Al composition, resulting in a normally-off channel. The normally-on access regions connecting the normally-off channel are created by selective regrowth of thicker barriers. High electron mobility and conductance in the channel are preserved in the on condition leading to a high $I_{DS,max}$ of 590 mA/mm. The high-$k$ ZrO$_2$ gate dielectric couples the gate potential to the channel efficiently, realizing large positive threshold voltage while retaining low leakage current. Selectively regrown barrier covering the access regions restores the 2DEG and enables a low on-resistance without sacrificing the initial barrier surface quality. The unique design and process technique show great promise in achieving high-performance E-mode GaN MOS-HEMTs.

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