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Heterointerface study of InAs/GaSb nanoridge heterostructures grown by metal organic chemical vapor deposition on V-grooved Si (0 0 1) substrates

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ABSTRACT

InAs/GaSb nanoridge heterostructures were grown on V-grooved (0 0 1) Si by metal organic chemical vapor deposition. Combining the aspect ratio trapping process and a low temperature GaAs buffer, we demonstrated high quality GaSb nanoridge templates for InAs/GaSb heterostructure growth. Two different interfaces, a transitional GaAsSb and an InSb-like interface, were investigated when growing these heterostructures. A 500 °C growth temperature in conjunction with a GaAsSb interface was determined to produce the optimal interface, properly compensating for the tensile strain accumulated when growing InAs on GaSb. Without the need for a complicated switching sequence, this GaAsSb-like interface utilized at the optimized temperature is the initial step towards InAs/GaSb type II superlattice and other device structures integrated onto Si.

1. Introduction

The InAs/GaSb material system has been well investigated for its unique broken gap band alignment and exceptional carrier mobilities, making it a viable material for infrared photodetectors, infrared light emitting diodes and tunneling field effect transistors [1–3]. One of the challenges preventing this material system from being utilized for this wide variety of devices is the lack of large-size, lattice-matched, semi-insulating substrates. Commonly used GaSb substrates are typically 2-in in diameter, of low-resistivity, and costly. Previous research on heteroepitaxy of GaSb on larger wafers of GaAs and Si has been conducted mostly by molecular beam epitaxy (MBE).

There are few reports of InAs/GaSb heterostructures grown using metal-organic chemical vapor deposition (MOCVD) due to the precision required in tuning the interface between these two materials [4,5]. However, the general consensus is that a GaAs-like heterointerface introduces threading dislocations due to the inability for this interface to compensate for the accumulated tensile strain [4–6]. Alternatively, the use of an InSb-like interface has been shown to be successful in managing accumulated tensile strain [7]. Unfortunately, this type of interface has only been shown to be feasible when using MBE with a lower growth temperature. An important consideration when using MOCVD is that InSb will decompose at growth temperatures suitable for GaSb/InAs, given that the melting temperature of InSb is approximately 535 °C. As a result, there have been reports of fine-tuned switching sequences to achieve proper strain compensation at the interface by transitioning from the alloys of GaSb and InAs [4,8]. The growth of these heterostructures on Si presents an even larger challenge due to the large lattice mismatch of InAs/GaSb and Si. One common approach to integrating these narrow band gap materials onto Si is through the use of an AlSb growth initiation layer [9,10] and an interfacial misfit (IMF) growth mode [11]. Unfortunately, AlSb epitaxy using MOCVD is difficult due to carbon contamination and the difficult optimization of the growth temperature [12].

Having established V-grooved Si substrates that have been used to successfully grow high quality GaAs nanoridges [13], here we report the growth of GaSb and InAs/GaSb heterostructures on these same substrates. The V-grooved Si proves to be essential in growing high quality III-V crystals without the presence of anti-phase boundaries [14] while the use of aspect ratio trapping reduces the density of threading dislocations. By beginning growth with a low-temperature (LT) deposited GaAs stress relaxing layer, a unique set of twins and stacking faults, instead of dislocations, are formed on {1 1 1} facets of Si [13]. This is followed by the integration of GaSb on Si [15] using a growth sequence inspired

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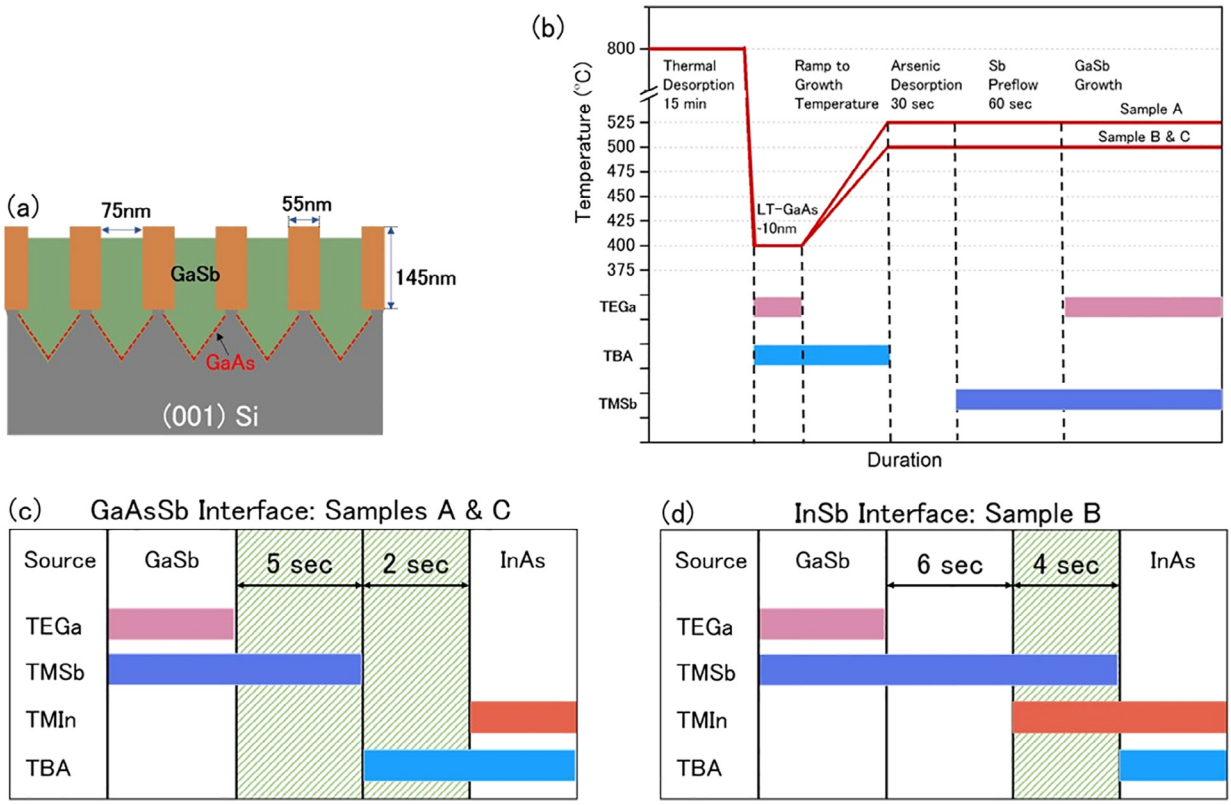

Fig. 1. (a) Dimensions of the nanopatterned Si; (b) Schematic of the IMF inspired growth sequence for GaSb showing the split between growth temperatures of 500 °C and 525 °C (dimensions not to scale); (c) Switching sequence used to obtain a GaAsSb alloyed interface with a growth temperature of 525 °C for sample A and 500 °C for sample C; (d) Switching sequence used to obtain an InSb-like interface with a growth temperature of 500 °C for sample B.

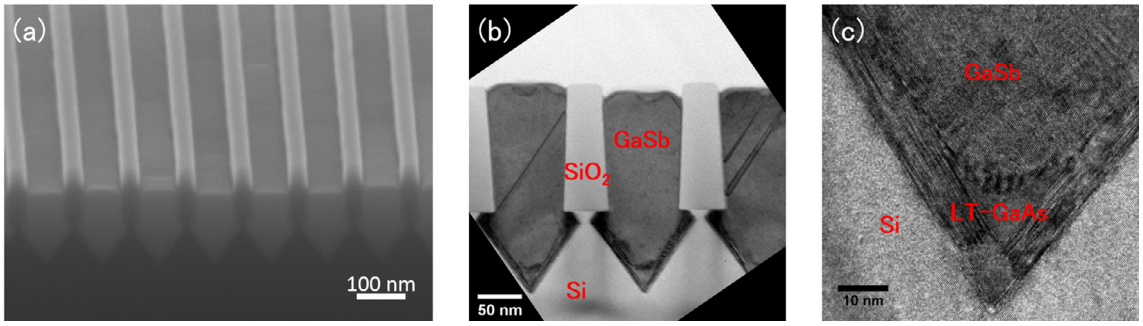

Fig. 2. (a) Tilted (70°) SEM image of GaSb nanoridges showing textured dashes on the surface indicating stacking faults propagating in the plane perpendicular to the V-groove; (b) X-TEM image of GaSb nanoridges showing stacking faults originating from the SiO_2 sidewalls and also the Si V-groove; (c) Heterointerface lined with misfit dislocations.

by the IMF growth mode. When determining the optimal interface between InAs and GaSb, a GaAsSb-like interface along with an InSb-like interface was compared. To make this comparison, the growth temperature for the InSb-like interface and accompanying heterostructure was lowered to be sufficiently far from the decomposition temperature of InSb. These InAs/GaSb heterostructures were evaluated for their defect generation at the heterointerface using transmission electron microscopy (TEM).

2. Experimental methods

Nominal microelectronics standard (0 0 1) Si substrates without offcut were patterned using SiO_2 stripes through dry etching. V-grooves with (1 1 1) facets between these SiO_2 stripes were formed using a dilute KOH solution at 70 °C and used as templates for growth. As shown in Fig. 1(a), the oxide stripes have a width of 55 nm, a spacing of 75 nm, and a height of 145 nm. An AIXTRON 200/4 horizontal MOCVD reactor was used to perform the growth, with tertiarybutylarsine (TBA), triethylgallium (TEGa), trimethylantimony (TMSb), and trimethylindium (TMIn) as the sources. The growth first begins with an oxide desorption for 15 min at 800 °C followed by the growth of a 10 nm GaAs buffer at 400 °C. The temperature is then raised to the heterostructure growth temperature while under a TBA flux. The TBA flux was paused and while under a H_2 overpressure, As was allowed to desorb from the GaAs surface for 30 s to form a Ga-rich surface. For 60 s, TMSb flux was opened to form the first monolayer of GaSb. The GaSb

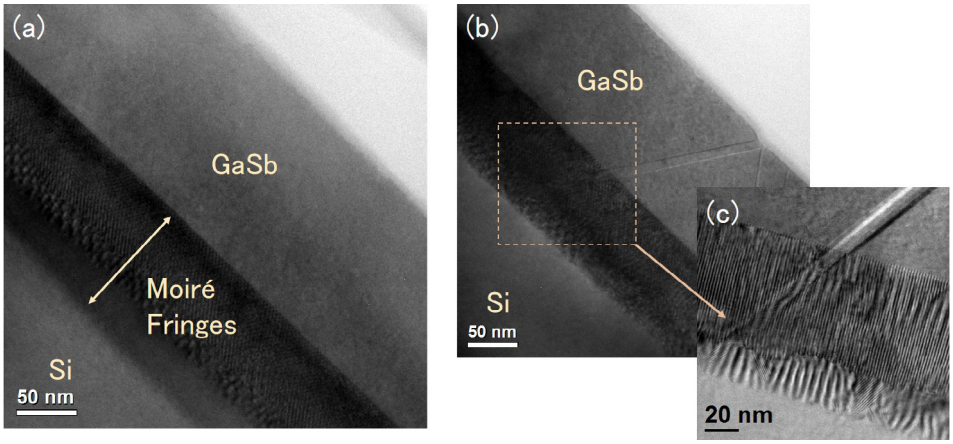

Fig. 3. (a) X-TEM image of the GaSb nanoridges along the ridge direction showing a defect free area; (b) X-TEM image of the GaSb nanoridges along the ridge direction showing stacking faults originating from the V-groove.

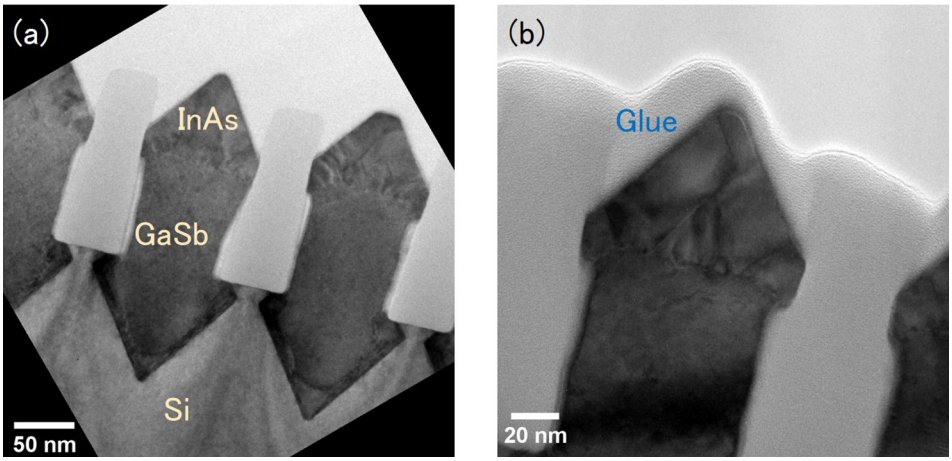

Fig. 4. (a) TEM image of sample A which is grown at 525 °C with a GaAsSb alloyed interface; (b) Clear generation of defects at the heterointerface.

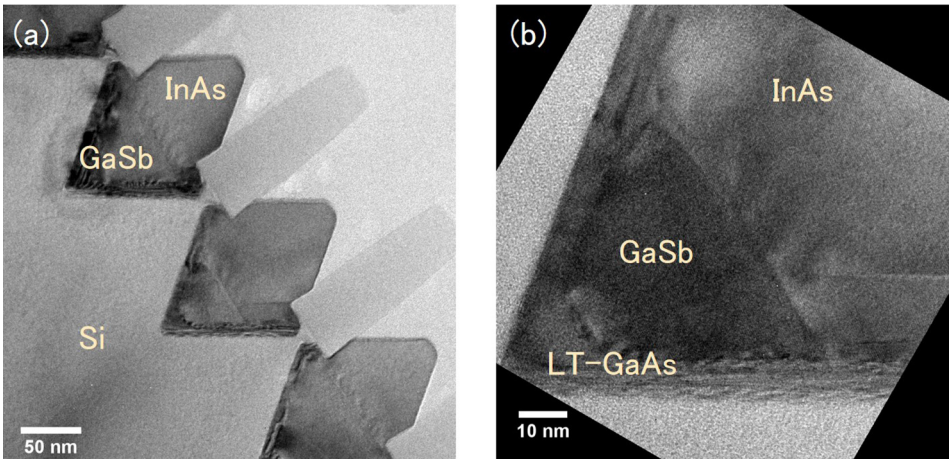

Fig. 5. (a) TEM image of sample B which is grown at 500 °C with an InSb interface; (b) Relatively lower density of defects generated at the heterointerface.

growth continued with addition of the TEGa flux under an optimized V/III ratio of 1.9. The IMF inspired growth sequence for GaSb is summarized in Fig. 1(b).

When determining the optimal growth conditions of InAs, three samples have been prepared. A GaAsSb alloyed interface was chosen for sample A and C, for its simple switching sequence, whereas an InSb-like interface was chosen for sample B, for its effectiveness in strain relief as shown in MBE grown InAs/GaSb heterostructures. Sample A was grown at 525 °C and Samples B and C were grown at 500 °C. The transition to growing InAs with a GaAsSb alloyed interface begins by stopping the TEGa flux and pausing for 5 s. The TMSb flux is terminated and the TBA flux is opened

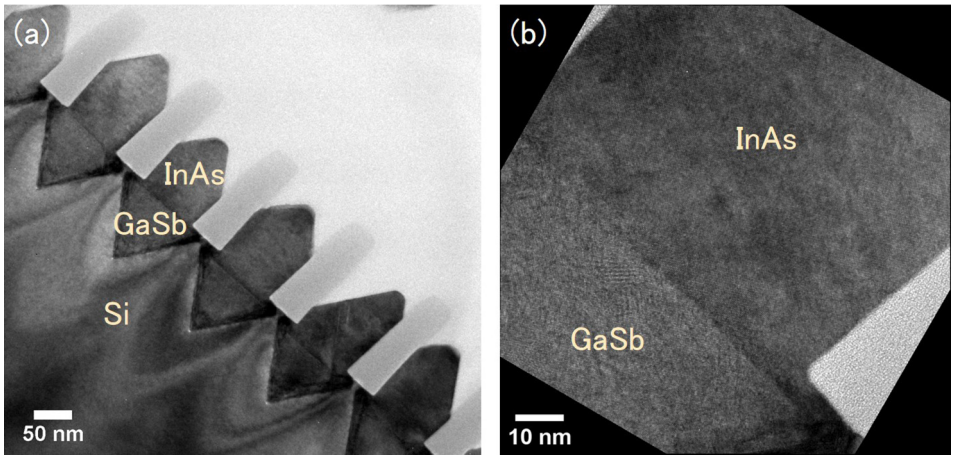

Fig. 6. (a) TEM image of sample C which is grown at 500 °C with a GaAsSb alloyed interface; (b) No generation of crystal defects at the heterointerface.

simultaneously. The TBA flow continues for 2 s before the TMIn flux is introduced which marks the growth of InAs under a V/III ratio of 3.0. This specific switching sequence is summarized in Fig. 1(c). For comparison, the InSb-like interface begins after the growth of GaSb with a 6 s interruption under TMSb flux. For 4 s, TMIn flux is opened to grow an InSb-like interface that is followed by the InAs growth with the same V/III ratio of 3.0. This switching sequence used to grow sample B is detailed in Fig. 1(d). As mentioned previously, to adapt the use of this InSb-like interface for an MOCVD system, a growth temperature of 500 °C for the entire heterostructure was adopted to be sufficiently distant from the InSb decomposition temperature of 535 °C.

3. Results and discussion

The GaSb nanoridges that are first grown to provide a suitable template for further heterostructure growth are shown in Fig. 2 (a). The presence of texture on the surface is the propagation of stacking faults in the plane perpendicular to the ridge direction. These stacking faults cannot be trapped by the SiO_2 pillars for this propagation orientation. Using cross sectional transmission electrical microscopy (X-TEM), the heterointerface between the GaSb and the GaAs stress relaxing layer shows texture indicating misfit dislocations as seen in Fig. 2(b) and (c). Although most of these misfit dislocations are 60° instead of 90° dislocations and cannot be described as an IMF array, they effectively release the stress induced by the lattice mismatch. One can observe the presence of stacking faults originating from the V-groove and from the SiO_2 pillars from Fig. 2(b). These stacking faults propagating in the plane parallel to the ridge direction are properly trapped by the SiO_2 sidewalls, in sharp contrast to the stacking faults present in Fig. 2(a).

Looking along the ridge direction, one can observe defect free areas as shown in Fig. 3(a). However, not all areas are defect free and the presence of the stacking faults that lie in the plane perpendicular to the ridge direction are shown propagating towards the surface of the nanoridges in Fig. 3(b). These stacking faults are of the same character as those revealed on the surface on the nanoridges as shown in Fig. 2(a). Examining more closely, these unobstructed stacking faults originate from the V-groove. Nevertheless, these GaSb nanoridges templates are more than suitable for further InAs/GaSb heterostructure growth.

The X-TEM image of sample A with the GaAsSb alloyed interface grown at 525 °C is shown in Fig. 4(a). There is a clear generation of threading dislocations and stacking faults at this heterointerface. The texture in the InAs layer shows the inability of this GaAsSb interface to compensate for the tensile strain that was accumulated. This texture is most prominently shown in Fig. 4(b). When comparing this to the sample B grown at 500 °C using the InSb-like interface, there is a stark contrast between the two.

Fig. 5(a) and (b) shows the results of sample B with the growth sequence described in Fig. 1(d); the InSb-like heterointerface generates no threading dislocations and few stacking faults. Based on these TEM images, it is clear that the InSb-like interface can appropriately compensate for the strain. However, one additional sample was prepared to determine whether the InSb-like interface was in fact the parameter for this improvement or rather the decreased growth temperature. Using the previous GaAsSb interface and performing the growth at 500 °C resulted in sample C as shown in Fig. 6. Interestingly, this specific set of growth parameters also results in no generation of threading dislocations at the heterointerface. As shown in Fig. 6(b), the heterointerface is free of stacking faults and threading dislocations. In fact, there is an even lower density of stacking faults which makes this set of growth parameters even more suitable for InAs/GaSb heterostructure growth when compared to the InSb-like interface. Not only does this GaAsSb interface at 500 °C compensate for the strain, the switching sequence is also simpler to control and easier to employ, making this an attractive alternative to the use of an InSb-like interface.

4. Conclusion

Adopting the good crystalline quality achieved from V-grooved Si and aspect ratio trapping, GaSb nanoridges have been grown using a growth sequence inspired by the IMF growth mode, forming the basis for InAs/GaSb heterostructures. With the use of an alloyed GaAsSb interface, proper compensation for the tensile strain was achieved at a growth temperature of 500 °C preventing the generation of threading dislocations and stacking faults at the InAs/GaSb heterointerface. With the growth techniques required for this high-quality heterointerface determined, integration of InAs/GaSb heterostructures onto Si is a first step towards integrating 6.1 Å compound semiconductors onto Si for optoelectronic and emerging electronic devices.

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