Study of Interface Traps in AlGaN/GaN MISHEMTs Using LPCVD SiN_x as Gate Dielectric

Xing Lu, Kun Yu, Huaxing Jiang, Anping Zhang, *Senior Member, IEEE,* and Kei May Lau, *Fellow, IEEE*

***Abstract*— Interface trapping is one of the most notorious effects that limit device performance in GaN-based MIS high electron mobility transistors (MISHEMTs). In this paper, we present a comprehensive study on interface traps in AlGaN/GaN MISHEMTs using low pressure chemical vapor deposition SiN_x as gate dielectric. We combined the trapping analysis in MIS diodes and actual MISHEMTs to estimate the interface trap state densities (D_{it}) and their distributions in the device, and to investigate their influence on device electrical properties. Two types of interface traps with different emission time constants, designated as "slow" and "fast" traps, were identified and characterized by means of pulse-mode current-voltage measurements and a frequency dependent conductance method. It was found that "fast" traps located in the device access region could be effectively restrained by passivation using plasma enhanced chemical vapor deposition SiN_x. However, "slow" traps, no matter whether located beneath the metal gate or in the access region, were less influenced by passivation. Due to the strong interference of traps in the access region, D_{it} extraction using the conventional conductance method was not accurate for the lateral GaN-based MIS diodes. A modified small-signal equivalent circuit that includes the impedance of traps in the access region is proposed. Proper passivation for the device access region is essential when using the conductance method for GaN-based MIS devices.**

***Index Terms*— AlGaN/GaN MIS high electron mobility transistors (MISHEMTs), current collapse, interface traps, low pressure chemical vapor deposition (LPCVD) SiN_x, passivation.**

I. Introduction

OWING to their excellent material properties, such as large breakdown field, high electron mobility, and good thermal conductivity, GaN-based high electron mobility transistors (HEMTs) are highly attractive for next-generation high-efficiency and high-voltage power applications [1], [2]. In order to suppress the gate leakage and enlarge the gate swing in HEMT devices with a Schottky gate, most recent developments have focused on MIS structures.

Various types of insulators have been deposited on the III–nitride heterostructures as a gate dielectric, such as Al_2O_3 and HfO_2 grown by atomic layer deposition (ALD) [3]–[6], SiO_2 deposited by plasma enhanced chemical vapor deposition (PECVD) [7], [8], and SiN_x grown by PECVD or *in situ* metal-organic chemical vapor deposition [9]–[11]. However, the insertion of a gate dielectric brings in high-density trap states (10^{10} to 10^{14} $cm^{-2}eV^{-1}$) located at the additional dielectric/III–nitride interface. The interface traps are usually induced by structural damage, oxidation-induced defects, or dangling bonds [12]. It has also been found that the interface traps are extremely sensitive to certain fabrication processes, such as surface preparation, dielectric deposition, and postdeposition annealing [13], [14]. The interface traps, always with a broad time constant range, are in electrical communication with the underlying III–nitride heterostructures through a charging/discharging process depending on the surface potential, thus deteriorating the device performance and stability.

Accurate characterization of interface traps is indispensable to the development of high-quality gate stacks and effective surface passivation for GaN-based MISHEMTs. Relatively deep interface traps with long emission time constants usually exist due to the wide bandgap nature of the III–nitride material, restricting its detectable energy depth [15]. A frequency-dependent conductance method has been widely used to evaluate the interface traps in AlGaN/GaN MIS structures [4], [10], [16], [17]. However, the conventional small-signal equivalent circuit model of the conductance method does not consider the influence of the access region in lateral devices, such as GaN-based MISHEMTs, which may cause error in the interface trap extraction.

Studies have shown that passivation can effectively suppress the virtual gate formed by the interface traps physically located at the access region of a GaN-based HEMT [18]. Therefore, with proper access region passivation, an interface trap analysis using the conductance method would be more accurate. In the literature, most reported GaN-based MIS-diodes under test are not well passivated during the extraction of interface traps using the frequency dependent conductance method [4], [10], [17].

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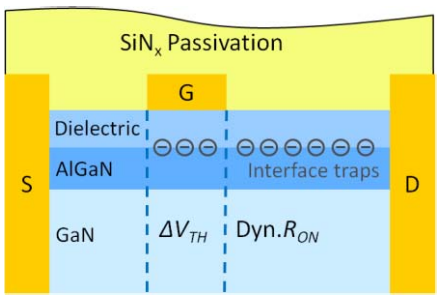

Fig. 1. Interface trap locations and their influence on electrical performance in AlGaN/GaN MISHEMTs.

Previously, it has been reported that interface traps as well as buffer and barrier traps can contribute to current collapse through a similar physical mechanism involving capture and emission of tunneled electrons from the gate metal [18]–[22]. As shown in Fig. 1, interface traps under the gate mostly result in threshold voltage instability, while interface traps in the gate–drain access region can lead to dynamic ON-resistance (Dyn.R_{ON}) degradation due to the depletion of 2-D electron gas (2DEG). The conductance method and most other capacitance measurements are implemented on large-area MIS-diode structures, while an actual MISHEMT device always has a much smaller gate capacitance (typically lower than 1–5 pF). The electric field distribution in a large-area MIS diode is significantly different from that in an actual MISHEMT. The results obtained by analyzing an MIS diode can provide information on the interface traps, but do not give a clear indication of where those traps are located in the MISHEMT or of how they affect the performance of the actual MISHEMT device [19].

Recently, low pressure chemical vapor deposition (LPCVD) SiN_x has been demonstrated as a promising gate dielectric and passivation material for AlGaN/GaN MISHEMTs due to its high-temperature and plasma-free deposition process, which can lead to high film quality and less damage to the AlGaN barrier [23], [24]. In this paper, we present a comprehensive study on interface traps in AlGaN/GaN MISHEMTs with an LPCVD SiN_x gate dielectric. Four types of samples, LPCVD SiN_x/AlGaN/GaN MISHEMTs with and without extra PECVD SiN_x passivation and LPCVD SiN_x/AlGaN/GaN MIS diodes with and without extra PECVD SiN_x passivation, were studied. The MIS diodes were prepared on the same chip as the MISHEMTs. Pulse-mode current–voltage ($I-V$) measurements were performed on the MISHEMTs to evaluate the traps with relatively long emission time constants (designated as "slow" traps), while the frequency-dependent conductance method was implemented on the MIS diodes to estimate the traps with relatively short emission time constants (designated as "fast" traps). We combined the characterizations of both MIS diodes and MISHEMTs to locate and analyze the interface traps. By comparing the devices with and without passivation, the influence of the devices' access region on the interface trap characterization using the conductance method was investigated. Furthermore, we propose a new small-signal equivalent circuit that includes the impedance of the trap states in the access region. The passivation effects for the "fast" and "slow" traps in the fabricated MISHEMTs are also discussed.

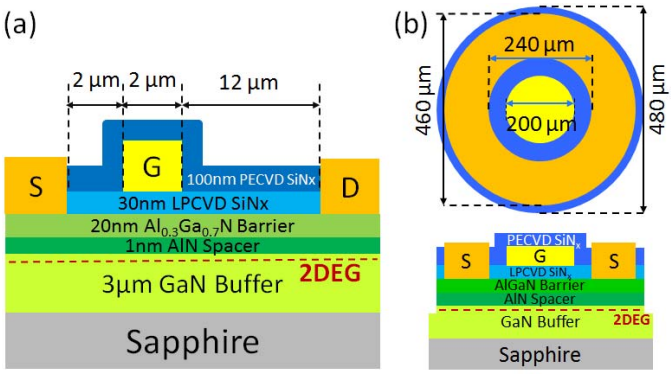

Fig. 2. Schematic diagrams of the LPCVD SiN_x/AlGaN/GaN (a) MISHEMT and (b) MIS diode with PECVD SiN_x passivation.

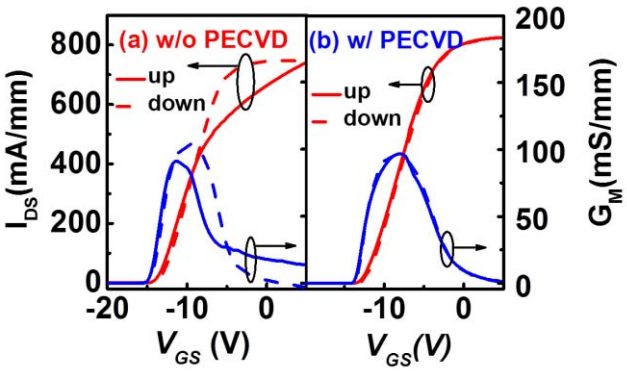

Fig. 3. Double-mode dc transfer curves of LPCVD SiN_x/AlGaN/GaN MISHEMTs with and without PECVD SiN_x passivation (V_{DS} = 10 V).

II. Device Performance

The LPCVD SiN_x/AlGaN/GaN MISHEMTs and MIS diodes in this paper were fabricated using an $Al_{0.3}G_{0.7}N$/GaN-on-sapphire sample. The thicknesses of the LPCVD SiN_x gate dielectric and PECVD SiN_x passivation are 30 and 100 nm, respectively. Fig. 2 shows the architectures of the fabricated LPCVD SiN_x/AlGaN/GaN MISHEMT and MIS diode with an extra PECVD SiN_x passivation. The MISHEMTs discussed in this paper feature a gate length (L_G) of 2 μm, a gate width (W_G) of 10 μm, a gate-to-drain distance (L_{GD}) of 12 μm, and a gate-to-source distance (L_{GS}) of 2 μm. The gate diameter of MIS diode is 200 μm and the distance between the gate and ohmic contact is 20 μm. More details of the device fabrication process can be found in our previous report [25].

A. DC Characteristics of LPCVD SiN_x MISHEMTs

Figs. 3 and 4 compare the dc characteristics of the LPCVD SiN_x/AlGaN/GaN MISHEMTs with and without PECVD SiN_x passivation. The double-mode transfer characteristics with a forward and reverse sweep between −20 and 5 V are shown in Fig. 3. For the unpassivated MISHEMT, significant peak transconductance and drain current degradation were observed during the forward sweep, suggesting severe

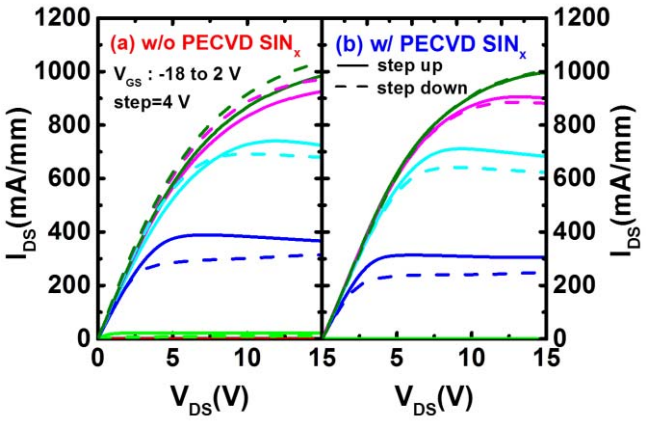

Fig. 4. DC output characteristics of LPCVD SiN_x/AlGaN/GaN MISHEMTs with and without PECVD SiN_x passivation. The drain bias was swept from 0 to 15 V, while the gate voltage was stepped up (solid lines) and down (dash lines).

current collapse. In contrast, the double-mode transfer curves for the passivated MISHEMT exhibited negligible discrepancies under the double-mode sweep conditions, indicating the suppression of trap-induced current collapse by passivation. Fig. 4 plots the output curves measured with the gate bias stepping up and down. In the MISHEMT without passivation, the drain current density is obviously lower at high gate bias ($V_{GS} = 2$ and -2 V) when the gate bias is stepped up from -18 to 2 V. In the linear region of the output curves, the passivated device exhibited smaller dispersion between the step-up and the step-down measurements when compared to the unpassivated device.

When comparing Figs. 3(b) and 4(b), it can be seen that the double-mode output characteristics for the passivated device show more obvious discrepancy ($V_{GS} = -6$ and -10 V) than that in the transfer curves. This could be attributed to the trapping effects in the device gate region [26]. In our experiments, the output measurements last much longer than the transfer measurements, resulting in a longer gate stress time and more serious trapping in the device.

B. C-V Measurements of LPCVD SiN_x MIS Diodes

The LPCVD SiN_x/AlGaN/GaN MIS diodes showed an extremely low gate leakage current of about 10^{-8} A/cm^2 at $V_{GS} = -20$ and 10 V, implying the high quality of the LPCVD SiN_x film. Double-mode $C-V$ measurements with a frequency of 100 kHz were carried out on both the MIS diodes with and without passivation. For both the samples, the obtained $C - V$ curves had two rising slopes, which is the characteristic feature of MIS heterostructures with a high-quality dielectric/III–nitride interface [15], [27].

As shown in Fig. 5, both MIS diodes exhibited a large clockwise hysteresis and threshold voltage shift (ΔV_{TH}). Such hysteresis can be attributed to acceptor-like traps located within the gate dielectrics or at the dielectric/III–nitride interface with a relatively long emission time constant [10], [27]. This kind of "slow" trap captures electrons during the forward sweep and cannot emit electrons during the reverse sweep due to the long emission time constant, resulting in the positive

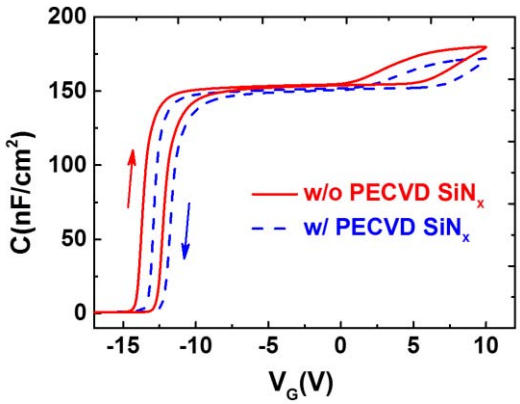

Fig. 5. Capacitance measurements for the LPCVD SiN_x/AlGaN/GaN MIS diodes with and without PECVD SiN_x passivation.

threshold voltage shift. In this paper, the ΔV_{TH} values of the passivated and unpassivated MIS diodes are similar to each other, suggesting that the passivation has less influence on these "slow" traps when located beneath the device's metal gate.

Previous studies have suggested that the typical $C - V$ curves of the GaN-based MIS diodes with ALD Al_2O_3 as gate dielectric includes a steep step with a negligible hysteresis and a less steep one with a large hysteresis [27], [28], which were different from the results in this paper using LPCVD SiN_x gate dielectric. However, large hysteresis for both rising slopes was observed in the $C-V$ curves of MIS diodes with PECVD SiN_x gate dielectric reported in [29]. This suggests that the $C - V$ hysteresis behavior probably depends on the gate dielectric material. On the other hand, the gate bias with an extremely wide range from -20 to 10 V in this paper probably further aggravated the threshold voltage instability.

III. Interface Trap Characterization

In order to evaluate the interface traps, pulse-mode $I - V$ measurements and the frequency-dependent conductance method were performed on the LPCVD SiN_x/AlGaN/GaN MISHEMTs and MIS diodes, respectively. We associated the trap analyses in actual MISHEMTs and MIS diodes to investigate the locations of interface traps and their influence on the electrical properties of the devices.

A. Pulse-Mode I_{DS}–V_{GS} Measurements

Pulse-mode $I_{DS} - V_{GS}$ measurements have been used for interface trap analysis in GaN-based MISHEMTs in previous works [15], [30]. In this paper, a similar method was used on LPCVD SiN_x/AlGaN/GaN MISHEMTs with various device dimensions: $L_G/L_{GS}/L_{GD}/W_G = 2/2/12/10$ μm and 2/1/1/10 μm. It should be noted that the devices have the same gate length but different access regions.

Fig. 6 shows the pulse-mode hysteresis characteristics of the unpassivated and passivated MISHEMTs with $L_G/L_{GS}/L_{GD}/W_G = 2/2/12/10$ μm. The pulsewidth W_p and the pulse period P_p are 5 μs and 100 ms, respectively. V_{DS} was kept at a low value of 1 V, in order to maintain a nearly uniform occupancy of the interface traps in the gate

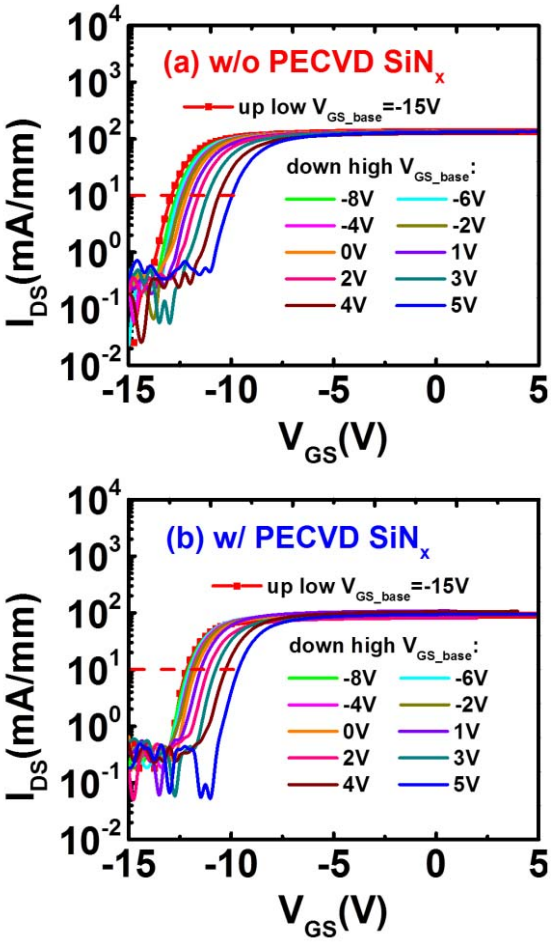

Fig. 6. Pulse-mode I_{DS}-V_{GS} characteristics of the (a) unpassivated and (b) passivated LPCVD SiN_x/AlGaN/GaN MISHEMT with ($L_G L_{GS} L_{GD} W_G$) = (2 2 12 10) μm. The pulsewidth and pulse period are 5 μs and 100 ms, respectively.

region and reduce the field-assisted detrapping [30]. In an ideal hysteresis characterization, the interface traps (acceptor-like) are supposed to be empty during the up sweep and to be filled with electrons during the down sweep [30]. The up-sweep pulsed $I_{\rm DS}-V_{\rm GS}$ curve in Fig. 6 with a low V_{GS_base} of -15 V is regarded as a baseline with minimal electron trapping in the interface traps. In the down sweep with a high V_{GS_base}, interface traps below the Fermi level with emission time constants longer than the pulsewidth would remain filled with electrons, leading to a positive shift of $V_{\rm TH}$. In contrast, interface traps with emission time constants shorter than the pulsewidth would emit electrons before each measurement point and thus could not be detected using this method [15], [30].

The interface trap state density $D_{\rm it}$ can be determined by

$$D_{\rm it} = \frac{C_{\rm OX} \cdot \Delta V_{TH}}{q^2} \tag{1}$$

where $C_{\rm OX} = 192$ nF/cm^2.

The emission time is assumed to limit the capture-emission process, since trap emission is normally much slower than trap capture. If the interface trap has an emission time constant longer than the period of the effective test signal (i.e., W_P), the trap is defined as a "slow" trap [10], [12]. The interface traps characterized using pulsed $I_{\rm DS}-V_{\rm GS}$ measurements are designated as "slow" traps if they have emission time constants longer than 5 μs in this paper. The detectable energy range can be deduced from Shockley–Read–Hall statistics

$$\tau = \frac{1}{v_{\rm th}\sigma_n N_c} \exp\left(\frac{E_C - E_T}{kT}\right) \tag{2}$$

where v_{th}, σ_n, and N_C are the electron thermal velocity, electron capture cross section and electron concentration at the effective density of states in the conduction band in GaN, respectively, [15], [27]. In this paper, the detectable energy range was calculated to be $E_C - E_T \geq 0.38$ eV. To detecting shallower interface traps, smaller pulsewidth needs to be adopted in the pulse-mode $I-V$ method.

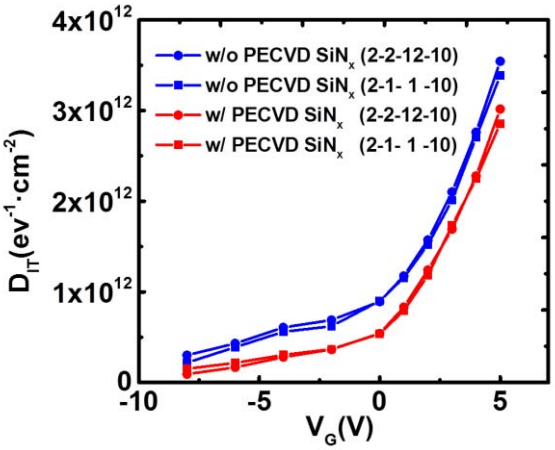

Fig. 7. Interface trap state density extracted from the pulse-mode I_{DS}-V_{GS} measurements for the MISHEMTs with and without passivation.

It should be noted that the pulse-mode $I-V$ method cannot distinguish $D_{\rm it}$ as a function of E_T [30]. Fig. 7 plots $D_{\rm it}$ versus V_G extracted from the pulsed $I_{\rm DS}-V_{\rm GS}$ measurements for the MISHEMTs with various device dimensions. The $D_{\rm it}$ of the MISHEMTs with different access regions but the same gate length showed very little discrepancy for both the passivated and unpassivated devices, suggesting that the interface traps characterized by the pulsed $I_{DS}-V_{GS}$ measurements were mainly located under the device gate. Also, the difference between $D_{\rm it}$ in the MISHEMTs with and without PECVD SiN_x passivation was small, indicating that the PECVD SiN_x passivation layer had less influence on the "slow" traps that were located in the MISHEMTs' gate region. This is in agreement with the results obtained from the $C-V$ measurements in the MIS diodes.

B. Frequency Dependent Conductance Method

The frequency dependent conductance method, based on measuring the equivalent parallel conductance (G_P) of an MIS capacitor as a function of gate bias and frequency, is one of the most sensitive methods to determine $D_{\rm it}$ [12]. The conductance represents the loss mechanism due to the capture and emission of electrons by interface traps, and thus can be used for $D_{\rm it}$ mapping [12].

Fig. 8(a) shows the small-signal equivalent circuit of an MIS capacitor appropriate to the frequency dependent

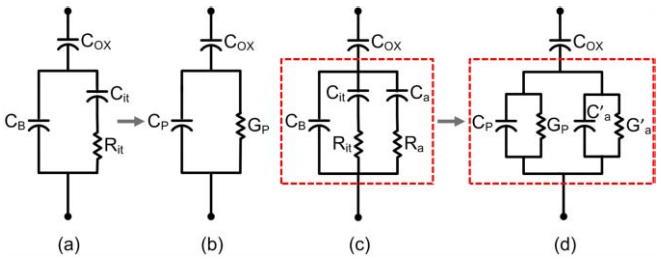

Fig. 8. Small-signal equivalent circuits for conductance measurements; (a) MIS capacitor with interface trap time constant $\tau_{it}=R_{it}C_{it}$, (b) Simplified circuit used in conductance-based D_{it} analysis, (c) including the impedance of traps in access region, and (d) equivalent parallel circuit model of (c).

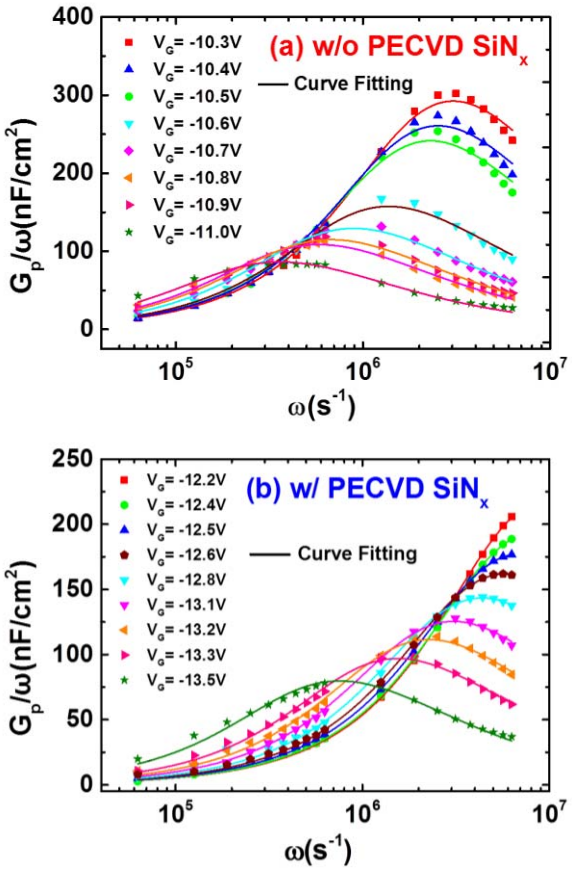

Fig. 9. Frequency dependent conductance as a function of radial frequency for the (a) unpassivated and (b) passivated MIS diode biased at selected gate voltage. The solid lines are fitting curves.

conductance method. The capacitance $C_{\rm it}$ and the resistance $R_{\rm it}$ represent the interface traps with a time constant of $\tau_{\rm it} = R_{\rm it}C_{\rm it}$. For convenience, the circuit is simplified into Fig. 8(b) with the parallel capacitance C_P and conductance G_P. Assuming a continuum of trap levels, G_P can be expressed as

$$\frac{G_p}{\omega} = \frac{qD_{\rm it}}{2\omega\tau_{\rm it}} \ln[1+(\omega\tau_{\rm it})^2] \tag{3}$$

where ω is the radial frequency and $\tau_{\rm it}$ is the trap time constant given by the Shockley-Read-Hall statistics [12], [31].

Fig. 9 shows the G_p/ω versus ω curves measured at selected gate biases for the unpassivated and passivated MIS diodes. $D_{\rm it}$ and their corresponding trap energy levels below the conduction band were extracted by fitting the experimental data using (3) and (1). The extracted $D_{\rm it}$ for the MIS diodes with and without PECVD SiN_x passivation are plotted in Fig. 10. The interface traps characterized by the conductance method exhibited short emission time constants in the range between 0.2 and 5 μs, and are classified as "fast" traps in this paper.

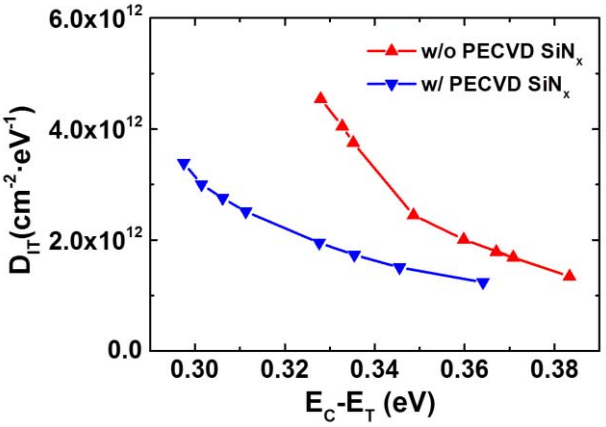

Fig. 10. Interface trap density as a function of the energy level depth below the conductance band for the MIS diodes with and without PECVD SiN_X passivation.

According to the small-signal equivalent circuit model of the conventional conductance method, the extracted $D_{\rm it}$ should be located under the MIS diode gate. Therefore, $D_{\rm it}$ value measured in the passivated and unpassivated devices should be closely similar to each other, since the passivation has little influence on the interface conditions under the MIS diode metal gate. However, it was found that the unpassivated device exhibited much higher $D_{\rm it}$, almost double when compared with that observed in the passivated device, which was in conflict with our expectation.

The result suggests that the passivation conditions for the access region in a GaN-based MISHEMT strongly affect the accuracy of $D_{\rm it}$ extraction using the conventional conductance method. Therefore, the influence of the access region should be considered and proper passivation for the access region is essential when using the conductance method to analyze the interface traps in AlGaN/GaN MISHEMTs.

A modified MIS diode equivalent circuit that considers the influence of access region traps is proposed, as shown in Fig. 8(c). C_a and R_a represent the series impedance of the traps in the access region, which can be replaced by the parallel conductance G'_a and capacitance C'_a. Similar to Fig. 8(a) and (b), the capacitance C_B, $C_{\rm it}$ and the resistance $R_{\rm it}$ can be replaced with the parallel conductance G_P and capacitance C_P. Fig. 8(d) shows the simplified equivalent parallel circuit model of Fig. 8(c). The total measured parallel conductance in this circuit is given by

$$\frac{G'_P}{\omega} = \frac{G_P}{\omega} + \frac{G'_a}{\omega} \tag{4}$$

where G_P is the parallel conductance that represents the real interface traps under gate, G'_a is the extra conductance related to the influence of the traps states in access region.

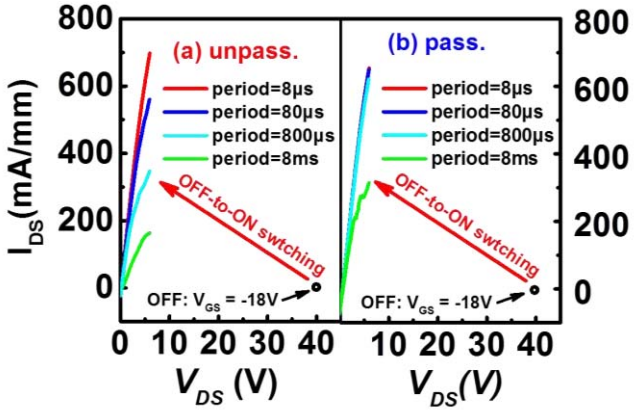

Fig. 11. Transient OFF-to-ON switching measurements under various stress periods from 8 μs to 8 ms. The applied pulsewidth is 0.8 μs. The MISHEMTs with and without passivation were switched from the off state with a quiescent bias of (V_{GSQ}, V_{DSQ}) = $(-18, 40\ V)$ to the ON state with a gate bias of 2 V.

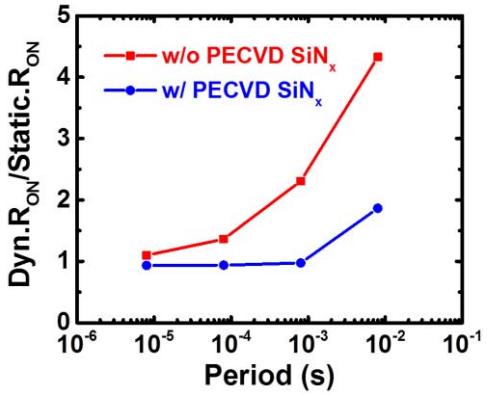

Fig. 12. Dynamic R_{ON} under various pulse periods extracted from Fig. 11.

According to (3), G_p/ω has a maximum and at that maximum $D_{it} = 2.5G_p/q\omega$. D_{it} extracted from the measured parallel conductance G'_p/ω (note $G'_p/\omega > G_p/\omega$) using conventional conductance method will be overestimated due to the existence of G'_a if the device is not properly passivated.

The modified small-signal equivalent circuit is still far from a perfect model to fully explain the influence of the access region on trapping analysis using the conductance method. As shown in Fig. 9, the maximum G_p/ω for the devices with and without passivation are not located at the same redial frequency, indicating the complexity of the situation. Nevertheless, this paper provides a concise and qualitative description of the issue.

On the other hand, D_{it} discrepancies between the samples with and without passivation reduced as the trap energy levels (E_C -E_T) increased, as shown in Fig. 10, indicating that proper passivation can effectively restrain the relatively shallow traps but has less influence on the relatively deep traps in the access region.

In brief, the combination of "slow" traps ($\tau_{it} > 5\ \mu$s) obtained using pulsed $I_{DS} - V_{GS}$ measurements and "fast" traps ($0.2\ \mu s < \tau_{it} < 5\mu$s) characterized by the frequency dependent conductance method gives a comprehensive indication of where these traps are located and how they are influenced by passivation.

IV. Trap Related Current Collapse Analysis

To further investigate the influence of interface traps on device performance, transient OFF-to-ON switching measurements were performed on the LPCVD SiN_x/AlGaN/GaN MISHEMTs with and without PECVD SiN_x passivation.

Fig. 11 shows the transient OFF-to-ON switching tests under various stress periods from 8 μs to 8 ms. The MISHEMTs were switched from the OFF state with a quiescent bias of (V_{GSQ}, V_{DSQ}) = (−18, 40 V) to the ON state with a gate bias of 2 V. The pulsed output curves of the unpassivated MISHEMT exhibited significantly higher dispersion than those of the passivated device. As shown in Fig. 12, dynamic R_{ON} was extracted from the linear regime (V_{DS}: 0 to 6 V) of the pulsed output curve. The passivated MISHEMT exhibited much lower dynamic R_{ON} degradation even with a stress period of 8 ms. In pulse measurements with a high V_{DSQ}, tunneled gate electrons become trapped by interface traps in the extrinsic gate–drain access region due to the high electric field, which depletes the 2-DEG in the access region, resulting in the dynamic R_{ON} degradation in the unpassivated device [20], [22], [32]. More electrons will then be trapped with the increasing stress period, and cannot respond to the test signal, further deteriorating the device dynamic performance.

For the PECVD SiN_x passivated MISHEMT, the alleviated current collapse can be attributed to the suppression of shallow traps by passivation, while the steep increase of dynamic R_{ON} with a pulse period of 8 ms, as shown in Fig. 12, is related to deep traps located at the interface or AlGaN barrier [22], [32]. Due to the improved surface passivation, trapping by shallow traps is restrained to a great extent, and thus, the trapping of electrons by deep traps becomes the most prominent mechanism. This, in turn, verifies that the passivation in this paper can effectively restrain the "fast" traps with a relatively shallow energy level (shallow traps) located at the access region but has less influence on the "slow" traps with a relatively deep energy level (deep traps).

V. Conclusion

We performed a comprehensive investigation of the interface traps in LPCVD SiN_x/AlGaN/GaN MISHEMTs by combining pulse-mode $I - V$ measurements performed on MISHEMTs with various device dimensions and the frequency dependent conductance method implemented on MIS diodes. Two types of interface traps with different emission time constants, designated as "slow" (deep) and "fast" (shallow) traps, were identified and characterized. Interface traps under the device metal gate mostly result in ΔV_{TH}, while interface traps in the gate–drain access region can contribute to current collapse by trapping electrons that have tunneled from the gate. By comparing the devices with and without PECVD SiN_x passivation, we found that the passivation can effectively restrain the shallow traps in the access region, but has less influence on the deep traps both in the access region and under the metal gate. Thus, the PECVD SiN_x passivation may not be able to fully eliminate current collapse due to the existence of deep traps located at the interface or in the AlGaN barrier or buffer, as verified by transient OFF-to-ON switching tests.

Moreover, a modified small-signal equivalent circuit that considers the influence of the access region has been proposed to explain the overestimation of D_{it} characterized using the conventional frequency dependent conductance method. To accurately extract the interface trap state density in GaN-based MIS heterostructures using the conductance method, proper passivation for the access region is essential.

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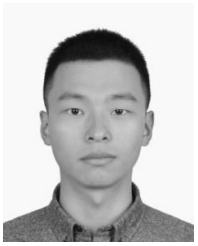

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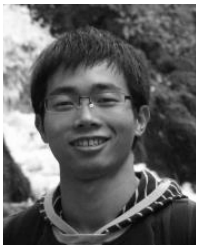

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