Investigation of *In Situ* SiN as Gate Dielectric and Surface Passivation for GaN MISHEMTs

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***Abstract*— In this paper, we present a systematic investigation of metal–organic chemical vapor deposition-grown *in situ* SiN as the gate dielectric and surface passivation for AlGaN/GaN metal insulator semiconductor high electron mobility transistors (MISHEMTs). The dielectric constant and breakdown field of the *in situ* SiN were extracted from devices with varied gate dielectric thicknesses. Using frequency-dependent capacitance–voltage and parallel conductance methods, we obtained a low trap density of $\sim 3 \times 10^{12}$ cm^{-2}eV^{-1} at the SiN/AlGaN interface. The MISHEMTs with a source–drain distance of 3 μm show a maximum drain current of 1560 mA/mm and a high on/off current ratio of 10^9. The device threshold voltage (V_{th}) stability was assessed by means of both negative and positive gate stress measurements, as well as temperature-dependent I_D–V_G measurements. We observed a minimal V_{th} shift of ~0.4 V under both 3000 s gate stress of V_{GS} = 4 V and up to 200 °C thermal stimulation. Furthermore, combining the *in situ* SiN with plasma-enhanced chemical vapor deposition SiN, we developed a bilayer passivation scheme for effective suppression of current collapse. Employing the high-quality *in situ* SiN, we have demonstrated large-area GaN MISHEMTs on Si with a gate width of 20 mm, showing a low off-state leakage of 2 μA/mm at 600 V and a low dynamic/static ON-resistance ratio. The device results show great advantages of employing *in situ* SiN in D-mode GaN MISHEMTs for high-efficiency power switching applications.**

***Index Terms*— GaN, gate dielectric, *in situ* SiN, passivation, thermal stability, threshold voltage.**

I. Introduction

GaN-BASED metal insulator semiconductor high electron mobility transistors (MISHEMTs) have demonstrated excellent performance for high-efficiency power switching applications[1]–[3]. Despite the fact that the use of a gate dielectric in MISHEMTs can significantly suppress gate leakage current and enlarge gate swing, the device performance strongly relies on the bulk properties of the gate dielectric and the dielectric/III-nitride interface quality. So far, atomic layer deposition (ALD) and low pressure chemical vapor deposition (LPCVD) have been the two common means to form high-quality gate dielectrics, such as Al_2O_3 and SiN, for GaN transistors [4]–[8]. However, high-density interface trap states in the order of $\sim 10^{13}$–10^{14} cm^{-2}eV^{-1} are usually present at the dielectric/barrier interface [8]–[10]. Compared with these *ex situ* deposited dielectrics, an *in situ* SiN gate dielectric can be epitaxially grown immediately after the GaN HEMT barrier growth in a metal-organic chemical vapor deposition (MOCVD) system [11]–[13]. Without the expose of the as-grown GaN HEMT barrier to the ambient air, the process-induced contamination or damage can be prevented. Moreover, the low growth rate and high growth temperature of *in situ* SiN are favorable for good dielectric quality. Benefiting from these advantages, excellent device results have been demonstrated utilizing *in situ* SiN as gate dielectrics in recent literature [14]–[16].

Nevertheless, as reported by our group previously, the *in situ* SiN/III-nitride interface quality is sensitive to growth conditions, e.g., temperature, pressure, and partial pressure of precursors [13]. Most of the previous works have mainly focused on the overall device performance using structures incorporating *in situ* SiN gate dielectric. Probing the functionality and effectiveness of the *in situ* SiN dielectric layer is of great importance, but has been less studied.

In this paper, we present a systematic investigation of *in situ* SiN as both the gate dielectric and surface passivation for AlGaN/GaN MISHEMTs. The dielectric properties in terms of dielectric constant and breakdown field are described first, followed by the characterization of *in situ* SiN/AlGaN interface quality. Furthermore, the performance of *in situ* SiN as a gate dielectric and a passivation layer was evaluated separately. Concerning the gate dielectric, the gate controllability over the channel and the threshold voltage stability were analyzed in detail by means of basic dc characterization, electrical stress, and temperature-dependent characterization. Regarding effective surface passivation, we found that a bilayer passivation scheme combining *in situ* SiN and plasma-enhanced chemical vapor deposition (PECVD) SiN was desirable. Finally, high-performance GaN power devices on Si with a 20-mm gate

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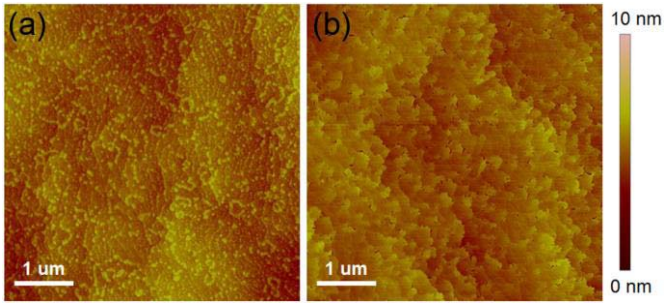

Fig. 1. AFM image of as-grown GaN HEMT sample (a) with and (b) without an *in situ* SiN cap.

width were demonstrated, proving the benefits of using *in situ* SiN as gate and passivation dielectrics for large-area GaN MISHEMTs.

II. Heterostructure Design and Device Fabrication

In situ SiN/AlGaN/GaN heterostructures were grown on 2-in sapphire substrates by MOCVD. The epilayers, from bottom to top, consist of a 3-μm GaN buffer, a 100-nm unintentionally doped GaN channel layer, a 1-nm AlN spacer, a 20-nm $Al_{0.3}Ga_{0.7}N$ barrier, and a thin *in situ* SiN cap. The *in situ* SiN was grown at a reactor temperature of 1125 °C, using silane and ammonia as precursors. To evaluate the material properties of the *in situ* SiN rigorously, four samples were grown with a SiN cap of different thicknesses, varying from 7 to 28 nm with a 7-nm step. For the electrical characterization of the *in situ* SiN/AlGaN/GaN heterostructures, MISHEMTs and circular-shaped MIS capacitors (MISCAPs) were fabricated. The device fabrication started with source/drain metallization using a Ti/Al/Ni/Au-based metal stack, with the SiN etched away in the contact region. Device isolation was performed using Ar implantation. Following that, a Ni/Au-based metal stack was deposited to form the gate. Finally, a 100-nm PECVD SiN layer was deposited for device passivation. The average ohmic contact resistance was determined to be 0.5 Ω-mm, and the sheet resistance of 2-DEG was ~400 Ω/sq as measured by the transfer length method (TLM) after the PECVD SiN passivation. For comparison, a GaN HEMT sample without an *in situ* SiN cap was grown and fabricated as a reference. Fig. 1 compares the atomic force microscopy (AFM) images of as-grown GaN HEMT samples with and without a 14-nm *in situ* SiN cap. Though the surface morphologies of the two samples are quite different (terraces can only be clearly observed in the HEMT sample), the root-mean-square (rms) roughness values across a 5-μm × 5-μm scanned area are quite close, 0.64 and 0.51 nm for samples with and without an *in situ* SiN cap, respectively. The small rms value of the sample with an *in situ* SiN cap suggests smooth surface morphology and uniform coverage of SiN on the AlGaN barrier. Therefore, the *in situ* SiN deposition will not degrade the surface morphology of GaN HEMT.

III. Device Results and Discussion

After the device fabrication, the current–voltage characterization was performed using an Agilent 4156C semiconductor parameter analyzer, and the capacitance–voltage (C–V) characterization was carried out using an Agilent E4980A precision *LCR* meter.

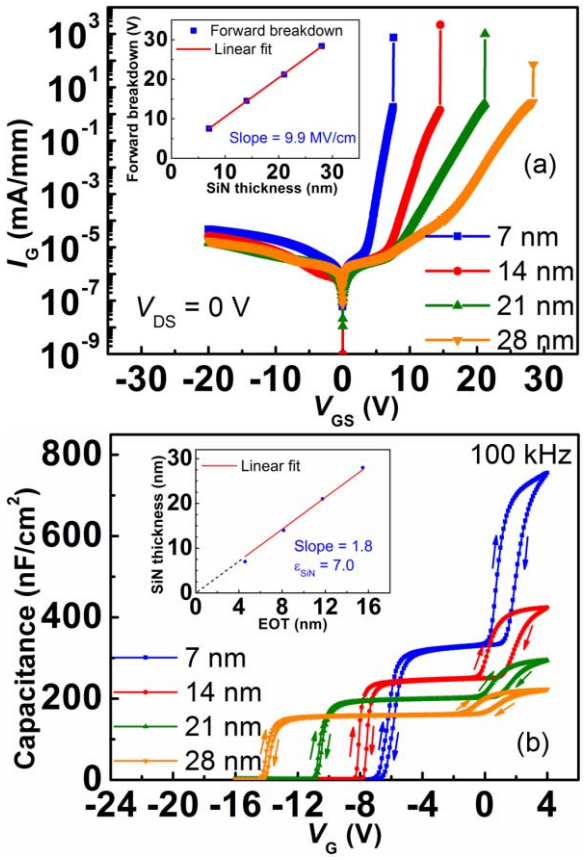

Fig. 2. (a) Forward and reverse gate leakage of GaN MISHEMTs and (b) double sweep C–V characteristics of circular MISCAPs with various *in situ* SiN thicknesses. Inset in (a): forward gate breakdown voltage dependence on the SiN thickness. Inset in (b): *in situ* SiN thickness versus the corresponding EOT.

A. Dielectric Properties of in situ SiN

Fig. 2(a) shows the gate leakage under both reverse and forward gate biases for MISHEMTs with different thicknesses of SiN gate dielectric. The source and drain electrodes were both grounded during the measurement. The difference in the reverse gate leakage current for the four samples is minimal. Devices with a thicker gate dielectric show a slightly lower leakage current, while the forward gate leakage current increases exponentially with the gate voltage. The gate forward breakdown voltage is nearly linearly dependent on the *in situ* SiN thickness, as shown in the inset of Fig. 2(a). The dielectric electric field strength extracted from linear fitting is ~9.9 MV/cm. Fig. 2(b) shows double sweep *C–V* curves at 100 kHz measured on circular MISCAPs with a diameter of 200 μm. All *C–V* curves exhibit two rising steps. The gate voltage at the first rising step corresponds to the pinchoff/threshold voltage for the 2-DEG channel, and the second rising step corresponds to the spill-over of electrons from the 2-DEG channel to the barrier surface, also known as barrier accumulation. Therefore, the maximum capacitance of

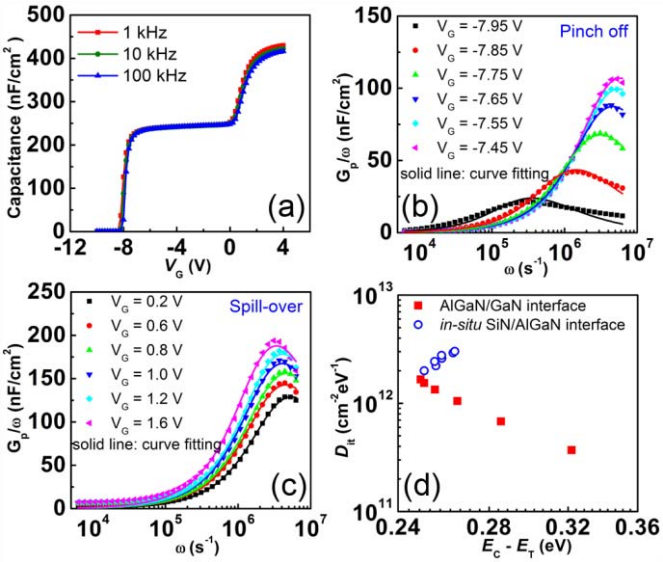

Fig. 3. Frequency-dependent (a) C–V characteristics, parallel conductance as a function of radial frequency at selected voltages near (b) pinch off and (c) onset of barrier accumulation. (d) Extracted interface trap density with corresponding trap energy level below the conduction band.

the second step is the capacitance of the *in situ* SiN itself. The threshold voltage shifts in the negative direction with the increase of the *in situ* SiN thickness, due to weakened gate control over the 2-DEG channel farther away from the gate electrode. Converting the *in situ* SiN capacitance into corresponding equivalent oxide (SiO_2) thickness (EOT), the relative dielectric constant of the *in situ* SiN is extracted to be ~7.0, 1.8 times that of SiO_2, as shown in the inset of Fig. 2(b). On the other hand, the double sweep C–V curves for all MISCAPs show a relatively large hysteresis (1–1.5 V) at the barrier accumulation region, and also a small hysteresis (0.1–0.4 V) at the pinchoff region. The hysteresis at pinchoff is affected by the one at barrier accumulation. We have not observed a clear dependence of hysteresis on the *in situ* SiN thickness in this paper. The hysteresis in the C–V curves may be related to deep traps with long time constants (several seconds or above) at/near the *in situ* SiN/AlGaN interface.

B. Interface Trap Characterization

The electrical characteristics of a representative device with a 14-nm *in situ* SiN gate dielectric are presented in the remainder of this paper, unless otherwise stated. The interface quality of the *in situ* SiN/AlGaN/GaN heterostructure was evaluated by the frequency-dependent C–V measurement on the circular MISCAPs.

Fig. 3(a) shows the C–V curves under various frequencies from 1 to 100 kHz. Negligible frequency dispersion and sharp transition slopes can be observed, suggesting a low interface trap density in the gate-stack. To quantitatively analyze the interface trap density and distribution, the typical frequency-dependent parallel conductance technique was applied with the measurement frequency ranging from 1 kHz to 1 MHz at room temperature [17], [18]. Fig. 3(b) and (c) shows the parallel conductance (G_p/ω) versus radial frequency (ω) for

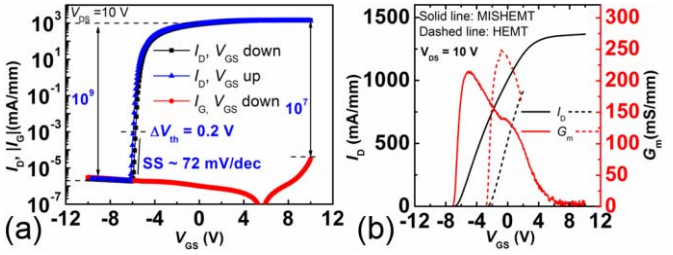

Fig. 4. (a) Semilog plot of typical double sweep transfer characteristics of GaN MISHEMTs. (b) Comparison of transfer characteristics and transconductance of GaN MISHEMTs and HEMTs.

selected gate voltages near the threshold voltage and onset voltage of the barrier accumulation of the MISCAPs. The trap density (D_{it}) and the time constant can be extracted by fitting the experimental $G_p(\omega)$ data. The trap energy level below the GaN conduction band, designated as E_C–E_T, can be deduced from the trap time constant based on the Shockley–Read–Hall statistical model. Assuming the effective density of states in the GaN conduction band to be 2.2×10^{18} cm^{-3}, the average thermal velocity of electrons to be 2×10^7 cm/s, and the trap states capture cross section to be 1×10^{-15} cm^2 [17], [19], the D_{it} as a function of energy level (E_C–E_T) is plotted in Fig. 3(d). D_{it} at the AlGaN/GaN heterointerface ranges from 3.7×10^{11} to 1.5×10^{12} $cm^{-2}eV^{-1}$, with energy levels spanning from 0.25 to 0.32 eV below the conduction band, and D_{it} at the *in situ* SiN/AlGaN interface is in the range of $(2–3) \times 10^{12}$ $cm^{-2}eV^{-1}$ with an energy level spanning from 0.25 to 0.27 eV below the conduction band. D_{it} is almost one order of magnitude lower than that of the MISHEMTs using an LPCVD SiN and ALD Al_2O_3 gate dielectric [8], [10]. MISHEMTs using ALD Al_2O_3 gate dielectric with comparable performance needs complicated surface treatments [20]. The results here suggest that superior interface quality in the gate-stack of GaN MISHEMTs can be obtained using an *in situ* SiN gate dielectric.

C. Enhanced Carrier Transport

DC characterization of GaN MISHEMTs and HEMTs was carried out on the devices with a gate width W_G of 10 μm, a gate length L_G of 1 μm, and both a gate–source distance L_{GS} and gate–drain distance L_{GD} of 1 μm. Fig. 4(a) shows a semilog plot of typical double sweep transfer characteristics of GaN MISHEMTs with an *in situ* SiN gate dielectric at a V_{DS} of 10 V. The device shows a high ON/OFF current ratio of ~10^9 and a steep subthreshold slope of 72 mV/decade, as well as a small hysteresis of 0.2 V. Moreover, the drain-current-to-gate-current ratio in the MISHEMT remains more than 10^7 at a V_{GS} of 10 V, indicating the excellent leakage blocking capability of the *in situ* SiN. Fig. 4(b) compares the transfer characteristics of GaN MISHEMTs and HEMTs. There is only a slight decrease of the peak transconductance in the MISHEMTs (250 mS/mm for HEMTs and 220 mS/mm for MISHEMTs), but a large increase in the linearity range and the gate swing, indicating more efficient gate control over the channel. Fig. 5(a) compares the output characteristics of GaN MISHEMTs and HEMTs. The MISHEMT showed well-behaved I_D–V_{DS} characteristics with a maximum drain

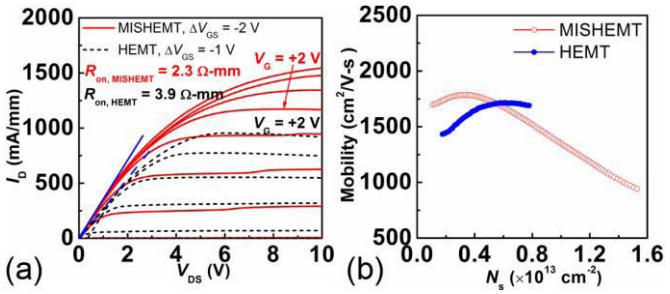

Fig. 5. (a) Output characteristics comparison of GaN MISHEMTs and HEMTs. (b) Extracted drift mobility of GaN MISHEMTs and HEMTs as a function of carrier concentration.

current ($I_{DS,max}$) as high as 1560 mA/mm at a V_{GS} of 8 V. An ON-resistance (R_{ON}) extracted in the linear region is 2.3 Ω-mm, for a source–drain distance of 3 μm. The high $I_{DS,max}$ and low R_{ON} are among the best results ever reported for AlGaN/GaN MISHEMTs with similar dimensions. Whereas for the HEMT, $I_{DS,max}$ and R_{ON} is ~900 mA/mm and 3.9 Ω-mm, respectively, at V_{GS} of 2 V, where the gate leakage has already been excessively high. The enhanced carrier transport in MISHEMTs is mainly attributed to the increase of carrier concentration (N_s) under greatly enlarged gate overdrive voltage as well as the high carrier mobility with low Coulomb scattering impact from the traps at the *in situ* SiN/AlGaN interface.

The drift mobility (μ_d) of carriers within the 2-DEG channel in MISHEMTs and HEMTs was quantitatively characterized using a split C–V method [21], [22], on a FATFET with a gate dimension of W_G/L_G = 200/100 μm. The drift mobility can be extracted according to the equation

$$\mu_d = \left(\frac{L_G}{W_G}\right)\left(\frac{G_{ch}}{qN_s}\right) \tag{1}$$

where G_{ch} is the channel conductance at a low drain bias of 0.1 V. The N_s was extracted from the integration of respective C–V curves of the FATFET using the equation

$$N_s = \frac{1}{qA}\int_{V_{th}}^{V_G} C(V_G)dV_G \tag{2}$$

where A is the gate metal area of FATFET. Fig. 5(b) shows the extracted drift mobility for MISHEMTs and HEMTs as a function of effective N_s in the channel. For MISHEMTs, the μ_d increases with smaller N_s and reaches a peak value of 1780 cm^2/V-s at N_s of 3.5 × 10^{12} cm^{-2}. While decreasing with higher N_s, μ_d is still over 1500 cm^2/V-s at a high N_s of 8 × 10^{12} cm^{-2}. While for the HEMT, due to the relatively high gate leakage under forward gate bias, the mobility can only be extracted with a maximum carrier concentration of ~8 ×10^{12} cm^{-2}. The extracted carrier mobility of MISHEMTs is larger than that of HEMTs when N_s is below 6 × 10^{12} cm^{-2}.

D. Threshold Voltage Stability

It has been reported that state-of-the-art MISHEMTs still suffer from threshold voltage drift effects induced by forward and reverse gate biases, or temperature increase [23]–[26],

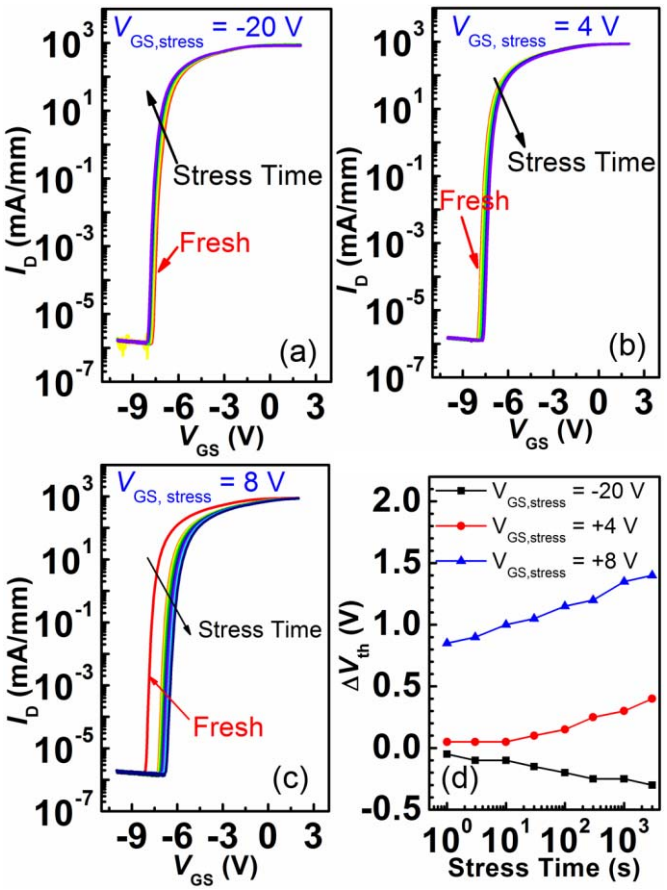

Fig. 6. (a) I_D–V_{GS} curves measured during the 3000 s. (a) Reverse gate bias stress (V_{GS} = − 20 V). (b) Forward gate bias stress of V_{GS} = 4 V. (c) Forward gate bias stress of V_{GS} = 8 V. (d) Threshold voltage shift ($\Delta V_{th} = V_{th,stress} - V_{th,0}$) during the stress in (a)–(c).

influencing the stability and reliability of these devices in operation. To assess V_{th} stability in the MISHEMTs with an *in situ* SiN gate dielectric, both the gate stress and the thermal stimulation are applied to the devices and the change in threshold voltage was monitored. The measurements were carried out on the devices with dimensions of L_G/W_G = 2/10 μm, and L_{GS}/L_{GD} = 2/12 μm.

For the gate stress measurement, the stress is applied only to the gate terminal at room temperature, with both drain and source grounded. In this way, V_{th} shift will mainly be attributed to the trapping process occurring in the dielectric and the dielectric/barrier interface. A stress of V_{GS} = −20, 4, and 8 V was used to evaluate the negative and positive bias-induced threshold voltage instability, respectively. The total stress time was fixed at 3000 s. V_{th} shift was monitored by a fast I_D–V_{GS} measurement (−10 V < V_{GS} < 2 V and V_{DS} = 10 V) after certain stress time intervals T_S (1, 3, 10, 30, 100, 300, 1000, and 3000 s). V_{th} is determined at an I_D of 1 μA/mm. The I_D–V_{GS} characteristics are well behaved under reverse gate stress [−20 V, Fig. 6(a)] and small forward gate stress [+4 V, Fig. 6(b)]. However, much larger shift of I_D–V_{GS} curves has been observed under relatively large forward gate stress [+8 V, Fig. 6(c)]. A negative V_{th} shift increases with the stress time under reverse gate bias, and

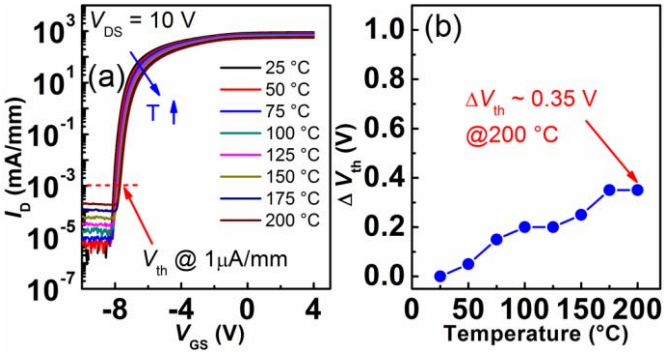

Fig. 7. Temperature-dependent (a) transfer characteristics and (b) threshold voltage shift ($\Delta V_{th} = V_{th,T} - V_{th,25\,°C}$) of the *in situ* SiN/AlGaN/GaN MISHEMTs with measurement temperature increasing from 25 °C to 200 °C.

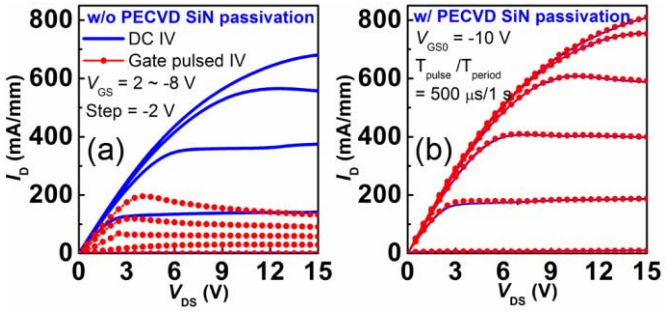

Fig. 8. Comparison of dc and gate pulsed output characteristics of GaN MISHEMTs with the *in situ* SiN gate dielectric (a) before and (b) after PECVD SiN passivation.

the same trend exists for the forward gate bias. V_{th} shift is −0.3 V and +0.4 V under −20 V and +4 V stress for 3000 s, respectively, as shown in Fig. 6(d). However, V_{th} shift is as large as 1.4 V for under +8 V stress for 3000 s, and takes nearly half an hour to recover. The result indicates that the bulk trapping of an *in situ* SiN is still very severe under large forward gate bias. Similar to the bulk trapping of plasma-enhanced ALD SiN gate dielectric in E-mode MISHEMT where large forward gate bias is necessary [24], [25], the *in situ* SiN still needs to be improved to alleviate the bulk trapping before they can work under high forward gate bias in the long term or be implemented in E-mode MISHEMTs as a gate dielectric. Nevertheless, the *in situ* SiN is suitable for D-mode MISHEMTs with benign forward gate bias operation [23].

The temperature dependent V_{th} shift is evaluated by submitting the MISHEMTs to thermal stimulation from room temperature (25 °C) to 200 °C with a 25 °C step. Fig. 7(a) shows the transfer characteristics at various temperatures. The OFF-state I_D at 200 °C is still as low as 10^{-4} mA/mm, resulting in a high ON/OFF current ratio of $\sim 10^7$. A small positive V_{th} shift is observed with the increase of measuring temperature. As shown in Fig. 7(b), the V_{th} shift is only 0.2 V at 100 °C and 0.35 V at 200 °C. These values are ~1 V less than that with the Al_2O_3 gate dielectric reported in [27]. It was previously suggested that the thick barrier is detrimental to the V_{th} thermal stability, and reducing the barrier thickness thus suppressing the trap states availability can be helpful to alleviate the thermally induced V_{th} shift [28]. Results here show that a high-quality dielectric/III-nitride interface and a high-quality dielectric bulk and barrier crystal with low trap density are more effective in maintaining excellent V_{th} thermal stability.

The minimal V_{th} shift characterized by both the gate bias stress with a mild forward voltage and thermal stimulation up to 200 °C is a strong evidence of the superior gate-stack performance when using *in situ* SiN gate dielectrics in D-mode GaN MISHEMTs. The *in situ* deposition method and high-temperature deposition condition of gate dielectrics can improve the device intrinsic immunity to adverse process effects, thus enhancing the operation stability and long-term reliability of the device without the need of changing the device design.

E. Passivation Effect

In addition to the gate-stack quality, the dynamic performance of GaN MISHEMTs is also vital to stable device operation. Although, excellent dynamic performance has been reported in devices using *in situ* SiN gate dielectrics, the passivation effect of single *in situ* SiN in GaN MISHEMTs is seldom discussed in detail. To evaluate the passivation effect of the *in situ* SiN gate dielectric only in GaN MISHEMTs, we compared the dc and gate pulsed output characteristics for the MISHEMTs both before and after the extra PECVD SiN passivation during the device fabrication. The devices are with dimensions of $L_G/W_G = 2/20$ μm and $L_{GS}/L_{GD} = 3/15$ μm. For the gate pulse measurement, the quiescent gate bias is $V_{GS0} = -10$ V, the pulse width is 500 μs, and the pulse period is 1 s. As shown in Fig. 8, the MISHEMTs with single *in situ* SiN passivation in the access region show a large dc and gate pulsed I–V dispersion, suggesting a serious virtual gate effect in the devices and the ineffectiveness of *in situ* SiN in the suppression of current collapse. This is consistent with the results reported by Huang *et al.* [29]. Possible reasons can be that the *in situ* SiN is not thick enough and the chemical composition of the *in situ* SiN in this paper is not in favor for eliminating shallow traps at the AlGaN surface [29]. In contrast, by combining additional PECVD SiN passivation, the current collapse in the MISHEMTs is dramatically mitigated, exhibiting negligible dc/pulsed I–V dispersion. Moreover, the devices still maintained a high ON/OFF current ratio of 10^9 after the PECVD SiN passivation, suggesting that the *in situ* SiN can serve as a robust interlayer to mitigate the PECVD SiN introduced surface leakage, which is commonly observed in the GaN HEMTs [30].

F. GaN Power MISHEMTs

After validating the *in situ* SiN as an excellent gate dielectric, we developed large-area *in situ* SiN/AlGaN/GaN power transistors with a maximum gate width of 20 mm. The heterostructures were grown on a 150-mm n-type Si (111) substrate. Large diameter Si wafers are beneficial to manufacture commercial GaN-based power devices, taking advantage

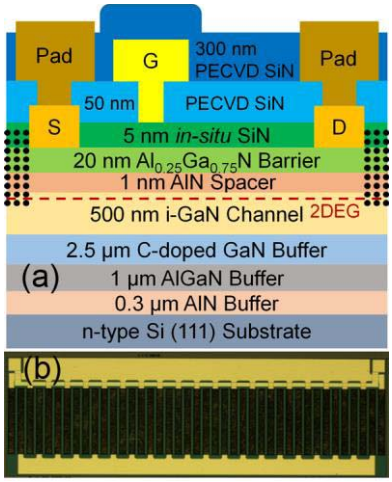

Fig. 9. (a) Cross-sectional schematic of GaN power MISHEMTs on Si. (b) Overview of the MISHEMTs with a gate width of 20 mm.

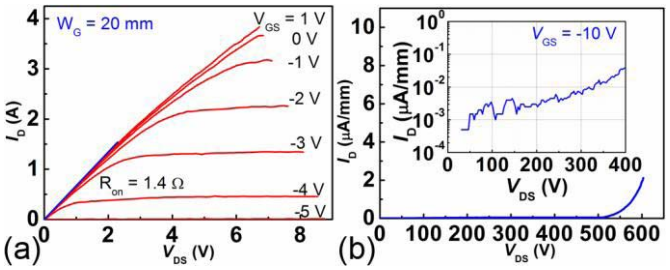

Fig. 10. (a) Output characteristics and (b) off-state leakage current of *in situ* SiN/AlGaN/GaN power MISHEMTs with a gate width of 20 mm. The substrate is floating during the off-state measurement.

of the mature Si platform and higher thermal conductivity. To maximize the device breakdown by reducing the peak electric field near the gate edge at the drain-side, a gate-connected field plate was employed in passivation-first process, similar to [31]. The cross-sectional large-area device structure reported here is schematically shown in Fig. 9(a). The device has a gate foot length of 2 μm, with a gate overhang of 2 μm on both the source and drain sides. L_{GS} and L_{GD} are 4 and 14 μm, respectively. A multifinger structure was adopted to reduce the gate resistance, with a gate finger width of 500 μm. The first PECVD SiN passivation layer under the gate head is 50 nm, and the second PECVD SiN passivation layer above the gate is 300 nm. The final power metal pad is 600 nm. Fig. 9(b) shows an overview of the device with a 20-mm gate width and the footprint of the device is 2.8 mm $\times$ 0.9 mm.

Fig. 10(a) shows the output characteristics of the GaN power MISHEMTs with a 20-mm gate width. The maximum I_{DS} under continuous dc power supply is 3.8 A at V_{GS} of 1 V, with a low ON-resistance of 1.4 Ω. The relatively low current density of ~190 mA/mm is probably due to the long and thin power metal bar of S/D contact, resulting in a large contact resistance and also due to the self-heating for devices under continuous power supply, which degrades the ON-resistance. Taking the full active area of the device into account along with the exclusion of the bonding pad area, the specific ON-resistance $R_{ON,sp}$ was calculated to be 5.6 mΩ-cm^2. Fig. 10(b) shows the OFF-state I_D under high-voltage drain bias, with a

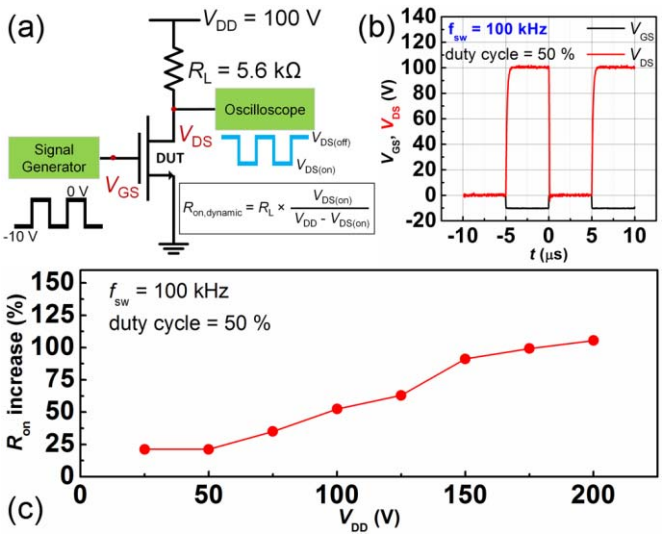

Fig. 11. (a) Schematic of resistive load hard switching test, V_{DD} = 100 V. (b) Switching waveforms of input gate signal and output drain voltage. The switching frequency is 100 kHz and the duty cycle is 50%. (c) Percentage increase of the dynamic R_{ON} over the static R_{ON} versus V_{DD}.

semilog plot in the inset. The substrate is floating during the OFF-state measurement. With a high-quality GaN buffer and the high leakage blocking capability of the *in situ* SiN, the OFF-state I_D is below 100 nA/mm at a V_{DS} of 400 V, and is as low as 2 μA/mm at 600 V. The OFF-state I_D mainly flows into the gate terminal. The OFF-state leakage may be further suppressed by increasing the gate dielectric thickness.

The dynamic performance of GaN power MISHEMTs was assessed by a resistive load hard switching test, as shown in Fig. 11(a). The device under test (DUT) has the dimensions of L_G/W_G = 2/200 μm and L_{GS}/L_{GD} = 4/24 μm. The supply voltage V_{DD} is 100 V (variable) and the load resistance is selected to be 5.6 kΩ to keep the device working in the linear region at ON-state. The DUT was switched at 100 kHz with a 50% duty cycle. The switching waveform of the input gate signal and the output drain voltage is shown in Fig. 11(b). The ON-state V_{DS} shows a flat envelope, suggesting a stable dynamic R_{ON}, which was extracted and found to be only 1.5 times of the static R_{ON}. The percentage increase of the dynamic R_{ON} over the static R_{ON} as a function of the V_{DD} (i.e., the OFF-state drain voltage) up to 200 V is shown in Fig. 11(c). The dynamic R_{ON} degraded slightly with the increase of OFF-state drain voltage. Nevertheless, the dynamic R_{ON} is double of the static value at 200 V under the hard switching test. The current collapse has been effectively suppressed by the *in situ* SiN and PECVD SiN bilayer passivation scheme.

IV. Conclusion

In this paper, the use of *in situ* MOCVD-grown SiN as the gate dielectric and passivation layer in AlGaN/GaN MISHEMTs has been systematically described and investigated. Besides offering a high-quality dielectric interface with the low trap density, the *in situ* SiN is found to be highly resistant to the electrical and thermal stress when serving as the gate dielectric in the MISHEMTs. Nevertheless, the *in situ* SiN in this paper has not been perfected and the V_{th} shift is

small only for benign forward gate bias (e.g., +4 V); therefore, the *in situ* SiN is currently an excellent gate dielectric only for D-mode MISHEMTs, which do not require excessively high forward gate overdrive. In the case of application in E-mode MISFETs, further reduction of bulk traps in the *in situ* SiN is needed. For surface passivation on GaN transistors, the *in situ* SiN alone is less effective than the PECVD SiN. Nevertheless, the *in situ* SiN can work in conjunction with the PECVD SiN to form a bilayer passivation scheme, not only effectively suppressing the current collapse but also greatly mitigating the surface leakage, thereby ensuring low-leakage high-breakdown performance in GaN MISHEMTs. The high-performance GaN power transistors have demonstrated their great potential using an *in situ* SiN gate dielectric for efficient power switching applications as well.

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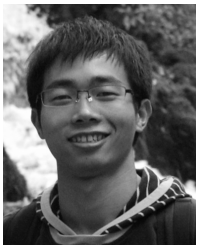

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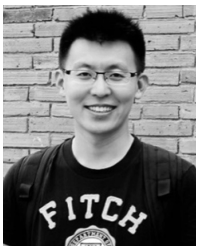

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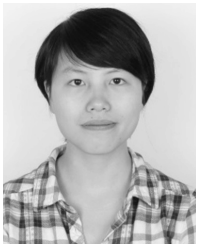

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