Monolithic Integration of Tunnel Diode-Based Inverters on Exact (001) Si Substrates

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***Abstract*— Monolithic integration of tunnel diode-based inverters on exact (001) Si substrates for the future high-speed, low-power, and compact digital circuits is demonstrated. A two-state inverter was fabricated using a forward biased fin-array tunnel diode as drive and a reverse-biased counterpart as load. On-chip operation and reduced fabrication complexity were achieved by exploiting the resistive characteristic of the reverse-biased tunnel diodes and the pre-defined patterns on the Si substrate.**

***Index Terms*— Tunnel diode, monolithic integration, inverter, digital circuits.**

I. Introduction

THE APPLICATION of tunnel diodes in digital circuits has long been recognized for advantages such as picosecond switching speed, reduced device counts per circuit function and low power consumption [1]–[3]. The folded I-V characteristic empowered by quantum mechanical tunneling has been utilized to fabricate ultra-high speed and compact circuits [4]. A simple series connection of a tunnel diode with a resistor or transistor can produce a circuit with double and even multi-stable states [5]. The inverter characteristic of tunnel diodes when connected with a load resistor is an inseparable part in multi-value logic design such as multiplexers [5], multi-valued adders [6], and mask programmable multi-valued logic gate [7]. III-V based tunnel diodes usually exhibit enhanced performance due to reduced tunneling mass and direct bandgap as compared with their Si based counterparts. Both silicon and III-V based tunnel diode digital circuits have been fabricated on their respective substrates with off-chip resistive components [8], [9]. However integration of III-V based digital circuits on conventional (001) Si substrates has not been explored.

Previously we have reported the fabrication and characterization of GaAs-InGaAs-GaAs tunnel diodes utilizing nano-scale fin-arrays grown on V-grooved Si by metal-organic chemical vapor deposition (MOCVD) [10]. Here, we present the monolithic integration of two-state inverters on exact (001) Si using the fabricated fin-array tunnel didoes with varying peak current densities. Off-chip components are completely eliminated by connecting the tunneling junctions with partially-etched GaAs fin-arrays. Compared with other tunnel diode based digital circuits, the tunnel diode based inverter presented here features extremely simple fabrication procedures with one-step photolithography and a subsequent wet etching process. Such simplified integration scheme ensures identical metal-semiconductor interfaces for all contact electrodes and eliminates potential surface damage from otherwise subsequent processing.

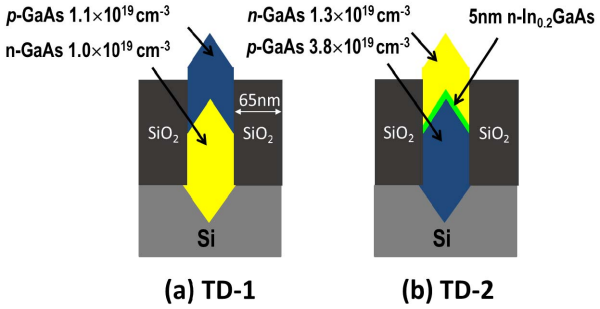

Fig. 1. Schematic of (a) TD-1 with a heavily doped p-GaAs/n-GaAs junction. (b) TD-2 with InGaAs insertion layer and reversed growth structure.

II. Device Structure and Fabrication

Two tunnel diode samples (TD-1 and TD-2) with fin-width of 65 nm were prepared on patterned (001) Si substrates using the same method detailed in [10] and [11]. Fig. 1 depicts schematics of two different diode epitaxial structure designs. The p- and n-electrode of TD-2 was in reverse of TD-1, with an InGaAs middle layer. Electron and hole densities were calibrated through Hall measurements of n- and p-type GaAs thin films grown on planar semi-insulating GaAs substrates, respectively. Identical growth parameters were used for the growth of n- and p-regions of the tunnel diodes. The tunnel diodes and inverters were fabricated simultaneously using the process described in Fig. 2. Contact electrodes were formed by e-beam evaporation and a subsequent lift-off process. We chose Pt/Au stack to contact top p-GaAs fin-arrays in TD-1 and Ni/Ge/Au stack to contact top n-GaAs fin-arrays in TD-2. Using the patterned metal pads as a self-aligned mask, mesa etching (H_3PO_4:H_2O_2:H_2O = 3:1:50) was performed to expose the underlying n-GaAs fin-arrays in TD-1 and p-GaAs fin-arrays in TD-2. After rinsing in DI water and blow-dry by N_2 gun, the devices were ready for measurement.

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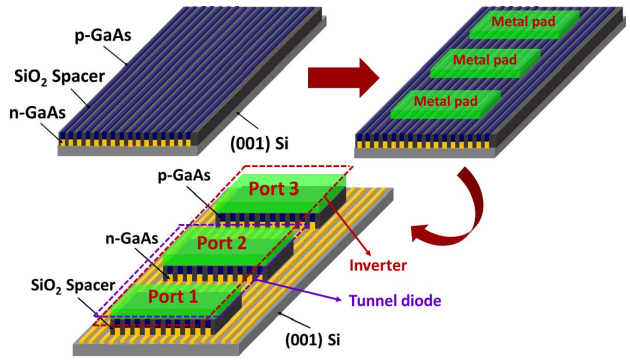

Fig. 2. Schematic and process flow of tunnel diodes and monolithically integrated inverters.

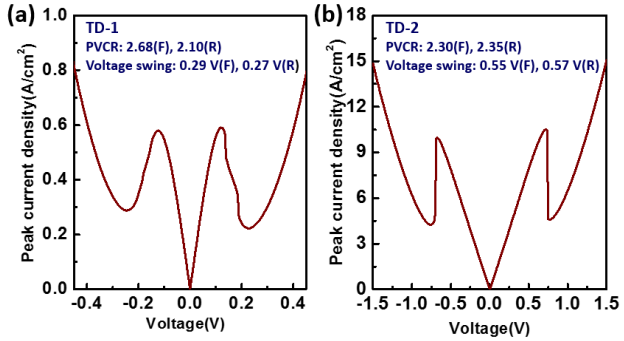

Fig. 3. Current-voltage characteristic of (a) TD-1 and (b) TD-2. (Note: F: forward bias, R: reverse bias).

III. Results and Discussion

The current-voltage (IV) characteristics were measured by probing on Port 1 and Port 2 in Fig. 2. Fig. 3 shows I-V curves measured from devices with a metal-pad dimension of 100×100 μm^2. Negative differential resistance (NDR) is clearly observed at room temperature. Unlike typical tunnel diodes with NDR only under forward bias, symmetric IV curves are obtained from our devices. Each tunnel diode is composed of two PN junctions connected in series. At either forward or reverse bias, one junction would be forward biased while the other is reverse biased. The kinks in the NDR region of TD-1 (Fig. 3(a)) indicate internal oscillation, commonly observed in the measurement of tunnel diodes [12]. A sharp transition in the NDR region accompanied by a large peak voltage (0.71 V) is observed in TD-2 (Fig. 3(b)), suggesting the presence of a large series resistance. Transmission line measurement (TLM) reveals a much larger contact resistance of 45 Ω·mm in TD-2 compared to TD-1 (8.6 Ω·mm). At forward bias, the peak to valley current ratios (PVCR) are 2.68 and 2.30 for TD-1 and TD-2, respectively. TD-2 exhibits an order higher peak current density of 10.5 A/cm^2 (normalized to the area of the (111) GaAs surface), with an increased voltage swing of 0.55 V. At reverse bias, both TD-1 and TD-2 show characteristics comparable to forward bias. It is noted that higher PVCR (5.08 for TD-1 and 3.57 for TD-2) has been measured from devices with a dimension of 40×40 μm^2.

Tunnel diodes with a dimension of 100×100 μm^2 were used to fabricate inverters for ease of measurement. Fig. 4(a) shows

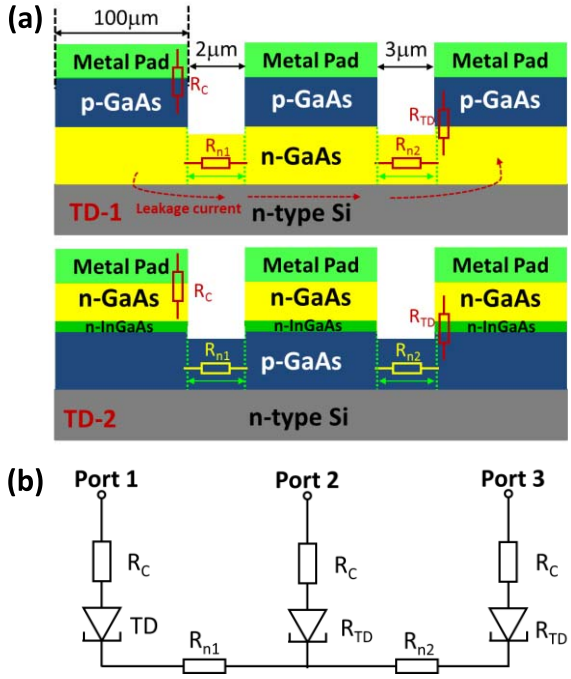

Fig. 4. (a) Cross section of the inverter along the direction of the GaAs fin-arrays. (b) Equivalent circuit of the inverter.

TABLE I
Comparison of the Parasitic Resistance of TD-1 and TD-2

	$R_c(\Omega)$	$R_{n1}(\Omega)$	$R_{n2}(\Omega)$	$R_{TD}(\Omega)$
TD-1	86	37	56	1.2k
TD-2	450	8	12	10

the cross-section view of an inverter along the direction of the fin-arrays. Three tunneling junctions are aligned in the V-grooved trenches and electrically connected by the partially etched GaAs fins. The distance between the tunneling junctions varies from 2 μm to hundreds of microns to obtain various load values. The equivalent circuit of the inverter is depicted in Fig. 4(b). R_C refers to the contact resistance between the metal and GaAs fin-arrays, which was determined by TLM measurement. R_{TD} is the equivalent resistance of the reversely biased tunnel diodes and can be obtained by fitting the slope of the tunnel diode IV curve near the origin. R_{n1} and R_{n2} represent the resistive value of the GaAs fins connecting the tunneling junctions, which were calculated by measuring the peak voltage shift when varying the probing pad spacing. Table I summarizes the parasitic resistances corresponding to the specific dimensions in Fig. 4(a). It should be noted that medium-doped n-type Si substrates were used in this work. Leakage current through the Si substrate is mitigated by the reversed growth structure in TD-2 as compared to TD-1.

The basic principle of the inverter is illustrated in Fig. 5(a). Two stable states Q1 and Q2 can be achieved by connecting a load resistor with a tunnel diode. The tunnel diode at Port 1 serves as drive while the load resistor is the sum of R_{n2}, R_{TD} and R_C at Port 3. Voltage sweep from 0 V to 0.5 V

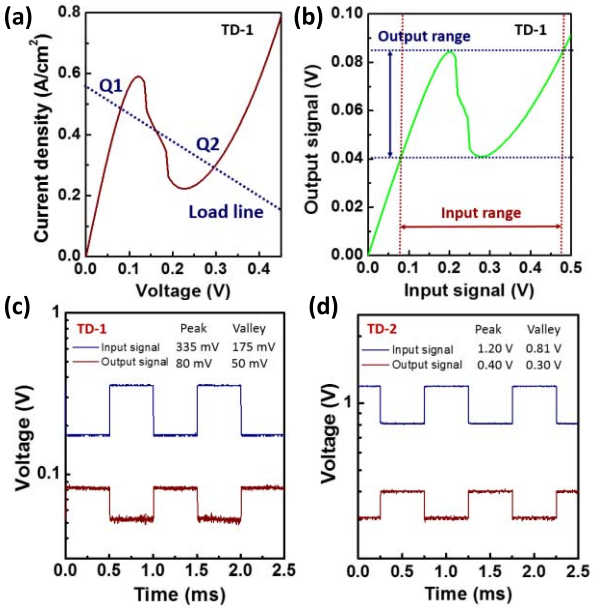

Fig. 5. (a) Basic principle of the tunnel diode based inverter. (b) Output signal and input signal characteristic of inverters based on TD-1. (c) Output and input square waveform characteristic of inverters based on TD-1. (d) Output and input square waveform characteristic of inverters based on TD-2.

was applied on Port-1, with Port-3 grounded. The output signal was measured from Port-2. From an inverter built on TD-1, we measured the output and input signal characteristic curve as shown in Fig. 5(b). The "N-shape" IV-curve plotted with the load line clearly illustrates the inverter characteristic, with the increase of input signal accompanied by output signal decrease. The input voltage range is determined as 80 to 480 mV and the output voltage range is from 40 to 84 mV. For inverter based on TD-2, voltage sweep from 0 V to 1.5 V was applied on Port-1 to accommodate the NDR region, with Port-3 grounded. The input voltage range is measured as 0.43 to 1.49 V and output voltage range is from 0.21 to 0.42 V. Using a function generator as signal source and an oscilloscope to capture output signal, the recorded input and output waveforms of TD-1 are shown in Fig. 5(c), exhibiting inverter characteristic. The input signal features 335 mV peak and 175 mV valley while the output signal exhibits 80 mV peak and 50 mV valley. Same measurement has also been performed with the inverter based on TD-2. Inverter characteristic is clearly observed with 1.20 V peak and 0.81 V valley for the input signal and 0.4 V peak and 0.3 V valley for the output signal. The improved input/output signal range is mainly due to the higher current density of TD-2. The visible noise of the output signal should be due to the initial noise from the function generator.

The input/output signal range increases with larger load resistance, as illustrated by the measured results from an inverter based on TD-1 in Fig. 6(a). Similar trend can also be observed from inverter based on TD-2, as evidenced by Fig. 6(b). Larger input/output signal ranges can improve signal to noise margin in actual use. Alternatively, both the input and output signal range can be tuned using a transistor as the load. Given recent progress in the integration of

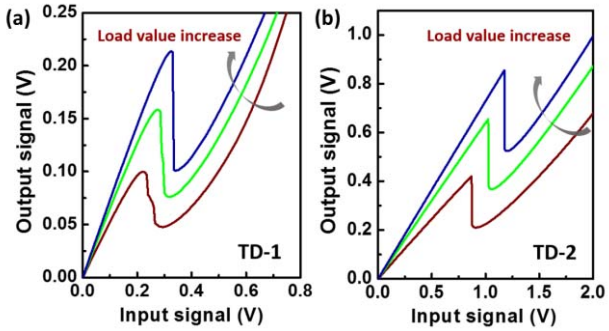

Fig. 6. (a) Output and input signal characteristic with varying load values of inverters based on (a) TD-1 (b) TD-2.

InGaAs FinFETs [13] and Gate-All-Around nanowire transistors [14] on Si using the aspect ratio trapping (ART) approach, co-integration of III-V tunnel diode based inverters and transistors onto a common Si platform would be promising for circuit speed enhancement and power reduction.

IV. Conclusion

In conclusion, a two-state inverter was monolithically integrated onto exact (001) Si substrates using GaAs/InGaAs fin-array tunnel didoes as drive and load. On-chip bistable operation was demonstrated with a simple fabrication process. These results show potential for future high speed, low power consumption and compact tunnel diode based memory and multi-valued digital circuits.

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