High Voltage Low Current Collapse AlGaN/GaN MISHEMTs with *in-situ* SiN Gate Dielectric

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***Abstract*—This paper reports on high performance AlGaN/GaN MISHEMTs with an *in-situ* SiN gate dielectric. Resulting from the high-quality gate dielectric and dielectric/barrier interface, the MISHEMTs with a gate-drain distance of 15 μm exhibit a high maximum drain current density of 1050 mA/mm, a steep subthreshold slope of 72 mV/dec, and a low gate-drain leakage of 0.6 μA/mm at V_{GD} of -900 V. The high breakdown voltage of 1200 V at I_D of 10 μA/mm, and low specific DC on-resistance of 1.7 mΩ·cm², yield a high power figure of merit (FOM = $V_{BR}^2/R_{on,sp}$) of 847 MW/cm² for the fabricated devices. Moreover, a small dynamic/DC on-resistance ratio of 1.03 is achieved in the MISHEMTs using the *in-situ* SiN/PECVD SiN bilayer passivation scheme.**

Keywords—AlGaN/GaN MISHEMTs; current collapse; high voltage; in-situ SiN.

GaN-based metal-insulator-semiconductor high-electron-mobility transistors (MISHEMTs) are promising for the next generation energy-efficient power switching applications. A high-quality gate dielectric and dielectric/III-nitride interface are crucial to achieve robust MISHEMT operation. MOCVD grown *in-situ* SiN has been recently employed as a gate dielectric for GaN MISHEMTs, exhibiting excellent leakage blocking capability [1, 2]. However, the quality of the *in-situ* SiN and the *in-situ* SiN/III-N interface highly depend on the growth conditions [3]. This paper presents the device results of MISHEMTs using *in-situ* SiN as the gate dielectric with superior interface quality. High breakdown voltage, low on-resistance, low off-state leakage, low current collapse have been achieved simultaneously in the MISHEMTs.

In-situ SiN/AlGaN/GaN heterostructures were grown on a 2-inch sapphire substrate by MOCVD. The epilayers, as shown in Fig.1, consist of a 3 μm GaN buffer, a 1 nm AlN spacer, a 20 nm $Al_{0.3}Ga_{0.7}N$ barrier, and a 14 nm *in-situ* grown SiN cap. The device fabrication started with source/drain Ohmic contact formation using an alloyed Ti/Al/Ni/Au-based metal stack. Then device isolation was performed using Ar-implantation, followed by gate metallization of Ni/Au. Finally, the devices were passivated with 100 nm PECVD SiN. After device fabrication, the Ohmic contact resistance and the sheet resistance of 2DEG were determined to be 0.5 Ω·mm and ~400 Ω/sq, respectively by TLM measurements.

Fig.2 plots the double sweep transfer characteristics of a typical device. The MISHEMT exhibits a high on/off current ratio of ~10^9 and a steep subthreshold slope of 72 mV/dec, as well as a negligible hysteresis of 50 mV. Fig.3 compares the DC/gate-pulsed IV dispersion of the MISHEMT with an L_{GD} of 15 μm. The device delivers a maximum drain current density of 1050 mA/mm at V_{GS} = 2V and V_{DS} = 15 V. The DC on-resistance is 8.5 Ω·mm, resulting in a specific on-resistance $R_{on,sp}$ of 1.7 mΩ·cm². Compared to the DC R_{on}, only 3% increase in the R_{on} was observed under pulsed IV measurement, indicating effective suppression of current collapse by using the *in-situ* SiN/PECVD SiN bilayer passivation scheme. Fig.4 shows the two terminal gate-drain leakage under reverse gate-drain bias. The leakage is as low as 0.6 μA/mm at V_{GD} of -900 V, suggesting the excellent leakage-blocking capability of the *in-situ* SiN. Fig.5 shows a nearly linear dependence of off-state breakdown voltage (V_{BR}) on the gate-drain distance. The V_{BR} for the MISHEMT was determined as the voltage when I_D reaches 10 μA/mm. MISHEMTs with L_{gd} of 15 μm show a high V_{BR} of 1200 V. Fig.6 benchmarks the $R_{on,sp}$ versus V_{BR} of MISHEMTs in this work with other depletion-mode MISHEMTs reported in literature. Combined R_{on} and V_{BR} of the MISHEMTs results in a high power figure of merit ($V_{BR}^2/R_{on,sp}$) of 847 MW/cm². The superior device performance is attributed to the high-quality *in-situ* SiN/AlGaN interface. Minimal frequency dispersion and sharp transition slopes in the frequency-dependent capacitance-voltage characteristics (Fig. 7) indicate a low interface trap state density. The trap density extracted by parallel conductance measurement shown in Fig. 8 ranges from 3×10^{11} to 3×10^{12} $cm^{-2}eV^{-1}$.

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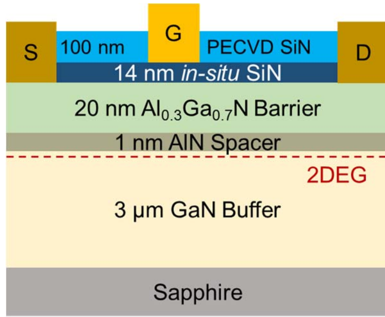

Fig.1. Cross-sectional schematic of fabricated MISHEMTs.

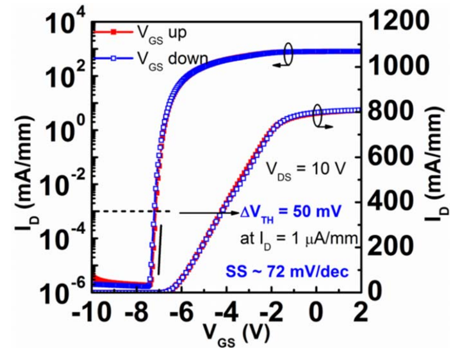

Fig.2. Double sweep transfer characteristics of the MISHEMTs. The device has dimensions of $L_G/L_{GS}/L_{GD}/W_G$ = 1.5/1.5/15/10 μm.

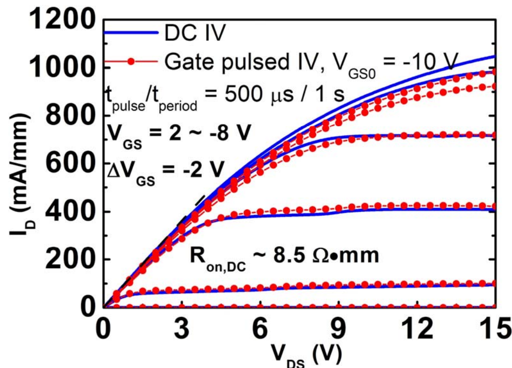

Fig.3. DC/gate pulsed IV of the MISHEMTs. The device has dimensions of $L_G/L_{GS}/L_{GD}/W_G$ = 1.5/1.5/15/10 μm.

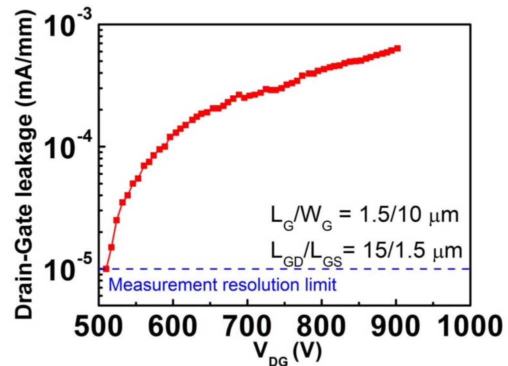

Fig.4. Two-terminal reverse biased gate-drain leakage of the MISHEMTs with L_{GD} of 15 μm. the leakage is below the measurement setup resolution for V_{DG} < 500 V.

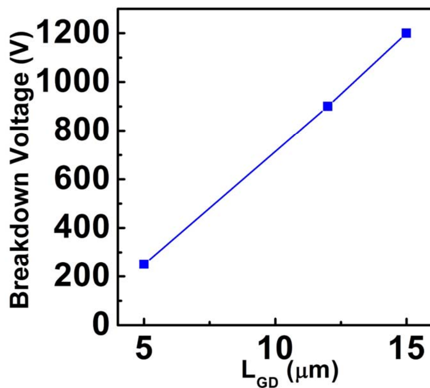

Fig.5 Breakdown voltage versus gate-drain distance.

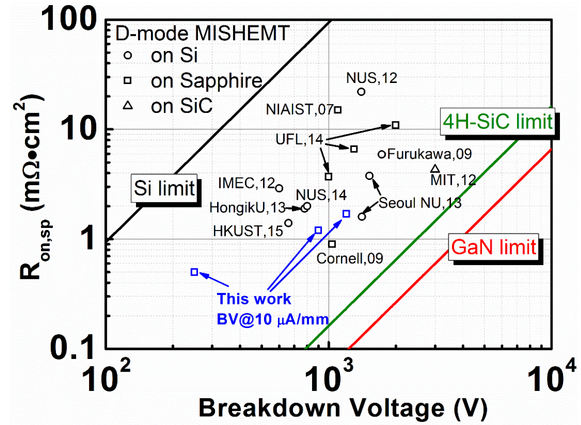

Fig.6. Benchmarking of specific on-resistance versus breakdown voltage for D-mode MISHEMTs on different substrates.

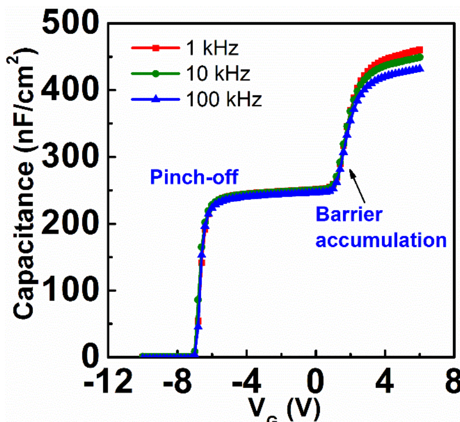

Fig.7. Frequency dependent capacitance voltage characteristics of circular MIS capacitors with a diameter of 200 μm.

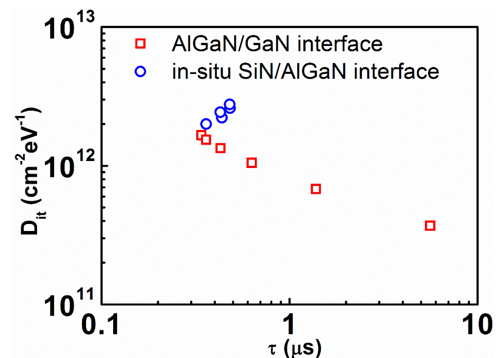

Fig.8. Extracted interface trap density D_{it} versus corresponding time constant.

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