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Off-state drain leakage reduction by post metallization annealing for Al$_2$O$_3$/GaN/AlGaN/GaN MOSHEMTs on Si

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Impact of post metallization annealing (PMA) on the off-state drain leakage (I_{off}) for Al$_2$O$_3$/GaN/AlGaN/GaN metal-oxide-semiconductor high electron mobility transistors (MOSHEMTs) on Si has been investigated. After implementation of PMA at 500 °C for 10 min in N$_2$ ambient, the I_{off} can be reduced by three orders of magnitude compared to that without PMA. In consequence, a high on/off current ratio of 10^8 and a steep subthreshold slope of 71 mV/dec are achieved for the MOSHEMTs. The reduction of I_{off} results from the suppression of source-drain surface leakage through the interface between Al$_2$O$_3$ and GaN. The decrease of accumulation capacitance of the MOS capacitors (MOSCAPs) after 500 °C PMA suggests an oxidation process at the GaN surface during the high temperature annealing, which was confirmed by the increase of oxide layer thickness measured by transmission electron microscopy (TEM), and also the increase of Ga–O/Ga–N bond ratio at the Al$_2$O$_3$/GaN interface revealed by X-ray photoelectron spectroscopy (XPS). These results suggest that the significant reduction of I_{off} after 500 °C PMA can be attributed to partial surface oxidation of the GaN cap, which suppresses the conduction path at the Al$_2$O$_3$/GaN interface.

1 Introduction GaN-based high electron mobility transistors (HEMTs) have demonstrated great potential for power switching and high frequency power amplifier applications [1–3]. The conventional HEMT with Schottky gate structure usually suffers from high gate leakage, which would increase the standby power loss and also limit the gate forward bias. In order to block the gate leakage current and suppress the drain current collapse, the Al$_2$O$_3$ gate dielectric by atomic layer deposition (ALD) has been adopted to form metal-oxide-semiconductor HEMTs (MOSHEMTs) [4–7]. However, adding an insulator between the gate metal and barrier layer creates an extra dielectric/(Al)GaN interface, which could introduce high density donor-like interface traps [8, 9]. These trap states can assist the two-dimensional variable range hopping (2D-VRH) conduction, resulting in serious surface leakage

current through the interface [10, 11]. Consequently, a high off-state drain leakage current (I_{off}) can be a serious issue for the MOSHEMTs. Post metallization annealing (PMA) has been studied to improve the gate contact with dielectric and also to reduce the fixed charges at the dielectric/semiconductor interface or within the dielectric bulk [12–16]. Most of these studies mainly focus on the influence of PMA on the threshold voltage of MOSHEMTs.

In this work, we investigated the effects of PMA on the I_{off} for Al$_2$O$_3$/GaN/AlGaN/GaN MOSHEMTs on Si. It was found that PMA at 500 °C in N$_2$ for 10 min can reduce the I_{off} by three orders of magnitude, resulting in a high on/off current ratio of 10^8 and a steep subthreshold slope (SS) of 71 mV/dec. The reduction of accumulation capacitance of the MOS capacitors (MOSCAPs) after 500 °C PMA revealed a partial oxidation of the GaN surface.

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Transmission electron microscopy (TEM) and X-ray photoelectron spectroscopy (XPS) techniques were performed to identify the oxidation process at the Al_2O_3/GaN interface during the high temperature annealing.

2 Experimental The GaN/AlGaN/GaN heterostructure used in this work was grown on a 6-inch n-type Si substrate by metal-organic chemical vapor deposition (MOCVD). As shown in Fig. 1(a), the epilayer, from bottom to top, consists of a 200-nm AlN nucleation layer, an 800-nm step-graded AlGaN layer, a 2-μm unintentionally doped GaN layer, a 1-nm AlN spacer, a 30-nm $Al_{0.25}Ga_{0.75}N$ barrier, and a 2-nm GaN cap. Hall measurements showed a sheet carrier density of 7×10^{12} cm^{-2} and mobility of 1800 cm^{2}V^{-1}s^{-1}, resulting in an average sheet resistance of 500 Ω/sq. Atomic force microscope (AFM) observation of the as-grown HEMT epi on Si showed a smooth surface morphology with root mean square (RMS) roughness of 0.5 nm across a 5×5 μm^2 scanned area.

The MOSHEMT fabrication started from device isolation by BCl_3/Cl_2-based inductively coupled plasma (ICP) etching. The mesa depth was around 150 nm. Then the source/drain metal stack Ti/Al/Ni/Au (20/150/50/80 nm) was deposited by e-beam evaporation and annealed at 850 °C in N_2 ambient for 30 s to form Ohmic contact. After that, the sample was cleaned by an oxygen plasma treatment with a power of 100 W for 1 min and a HCl:H_2O (1:3) solution immersion for 2 min. Then a 10-nm Al_2O_3 gate

dielectric was deposited immediately in an Oxford Instruments atomic layer deposition (ALD) system at 300 °C using trimethylaluminum (TMA) and H_2O vapor as precursors. Finally the Ni/Au (20/200 nm) gate metal was deposited by e-beam evaporation. After device fabrication, the sample was separated into four pieces, three of which were annealed at 300, 400, and 500 °C, respectively, by rapid thermal annealing (RTA) process in N_2 ambient for 10 min. The MOSHEMTs used in the following characterization are with 2 μm gate length, gate-source and gate-drain distance of 1 μm, and gate width of 10 μm. Circular MOSCAPs with 200 μm in diameter were also fabricated on the same sample for capacitance–voltage (CV) characterization.

3 Results and discussion Figure 2 shows the drain current and gate leakage current versus gate bias for the fabricated MOSHEMTs. For all the devices without and with various PMAs, the gate leakage currents remain below 10^{-6} mA mm^{-1}. The devices without PMA show a high I_{off} of 10^{-2} mA mm^{-1} at V_{GS} of -8 V and V_{DS} of 6 V. The large difference between the gate leakage current and the I_{off} indicates that the I_{off} is dominated by the drain-to-source leakage. No obvious change in the I_{off} is observed for the devices with PMA at 300 °C and 400 °C, while the I_{off} is reduced by three orders of magnitude for the devices with PMA at 500 °C. Consequently, a high I_{on}/I_{off} ratio of $\sim 10^8$ and a sharp SS of 71 mV/dec are achieved for the MOSHEMTs with 500 °C PMA. The positive shift of threshold voltage for samples with PMA was attributed to the reduction of fixed positive charges at the Al_2O_3/GaN interface or within Al_2O_3 bulk [12, 13].

In order to find out the impact of PMA on the effectiveness of the Al_2O_3 passivation in the access region, DC-pulsed IV dispersion of output characteristics for the MOSHEMTs without PMA and with various PMA conditions were characterized, as compared in Fig. 3. For the DC output characteristics, the maximum drain current at the gate bias of $+2$ V for the device with 500 °C PMA is $\sim 20\%$ lower than that without PMA. This is partially due to the positive shift of the threshold voltage after 500 °C PMA, which reduces the gate overdrive voltage. On the other hand,
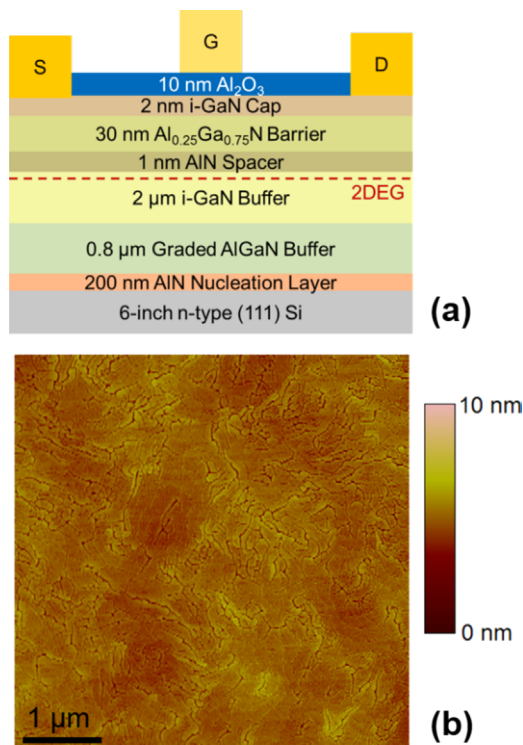
Figure 1 (a) Cross-sectional schematic of fabricated MOSHEMTs and (b) AFM image with 5×5 μm^2 scan for the as-grown GaN/AlGaN/GaN HEMT structure on Si.
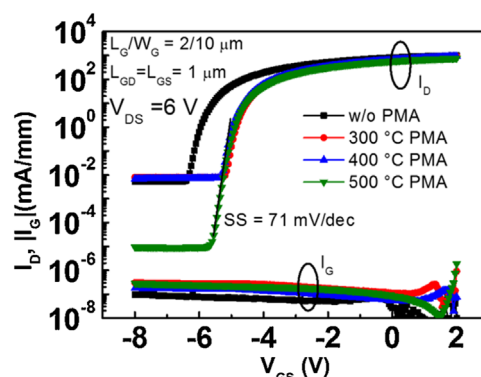
Figure 2 Comparison of drain and gate current versus gate bias of devices without and with different PMAs at V_{DS} of 6 V.
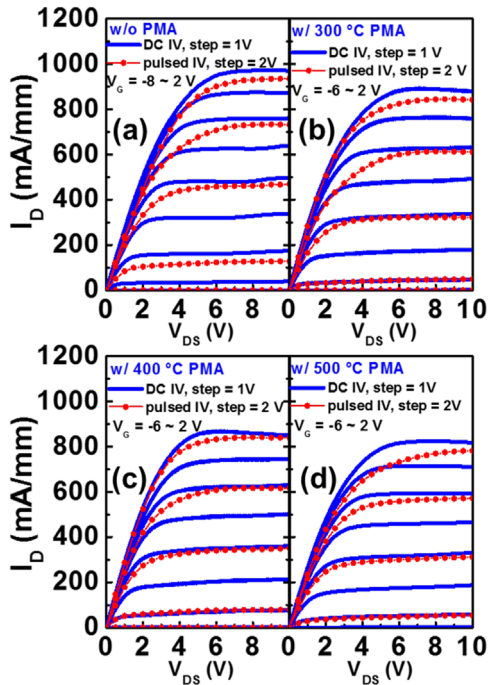
Figure 3 DC/gate pulsed output characteristics of the MOS-HEMTs (a) without PMA, (b) with 300 °C PMA, (c) with 400 °C PMA, and (d) with 500 °C PMA. The pulse period is 1 s and pulse width is 500 μs. Gate pulse base voltage V_{GS0} is −8 V.

the sheet resistance (R_{sh}) and Ohmic contact resistance (R_c), measured 387 Ω/sq and 1.1 Ω · mm without PMA, slightly increase to 400 Ω/sq and 1.2 Ω · mm after 500 °C PMA. The slight increase of R_{sh} and R_c may have contributed to the decrease of maximum drain current. For the pulsed IV characterization, a pulsed voltage with duty/period of 500 μs/1 s was applied to the gate with the base voltage at −8 V (quiescent bias at pinch-off condition). On-state resistance (R_{on}) was extracted in the linear region with gate bias of +2 V and compared between DC and gate pulsed IV. The ratio of $R_{on,pulse}/R_{on,DC}$ is 1.13, 1.03, 1.02, and 1.09 for the device without PMA, with 300, 400, and 500 °C PMA, respectively. The little increase of the $R_{on,pulse}$ compared to the $R_{on,DC}$ indicates good surface passivation effect of the Al_2O_3, and the negligible difference between the ratio of $R_{on,pulse}/R_{on,DC}$ without PMA and that with various PMA conditions suggests good thermal stability of the effective Al_2O_3 passivation.

Figure 4 shows the buffer leakage between two individual Ohmic pads with both width and gap of 100 μm for samples without and with various PMA temperatures. The buffer leakage of a HEMT sample fabricated using the same epi wafer was added for comparison with the same PMA conditions. It can be seen that the buffer leakage currents for the MOSHEMT samples without PMA and with 300 and 400 °C PMA are three orders of magnitude higher than that of the HEMT sample with/without PMA. The significantly increased buffer
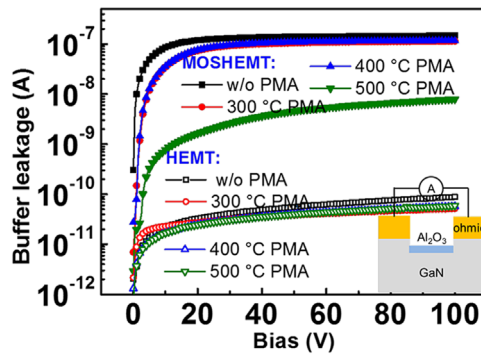

Figure 4 Buffer leakage comparison of MOSHEMT and HEMT samples without and with various PMAs. The pad width and gap both are 100 μm.

leakage mainly results from the surface leakage at the Al_2O_3/GaN interface. With PMA at 500 °C, the surface leakage can be reduced by more than one order of magnitude.

Double-sweep mode CV characteristics of the MOS-CAPs on samples without PMA, with 300 °C PMA and with 500 °C PMA were shown in Fig. 5. The accumulation capacitance for the MOSCAP with 500 °C PMA is ~10% lower than those without PMA and with 300 °C PMA. The reduction of the accumulation capacitance indicates the increase of equivalent oxide thickness (EOT). Moreover, the hysteresis in the CV of MOSCAPs can be reduced from ~0.2 V without PMA to ~0.1 V with 300 and 500 °C PMA, suggesting an improved interface after PMA. The reduction of the accumulation capacitance is also part of the reasons for the decrease of maximum drain current of MOSHEMTs with 500 °C PMA. It was suspected that the GaN surface had been oxidized during the high temperature annealing.

To compare the oxide thicknesses for samples without and with 500 °C PMA, two samples were prepared with 10 nm Al_2O_3 and 20 nm Ni on top for TEM observation. PMA at 500 °C was performed for one of them. The cross-sectional TEM images for the two samples are shown in
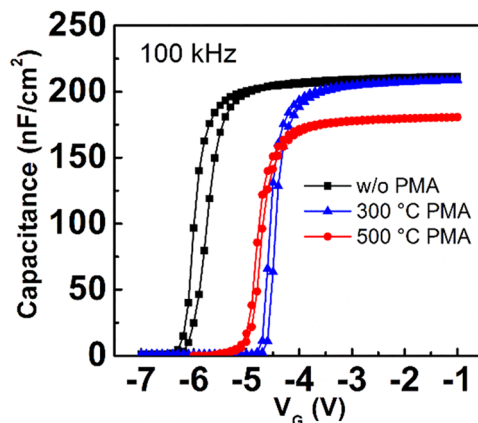

Figure 5 Capacitance–voltage characteristics of circular MOS-CAPs without and with various PMAs.

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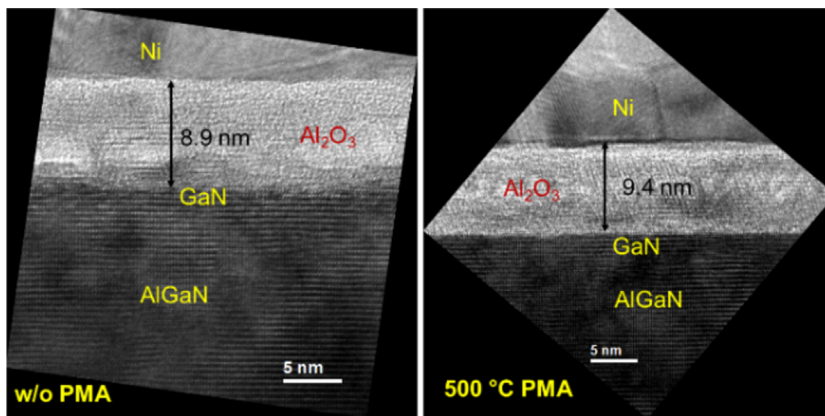
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Figure 6 Cross-sectional TEM images for samples without PMA and with 500 °C PMA.

Fig. 6. The oxide layer thickness increases slightly from 8.9 to 9.4 nm and the interface of Al_2O_3/GaN is more abrupt after 500 °C PMA.

To further verify the oxidation process during the 500 °C PMA, the chemical bonding composition at the Al_2O_3/GaN interfaces was revealed by XPS, using a monochromatic Al K_α radiation source ($hv = 1486.6$ eV). Two GaN/AlGaN/GaN samples with 2 nm Al_2O_3 on top were prepared. After Al_2O_3 deposition, one of the two samples was annealed at 500 °C in N_2 ambient for 10 min by RTA (500 °C PMA condition). Figure 7 shows the Ga 3d core-level spectra of the two samples. The peaks are de-convoluted into four major components attributed to Ga–Ga, Ga^+–O (Ga_2O), Ga–N, and Ga^{3+}–O (Ga_2O_3) [17]. The two oxidation states Ga_2O and Ga_2O_3 contribute together to the Ga–O bond component. By calculating the percentage of each component, the Ga–O/Ga–N bond ratio was found increased from 0.32 to 0.62 after 500 °C annealing. The increase of Ga–O/Ga–N bond ratio indicates the oxidation process at the Al_2O_3/GaN interface during the high temperature annealing. The significant increased Ga 1+

oxidation state suggests the formation of a thin Ga_2O interfacial layer, which was believed to give rise to a lower defect density and favorable impact on surface passivation [18]. Therefore, the 2D-VRH conduction, which was regarded as the mechanism of surface leakage in passivated GaN HEMTs [11], can be suppressed. Consequently, the I_{off} can be significantly reduced.

4 Conclusions The impact of PMA on the I_{off} for GaN MOSHEMTs on Si has been investigated in this study. It is found that the I_{off} can be reduced by three orders of magnitude with PMA at 500 °C in N_2 for 10 min. The reduction of I_{off} results from the suppression of surface leakage, which is achieved by the surface oxidation process at the interface of Al_2O_3/GaN during the high temperature annealing.
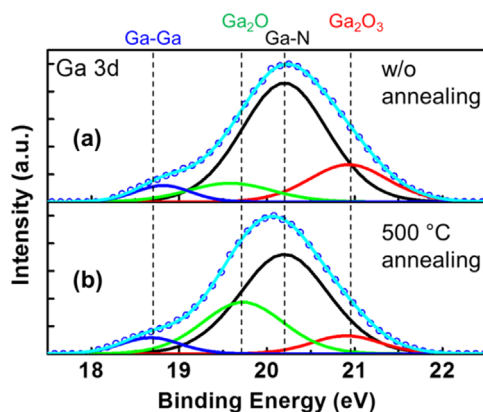
Figure 7 Ga 3d core-level spectra at the Al_2O_3/GaN interface of the Al_2O_3/GaN/AlGaN/GaN samples (a) without annealing and (b) with 500 °C annealing. Each measured spectrum (blue circle symbol) was de-convoluted into four major components (solid lines) corresponding to Ga–Ga (blue), Ga_2O (green), Ga–N (black), and Ga_2O_3 (red).

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