Fabrication and Characterization of Gate-Last Self-Aligned AlN/GaN MISHEMTs With *In Situ* SiN_x Gate Dielectric

Xing Lu, Jun Ma, Huaxing Jiang, Chao Liu, Peiqiang Xu, and Kei May Lau, *Fellow, IEEE*

***Abstract*— This paper reports on the fabrication and characterization of gate-last self-aligned *in situ* SiN_x/AlN/GaN MISHEMTs. The devices featured *in situ* grown SiN_x by metal–organic chemical vapor deposition as a gate dielectric and for surface passivation. Selective source/drain regrowth was incorporated to reduce contact resistance. SiN_x sidewall spacers and low-κ benzocyclobutene polymer ($\kappa = 2.65$) supporting layers were employed under the gate head to minimize the parasitic capacitance for high-frequency operation. The device with a gate length (L_G) of 0.23 μm exhibited a maximum drain current density (I_{DS}) exceeding 1600 mA/mm with a high ON/OFF ratio (I_{ON}/I_{OFF}) of over 10^7. The current gain cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) were 55 and 86 GHz, respectively. In addition, the effect of temperature, from room temperature up to 550 K, on the dc and RF performances of the gate-last self-aligned MISHEMTs was studied.**

***Index Terms*— AlN/GaN, benzocyclobutene (BCB) planarization, gate-last self-aligned, high-temperature, *in situ* SiN_x, MISHEMT, RF, source/drain (S/D) regrowth.**

I. Introduction

GaN-BASED HEMTs have a great potential for RF/millimeter wave power applications due to their unique combination of high electron velocity, large sheet carrier density, and high breakdown field [1]. In recent years, remarkable progress in GaN HEMTs has been made, with the reported f_T and f_{max} exceeding 300 GHz [2]–[10]. Such results were accomplished through novel heterostructures and innovative device fabrication technologies, such as a thin AlN or InAlN top barrier [2]–[7], [10]–[16], an AlGaN or InGaN back barrier [2], [4], [6]–[10], an N-polar GaN HEMT structure [4], [8], [9], heavily doped source/drain (S/D) ohmic contact regrowth [2]–[9], [12], [13], advanced T-gate fabrication process [2]–[6], [9], or a gate-first self-aligned approach [4], [8]. f_T and f_{max} of GaN HEMTs can be primarily improved through the downscaling of device geometry, whereas the aspect ratio (gate length and gate-to-channel distance) has to be maintained for the mitigation of short-channel effects. The significant drop of the 2-D electron gas (2-DEG) density with the decrease in the AlGaN barrier thickness impedes the progress of device scaling for the conventional AlGaN/GaN HEMTs. On the other hand, the AlN/GaN heterostructure with a thin barrier layer offers high carrier density and good gate control capability simultaneously, which is attributed to the relatively large bandgap and strong polarization effects of AlN [17]–[19]. Recently, a high-quality AlN/GaN epitaxial growth has been reported with a large 2-DEG concentration ($>10^{13}$ cm^{-2}) and high mobility (>1000 cm^2/V $\cdot$ s) for extremely thin AlN barriers (<6 nm) [18]. However, the ultrathin AlN barriers generally suffer from surface sensitivity and lead to large gate leakage currents unless they are well passivated [13], [14]. *In situ* SiN_x grown in the metal–organic chemical vapor deposition (MOCVD) reactor immediately after the heterostructures has shown advantages over other *ex situ* deposited insulators for GaN HEMTs for reasons, such as better surface passivation effects, suppression of gate leakage current, and elimination of process- and growth-related defects [17], [20]–[22]. High-performance AlN/GaN HEMTs have been reported with an *in situ* SiN_x cap layer for surface passivation rather than a gate dielectric [15]–[17]. The SiN_x in the gate region was selectively removed during the device fabrication.

This paper reports the fabrication as well as materials and electrical characterizations of AlN/GaN MISHEMTs that employ *in situ* SiN_x as a gate dielectric and also for surface passivation and protection. A novel gate-last self-aligned process was developed for device fabrication [23]. Regrown ohmic contacts and low-κ benzocyclobutene (BCB) planarization [24], [25] have enabled the reduction of the access resistance and the parasitic capacitance, thus minimizing the RC-related delay. The devices also feature precisely defined gate-to-regrown-S/D distances (L_{GS}/L_{GD}) by the SiN_x sidewall spacers. Compared with the gate-first self-aligned process [4], [8], the T-shaped gate formed in this gate-last approach enables high f_T and f_{max} simultaneously. In addition, the demonstrated gate-last self-aligned process is

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less demanding in the gate lithography than the conventional T-gate process [2]–[6], [9], which can potentially reduce the process complexity and improve the yield.

In addition, the GaN-based devices, inherently possessing a wide bandgap and great thermal stability, can operate properly, even at high temperatures. To fully explore the potential of the devices operating at high temperature, it is important to evaluate their high-temperature behavior [26]–[28]. In this paper, both dc and RF performances of the gate-last self-aligned MISHEMTs at temperatures up to 550 K were investigated. The thermal dependence of the main parameters, such as I_{DS}, peak transconductance (G_m), gate-to-source capacitance (C_{gs}), gate-to-drain capacitance (C_{gd}), and output resistance (R_{ds}), has been extracted and discussed. These results present a roadmap for device structure and process optimizations so as to improve the high-temperature performance, which is crucial for the development of the next-generation high-speed power transistors.

II. AlN/GaN Heterostructure and *In Situ* SiN_x Gate Dielectric

The *in situ* SiN_x/AlN/GaN heterostructures used in this paper were grown on a 2-in sapphire substrate in an AIXTRON 2000 HT MOCVD system. The epilayers consist of, from bottom to top, a 35-nm low-temperature AlN nucleation layer, a 300-nm high-temperature AlN buffer layer, a 2.7-μm undoped GaN layer, followed by a 3-nm AlN barrier layer, and, finally, a 7-nm *in situ* SiN_x cap layer. The *in situ* SiN_x was grown at 1145 °C immediately after the AlN/GaN heterostructure growth in the same MOCVD chamber, using silane and ammonia as precursors [21]. The growth rate of the *in situ* SiN_x was ~1.8 Å/min. For the electrical characterization of the *in situ* SiN_x/AlN/GaN MIS structures, circular-shaped MIS diodes were fabricated. First, mesa etching for device isolation was performed using CF_4/O_2-based reactive ion etching (RIE), followed by a Cl_2-based inductively coupled plasma (ICP) etch. After selective removal of the SiN_x cap layer in the ohmic contact region by RIE, Ti/Al/Ni/Au (20/150/50/80 nm) was deposited by e-beam evaporation and annealed at 850 °C in N_2 ambient for 30 s. Finally, the Ni/Au (20/200 nm) gate metal was deposited on the *in situ* SiN_x by e-beam evaporation. The diameter of the circular metal gate was 120 μm.

The atomic force microscopy (AFM) image of the as-grown sample in Fig. 1(a) shows a smooth surface morphology. The root mean square (rms) roughness across a 5-μm × 5-μm scanned area is 0.43 nm. Room temperature (RT) Hall measurements revealed a 2-DEG density of 1.41 × 10^{13}/cm^2 and a mobility of 1010 cm^2/V · s, corresponding to a sheet resistance (R_{sh}) of 438 Ω/□. The results indicate that the *in situ* SiN_x cap layer can effectively prevent the relaxation of the AlN barrier during the postgrowth cooling process. Ma *et al.* [29] found that the electrical characteristics of the *in situ* SiN_x/AlN/GaN MIS structures were very sensitive to the growth conditions, such as temperature, pressure, and the gas flow of silane and ammonia, of the SiN_x cap layer. The self-etching effect of SiH_4 on the AlN barrier was obvious when the growth conditions for the SiN_x cap layer were not carefully optimized. This can lead to rough surface morphology and low 2-DEG mobility. Fig. 1(b) shows the AFM image of another sample, which has an identical structure to that shown in Fig. 1(a), except that the topmost *in situ* SiN_x layer was grown under unoptimized conditions. It can be seen that the surface of the nonoptimal sample is relatively uneven and the rms roughness rises to 1.1 nm. The 2-DEG mobility drops down to only 770 cm^2/V · s due to the roughness.

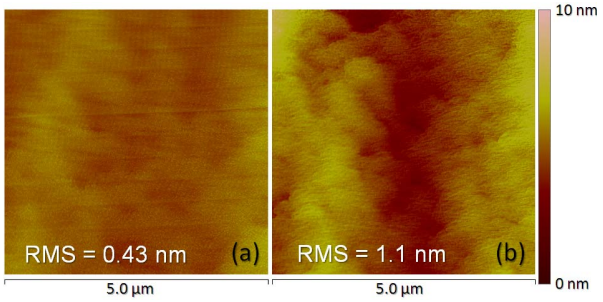

Fig. 1. AFM images of two *in situ* SiN_x/AlN/GaN MISHEMT samples with (a) optimum and (b) nonoptimal *in situ* SiN_x growth conditions.

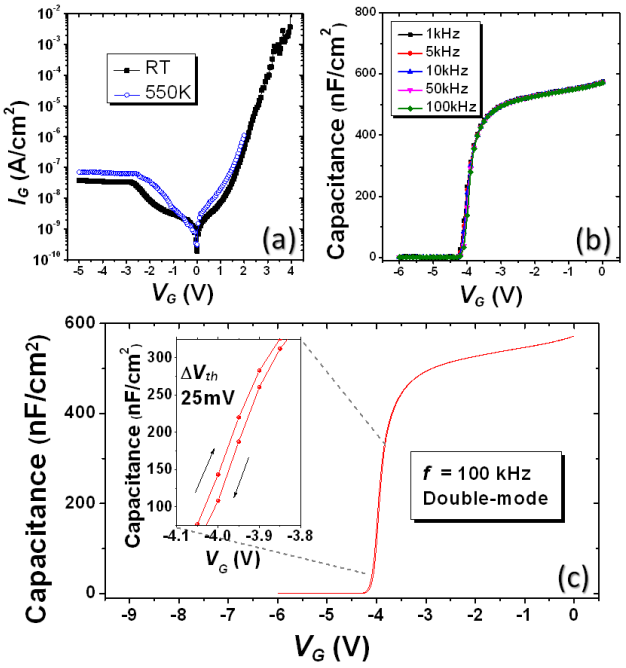

Fig. 2. (a) Gate leakage current measurements of the *in situ* SiN_x/AlN/GaN MIS diode at two different temperatures, RT and 550 K. (b) C–V characteristics of the MIS diode at multiple frequencies. (c) Double-mode C–V characteristics at 100 kHz.

We believe that the *in situ* SiN_x gate dielectric in this paper is of high quality because of the high growth temperature and the low growth rate. Fig. 2(a) shows the typical gate leakage current measurements of the *in situ* SiN_x/AlN/GaN MIS diode at two different temperatures, RT and 550 K. Even at a high temperature of 550 K, the reverse gate leakage current density of the MIS diode is below 10^{-7} A/cm^2, remarkably lower than that of similar structures using other dielectrics [30]. The 7-nm *in situ* SiN_x on the AlN/GaN heterostructure can tolerate

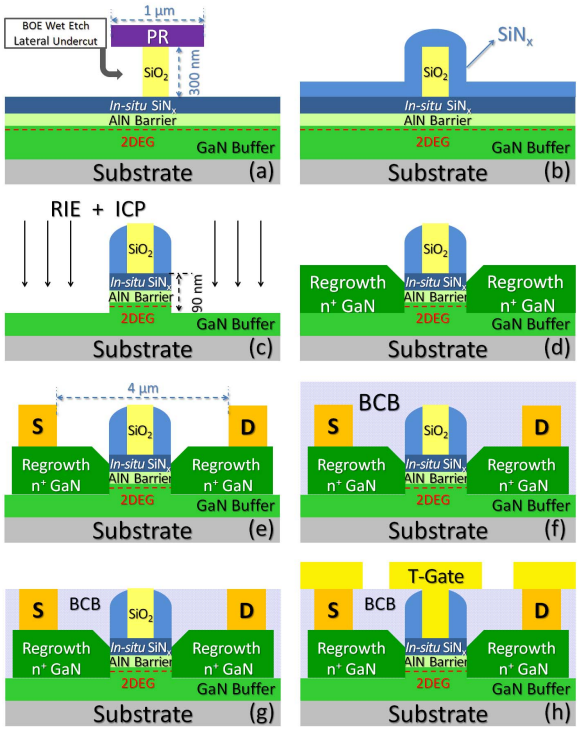

Fig. 3. Schematic of the gate-last self-aligned process flow.

a forward gate bias up to 4 V at RT, as shown in Fig. 2(a). An XPS analysis reveals that the *in situ* SiN_x in this paper is slightly Si-rich, with an N/Si ratio of 1.29. Undeniably, the Si-rich SiN_x contains Si dangling bonds and distorted excess Si-Si bonds, which may result in midgap defect states or bulk traps [21]. Thus, there is still room for improvement in the stoichiometry of the *in situ* SiN_x gate dielectric in this paper.

The fact that the SiN_x gate dielectric is grown *in situ* means that the AlN surface is never exposed to air. The main benefit is the prevention of oxidation/contamination of the AlN surface due to air exposure or damage during the device fabrication process. Thus, the formation of interface states would be suppressed or reduced. Fig. 2(b) and (c) shows the multiple frequency and double mode capacitance–voltage (C–V) characteristics of the MIS diode, respectively. Sharp rising slopes with small frequency dispersions between 1 and 100 KHz and tiny hysteresis (~25 mV) can be observed, suggesting a high-quality interface between the *in situ* SiN_x gate dielectric and the AlN barrier. These exciting results reveal the potential of this novel structure for high-speed power transistor applications.

III. Gate-Last Self-Aligned Process

The gate-last self-aligned process was realized by means of a dummy gate [13], which was eventually removed after BCB planarization and replaced with a metal gate. Fig. 3 shows the detailed process flow. First, 300-nm-thick SiO_2 layer was deposited by the plasma-enhanced chemical vapor deposition (PECVD). The initial 1-μm SiO_2 dummy gate was defined by photolithography and patterned using a RIE process. Subsequently, wet lateral etching was performed

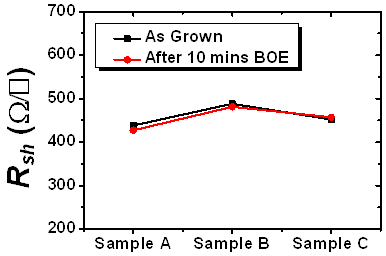

Fig. 4. Sheet resistance R_{sh} of the *in situ* SiN_x/AlN/GaN MISHEMT sample before and after BOE immersion.

in a buffered oxide etch (BOE) to further shrink the SiO_2 gate length down to <500 nm [Fig. 3(a)]. A layer of PECVD SiN_x was then blanket deposited, followed by an anisotropic RIE process to form sidewall spacers. Before regrowth, the S/D regions were exposed by ICP, etching down to the GaN buffer. The etch depth into the MISHEMT structure was 90 nm [Fig. 3(b) and (c)]. Afterward, 180 nm n^+-GaN with a two-step doping profile (Si doping level: $\sim 2 \times 10^{19}$ cm^{-3} for the first 30 nm and up to 6×10^{19} cm^{-3} for the remaining 150 nm) was grown in the exposed S/D regions by MOCVD [Fig. 3(d)]. The light doping used at the beginning of the regrowth ensures that the regrown layer is of good crystalline quality and is smooth for the subsequent growth of the heavily doped top layer. After mesa isolation etching by ICP, S/D electrodes were formed on the n^+-GaN layer using an unalloyed Cr/Au contact. The distance between the S/D metal electrodes (L_{SD}) was 4 μm [Fig. 3(e)]. Then, the sample was spin-coated with a layer of BCB and cured in a vacuum oven at 250 °C. The curing time was 2 h, including 30 min for the temperature ramping. The cured BCB film is able to provide sufficient mechanical support for the following T-shaped metal gate [Fig. 3(f)]. After curing, the BCB was etched back using an RIE process to expose the SiO_2 dummy gate [Fig. 3(g)]. Finally, the dummy gate was removed by BOE and replaced with a Ni/Au metal gate. The gate head of the T-shaped metal gate was 1.5 μm, defined by photolithography [Fig. 3(h)].

The sustainability of the *in situ* SiN_x gate dielectric to the BOE is of great importance for this gate-last self-aligned process, since the SiO_2 dummy gate has to be completely removed using the BOE. The etch rate of *in situ* SiN_x by BOE was found to be extremely slow [31], which is attributed to the high growth temperature (1145 °C) in our experiment. We observed no obvious degradation on the *in situ* SiN_x surface even after a 10-min immersion in the BOE. In addition, RT Hall measurements for three samples before and after the BOE immersion were performed. As shown in Fig. 4, the R_{sh} remains the same for all three samples, indicating that the *in situ* SiN_x gate dielectric is highly resistive to BOE. The PECVD SiN_x sidewall spacers, grown at low temperature (300 °C), could be densified during the high-temperature S/D regrowth process. Therefore, they are also able to withstand the BOE wet etching.

Fig. 5(a) shows the microphotograph of a patterned 50-μm SiO_2 dummy gate with transparent photoresist on top. Fig. 5(b) shows the top-view and cross-sectional scanning electron microscopy (SEM) images of the gate region for

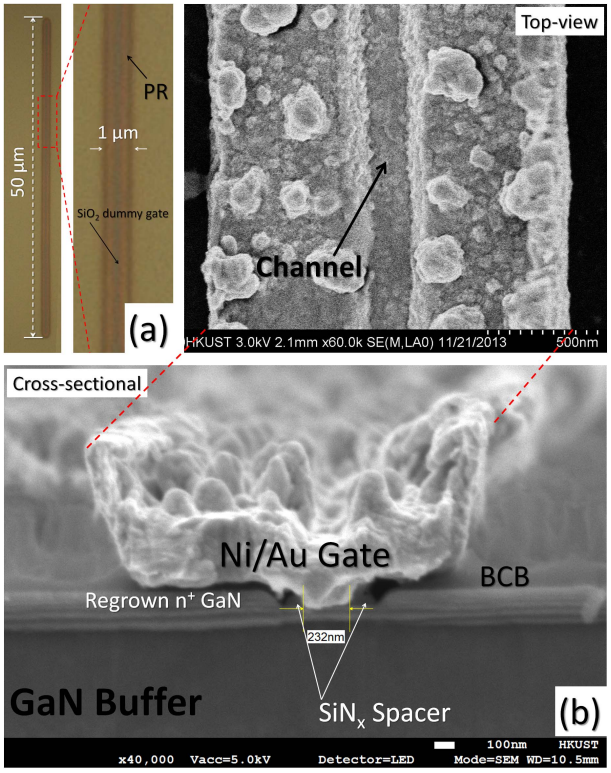

Fig. 5. (a) Microphotograph of a patterned 50-μm SiO_2 dummy gate with transparent photoresist on top [corresponding to Fig. 3 (a)]. (b) Cross-sectional and top-view SEM images for the gate region of a fabricated MISHEMT.

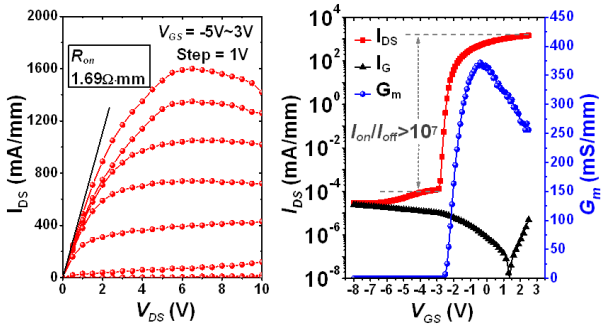

Fig. 6. DC output and transfer characteristics of the MISHEMT with $L_G = 0.23$ μm and $W_G = 2 \times 50$ μm.

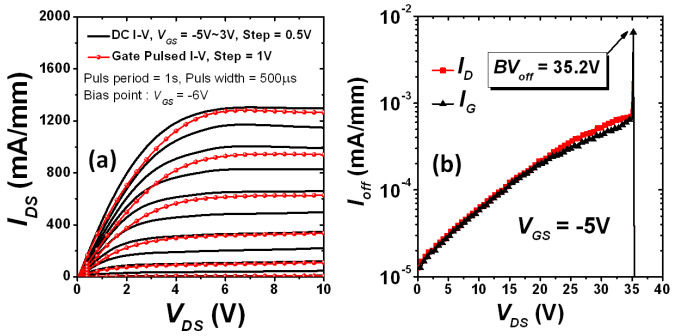

Fig. 7. (a) Gate pulsed and dc output characteristics of the MISHEMT with $L_G = 0.58$ μm and $W_G = 50$ μm. (b) Three-terminal OFF-state breakdown characteristics of the MISHEMT at $V_{GS} = -5$ V.

a fully fabricated device. Due to the poor etch conditions in the BCB planarization process, both the supporting layer and the gate head in the device show high roughness. However, a smooth surface can be achieved by carefully optimizing the BCB etch conditions. The L_{GS} and L_{GD}, defined by the SiN_x sidewall spacers, are both 90 nm. The thickness of the BCB supporting layer is ~100 nm. The regrown n^+-GaN shows a smooth surface morphology, with an rms value of 0.38 nm across a 5-μm × 5-μm scanned area measured by AFM. The metal/n^+-GaN contact resistance and the sheet resistance of the n^+-GaN are 0.313 $\Omega \cdot$ mm and 157 $\Omega/\square$, respectively, as determined by transmission line method measurements. However, the S/D contact resistance in this paper is relatively high [13] and further improvement can be made by optimizing the regrowth conditions.

IV. Device Results and Discussion

On-wafer dc and RF characterizations of the MISHEMTs were performed at temperatures ranging from RT to 550 K. A high-temperature probe station with a thermal controller to adjust and hold the temperature was used. The measurements were carried out in air ambient. Before each measurement, the temperature was held constant for 5 min for thermal stabilization. S-parameter measurements were carried out in the frequency range of 0.1–39 GHz using an Agilent PNA network analyzer. The system was calibrated with a short-open-load-through calibration standard substrate at RT. On-wafer open and short pads were used to deembed the parasitic pad capacitances and inductances from the measured S-parameters at each measurement temperature.

A. DC and RF Characteristics at RT

Fig. 6 shows the RT dc characteristics of the 0.23-μm gated MISHEMT with a gate width (W_G) of 2 × 50 μm. The device exhibited a high maximum I_{DS} of 1600 mA/mm at $V_{DS} = 6$ V and $V_{GS} = 3$ V, and the R_{ON} was as low as 1.69 $\Omega \cdot$ mm. The peak G_m was 372 mS/mm at $V_{DS} = 6$ V and $V_{GS} = -0.5$ V. The achieved results are mainly attributed to the reduction of access resistance by the heavily doped S/D regrowth, as well as the scaled self-aligned L_{GS}/L_{GD}. Moreover, the device presented both gate leakage and OFF-state drain leakage below 10^{-4} mA/mm at $V_{GS} = -8$ V and $V_{DS} = 6$ V, resulting in a large I_{ON}/I_{OFF} of over 10^7. The pulsed output characteristics were performed on a 0.58-μm gated MISHEMT with a W_G of 50 μm, as shown in Fig. 7(a). A 500-μs pulsed voltage was applied to the gate with the base voltage kept at −16 V (quiescent bias at pinchoff condition). It can be seen that the pulsed measurement shows little current degradation. These results indicate that the high-quality *in situ* SiN_x was very effective in suppressing the leakage current and passivating the AlN surface. The three-terminal OFF-state breakdown characteristics of the gate-last self-aligned MISHEMTs at $V_{GS} = -5$ V are plotted in Fig. 7(b). The device with $L_{GD} = 90$ nm features a high breakdown voltage (BV_{OFF}) in excess of 35 V. The BV_{OFF} is limited by catastrophic gate–drain breakdown.

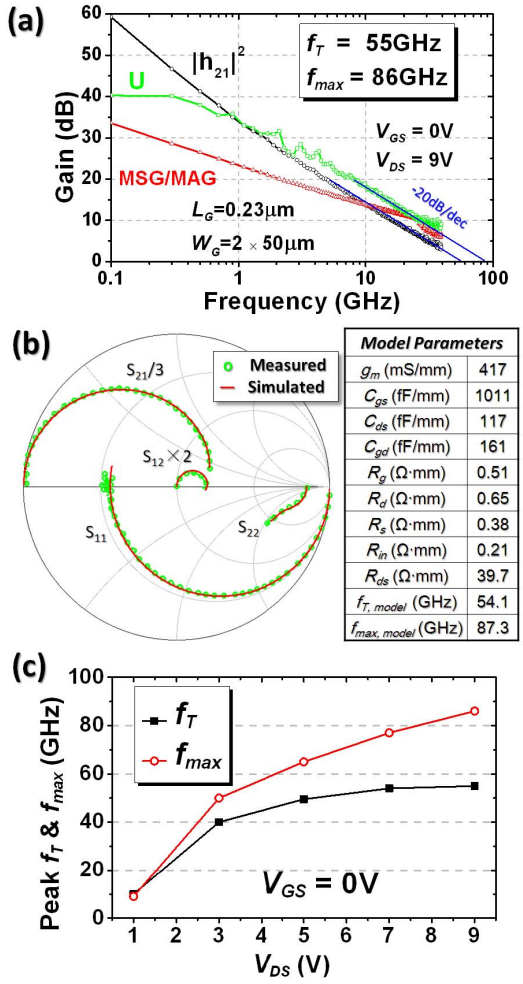

Fig. 8. (a) Small signal RF characteristics of the MISHEMT with $L_G = 0.23$ μm and $W_G = 2 \times 50$ μm showing peak $f_T/f_{\max}$ of 55/86 GHz. (b) Smith chart of measured and simulated RF data and the table with the model parameters for the device. (c) f_T and $f_{\max}$ as a function of $V_{\rm DS}$ for the MISHEMT with $L_G = 0.23$ μm and $W_G = 2 \times 50$ μm.

The large breakdown voltage is mainly attributed to the field plate effects of the big gate head and the greatly reduced gate leakage current using a high-quality *in situ* SiN_x gate dielectric.

Fig. 8(a) shows the RF characteristics of the 0.23-μm gated device measured at maximum f_T bias condition ($V_{\rm DS} = 9$ V, $V_{\rm GS} = 0$ V) at RT. Simultaneously high $f_T/f_{\max}$ of 55/86 GHz were obtained by extrapolating the current gain ($|h_{21}|^2$) and unilateral power gain (U), respectively, using a -20 dB/decade slope. Small-signal equivalent circuit model elements of the MISHEMT were extracted from the measured S-parameters [14], as shown in Fig. 8(b). The Smith chart shows an excellent agreement between the simulation and measurement data, confirming the measured f_T and $f_{\max}$ values. The f_T and $f_{\max}$ as a function of $V_{\rm DS}$ for the measured 0.23-μm gated device are plotted in Fig. 8(c). The f_T continuously increases with $V_{\rm DS}$ until reaching a maximum value at $V_{\rm DS} = 7$ V. This suggests that the drain depletion length, and therefore, the drain delay, which typically increase with $V_{\rm DS}$, were suppressed in this self-aligned architecture [2], [13].

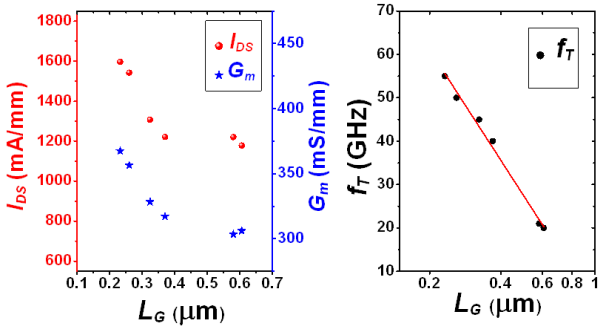

Fig. 9. Scaling behavior of $I_{\rm DS}$, G_m, and f_T with respect to L_G for the self-aligned gate-last MISHEMTs.

Fig. 9 plots the typical scaling behavior of $I_{\rm DS}$, G_m, and f_T with respect to L_G for the gate-last self-aligned MISHEMTs. The best $f_T \times L_G$ product obtained from a 0.32-μm gated device was 14.6 GHz $\cdot$ μm, which is among the best reported values for state-of-the-art GaN HEMTs. In particular, f_T drops linearly with $1/L_G$, revealing the resistance of this gate-last self-aligned architecture to the parasitic effects, which usually get worse at small device dimensions. However, the gate-last self-aligned devices in this first demonstration are yet to be fully scaled. The shrinkage in gate length is limited by the currently used photolithography technique. As a result, there are a significant gate transit delay due to large parasitic components in the devices resulting from the relatively large L_G and $L_{\rm SD}$, as well as the big gate head. To further scale down the device dimensions, e-beam lithography and a single step dry etch process are required to define and pattern the SiO_2 dummy gate. In addition, the gate head and $L_{\rm SD}$ have to be downscaled correspondingly.

The T-gate geometry, including the gate stem height and the gate head dimension, requires careful optimization for a deeply scaled device, since the gate capacitance has a great impact on the RF performance [2], [9]. Due to the relatively high permittivity surrounding the gate, devices fabricated using a self-aligned approach would unfortunately have a larger parasitic gate fringing capacitance than the conventional T-gate structure whose gate is surrounded by air. However, the dielectric layer not only passivates the semiconductor surface but also provides mechanical support to the gate head. These unique features are beneficial to the device reliability and the subsequent interconnection architecture. Even when L_G scales down to 30 nm for an optimized gate geometry, the extra gate fringing capacitance induced by the dielectrics surrounding the gate is still not the major factor impacting the device performance. It has been reported that the f_T for the devices with a relatively high-κ SiN_x or SiON layer surrounding the gate was only $\sim$23% lower than that of the devices with the gate surrounding dielectrics removed [5], [8]. One can expect that carefully optimizing the gate geometry and using low-κ dielectrics under the gate head can further reduce the parasitic gate fringing capacitance. Therefore, the proposed gate-last self-aligned technology using the low-κ BCB in this paper would be an alternative technology balancing the device performance, reliability, and process complexity.

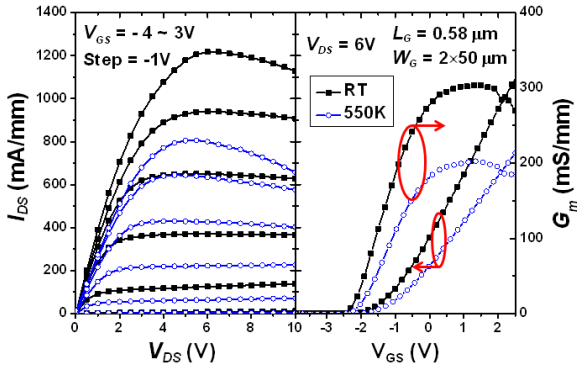

Fig. 10. DC output and transfer characteristics of the MISHEMT with $L_G = 0.58$ μm and $W_G = 2 \times 50$ μm at RT and 550 K.

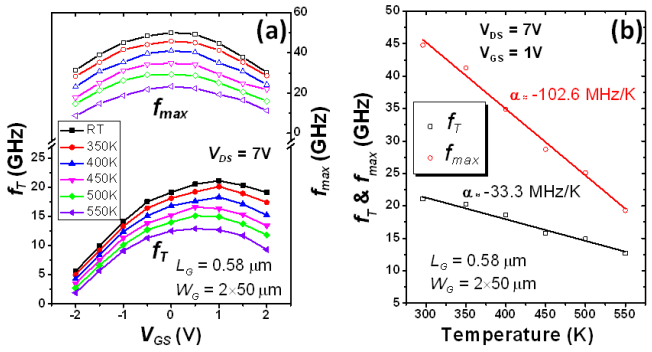

Fig. 11. (a) Thermal evolutions of f_T and $f_{\max}$ as a function of V_{GS} at $V_{DS} = 7$ V. (b) Dependences of f_T and $f_{\max}$ on the ambient temperature at $V_{GS} = 1$ V at $V_{DS} = 7$ V.

B. Thermal Evolution of Device Performance

To investigate the influence of temperature on the device performance, high-temperature dc and RF measurements were performed for a 0.58-μm gated gate-last self-aligned MISHEMT with a W_G of 2×50 μm. Fig. 10 shows the measured dc output and transfer characteristics at RT and 550 K. The maximum I_{DS} and peak G_m values are reduced by ~33% when the temperature is raised from RT ($I_{DS} = 1220$ mA/mm and $G_m = 303$ mS/mm) to 550 K ($I_{DS} = 810$ mA/mm and $G_m = 202$ mS/mm), mainly due to the decrease in the electron mobility and drift velocity [26]–[28].

The thermal evolutions of f_T and $f_{\max}$ as a function of V_{GS} at $V_{DS} = 7$ V are shown in Fig. 11(a). From RT to 550 K, the maximum f_T (at $V_{GS} = 1$ V at $V_{DS} = 7$ V) drops linearly, from 21.1 to 12.7 GHz, with temperature at a temperature dependent rate (α) of -33.3 MHz/K, as shown in Fig. 11(b). This value is lower than the previously reported results (~ -46 MHz/K) for the conventional T-gate AlGaN/GaN HEMTs on SiC [26], indicating the superior thermal stability of the gate-last self-aligned *in situ* SiN_x/AlN/GaN MISHEMTs in this paper. A similar phenomenon is also observed for $f_{\max}$, which drops from 44.8 GHz at RT to 19.3 GHz at 550 K with $\alpha \approx -102.6$ MHz/K. In addition, no obvious performance degradation was found for the MISHEMT after the high-temperature measurements. The reduced temperature sensitivity of the gate-last self-aligned device is mainly attributed to the introduction of regrown n^+-GaN in the access region, which is nearly independent of temperature [12].

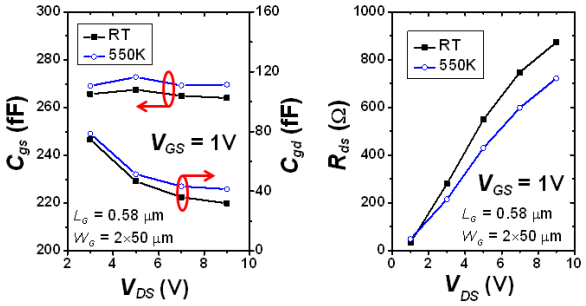

Fig. 12. Thermal dependences of C_{gs}, C_{gd}, and R_{ds} as a function of V_{DS}.

Interestingly, when the temperature was raised from RT to 550 K, both f_T and $f_{\max}$ showed more severe degradation (~40% and ~57%, respectively) than I_{DS} and G_m (~33%). This phenomenon is probably related to the change of intrinsic capacitances (C_{gs} and C_{gd}) and resistance (R_{ds}) with temperature. C_{gs}, C_{gd}, and R_{ds} directly affect the device's RF performances, since $f_T \approx g_m/[2\pi \cdot (C_{gs} + C_{gd})]$ and $f_{\max} \approx f_T \cdot (R_{ds}/4R_g)^{1/2}$. As shown in Fig. 12(a), both C_{gs} and C_{gd} show a slight increase with temperature. This may be explained by the changes in material permittivity and the structure deformations induced in the passivation and channel layers at high temperature [32], [33]. On the other hand, the dependence of R_{ds} on temperature is opposite [Fig. 12(b)], which may be related to a lower 2-DEG confinement at high temperature. Therefore, the relatively high reduction of f_T and $f_{\max}$ at high temperature can be clearly explained.

V. Conclusion

In this paper, the use of *in situ* grown SiN_x as a gate dielectric and as device passivation for AlN/GaN MISHEMTs has been described and discussed. A scalable gate-last self-aligned technology has been developed for MISHEMT fabrication. The submicrometer gated devices featuring scaled self-aligned L_{GS}/L_{GD} and a low-κ BCB supporting layer under the gate head exhibited respectable dc and RF performances. In addition, we have studied the effect of temperature on the dc and RF performances of the gate-last self-aligned MISHEMTs. The thermal behavior of their main parameters were also extracted and discussed, which can provide feedback for further device optimization. The achieved results in this paper suggest the potential of the gate-last self-aligned *in situ* SiN_x/AlN/GaN MISHEMTs for future high-frequency power applications.

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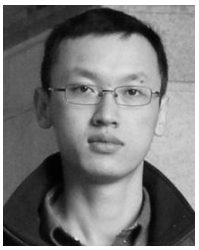

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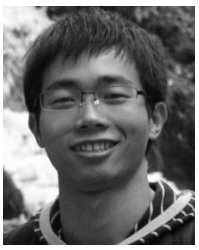

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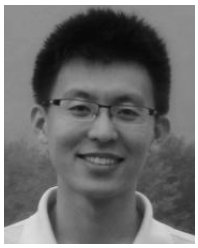

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