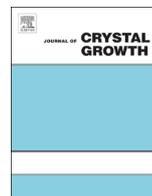




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# MOVPE growth of *in situ* SiN<sub>x</sub>/AlN/GaN MISHEMTs with low leakage current and high on/off current ratio



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## ABSTRACT

We report the MOVPE growth of high-performance AlN/GaN MISHEMTs using regrown n-type GaN (n-GaN) as source/drain (S/D) and *in situ* SiN<sub>x</sub> as gate dielectric. The n-GaN S/D and *in situ* SiN<sub>x</sub> were investigated for minimizing on-resistance and suppressing gate leakage current, respectively. The results showed that a two-step Si doping profile for the n-GaN greatly reduced the access resistance, and small gate leakage as well as low trap state density were achieved with the *in situ* SiN<sub>x</sub> gate dielectric. The fabricated 0.33 μm-gated MISHEMT exhibited a maximum drain current density of 1550 mA/mm and an on/off current ratio over 10<sup>7</sup>.

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## 1. Introduction

GaN-based high electron mobility transistors (HEMTs) have attracted great attention for radio frequency/microwave power applications, due to their high-density two-dimensional electron gas (2DEG), high breakdown field strength and high electron saturation velocity [1–3]. Nowadays innovative device scaling is being intensively studied for GaN-based HEMTs and remarkable progress has been presented [4,5]. As the gate length scales, reducing gate-to-channel distance is desirable to mitigate the short channel effect [6,7]. AlN/GaN HEMTs are promising because of a unique combination of high-density 2DEG and ultra-small barrier thickness (< 7 nm) [8,9]. Recently great progress has been achieved and AlN/GaN heterostructures with remarkable channel transport characteristics have been demonstrated [10,11].

Despite the great potential of AlN/GaN heterostructures, there are a few obstacles impeding the development of high-performance AlN/GaN HEMTs. First, it is difficult to achieve low contact resistance to the 2DEG channel due to the high potential barrier of AlN, leading to a large on-resistance [12]. Regrown n-GaN as S/D has been shown efficient in reducing the on-resistance, yet the report about the relationship between the regrowth conditions and device characteristics is rare [13–15]. Second, a metal-insulator-semiconductor (MIS) structure is typically adopted for AlN/GaN HEMTs due to the defective and thin AlN barrier layer, but most of the gate dielectrics are *ex situ* deposited and can potentially introduce process-related

contaminations/defects [16]. Compared with the *ex situ* dielectrics, SiN<sub>x</sub> can be *in situ* deposited by MOVPE and is effective in passivating AlN/GaN heterostructure for enhanced channel conductivity as well as low interface trap states, making it an ideal candidate as the gate dielectric for AlN/GaN MISHEMTs [17–19]. However, reports on successful use of the *in situ* SiN<sub>x</sub> as the gate dielectric for the AlN/GaN MISHEMTs are still limited [20,21].

In this work, we present the growth of high-performance *in situ* SiN<sub>x</sub>/AlN/GaN MISHEMTs with regrown n-GaN S/D. Both material growth and device architecture of the MISHEMTs were engineered for improved device performance. Different doping concentrations/profiles for the regrown n-GaN S/D were investigated for minimizing the access-resistance. SiN<sub>x</sub> *in situ* grown by MOVPE was adopted as the gate dielectric, and its impact upon the device performance was presented and analyzed. The sub-micron gated AlN/GaN MISHEMTs were fabricated, exhibiting high drain current density and large on/off current ratio.

## 2. Experimental procedure

The samples presented in this work were grown with an Aixtron 2000HT MOVPE system. Trimethylgallium (TMGa), trimethylaluminum (TMAI), silane (SiH<sub>4</sub>) and ammonia (NH<sub>3</sub>) were used as precursors for Ga, Al, Si and N, respectively. H<sub>2</sub> and N<sub>2</sub> were used as carrier gases. Atomic force microscopy (AFM), scanning electron microscopy (SEM), transmission electron microscopy (TEM), high-resolution x-ray diffraction (XRD), room-temperature Hall effect measurement and transmission line model (TLM) were implemented for characterization of the samples.

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To study the impact of Si doping upon the regrown n-GaN S/D, samples A–E with different doping concentrations and profiles were regrown on patterned AlGaN/GaN templates with semi-insulating buffer layers, as shown in Fig. 1(a). The templates are standard HEMT epi grown by MOVPE and consisted of a 20 nm  $\text{Al}_{0.3}\text{Ga}_{0.7}\text{N}$  barrier, an 1 nm AlN spacer, a 875 nm unintentionally doped GaN (u-GaN) layer and a 1.2  $\mu\text{m}$  buffer layer. Details about the structure and growth conditions of the templates can be found elsewhere [22]. 300 nm  $\text{SiO}_2$  was deposited by plasma-enhanced chemical vapor deposition (PECVD) and patterned using wet etching, to define and mask the gate area for following  $\text{Cl}_2$ -based inductively coupled plasma (ICP) etching. The pre-regrowth etch depth into the buffer was approximately 120 nm. Then, n-GaN S/D was regrown on the templates by MOVPE at 1090 °C, without any surface treatment before the regrowth. After that, the  $\text{SiO}_2$  was removed and Ti/Al/Ni/Au (20/150/50/80 nm) ohmic contacts were formed by e-beam evaporation. Two kinds of TLM patterns were used and named as n-GaN and n-GaN and 2DEG, as shown in Fig. 1(b) and (c), respectively.

Samples F and G were *in situ*  $\text{SiN}_x$ /AlN/GaN heterostructures sharing the same 2.5 nm AlN barrier layer but *in situ*  $\text{SiN}_x$  layers with different thickness (3 and 7 nm for sample F and G, respectively), as shown in Fig. 1(d). More details about the AlN/GaN heterostructure can be found elsewhere [23]. The *in situ*  $\text{SiN}_x$  was deposited immediately following the AlN/GaN growth in the MOVPE chamber at 1145 °C and 100 mbar. MIS diodes were fabricated using samples F and G. The process started with mesa etching using a  $\text{CF}_4/\text{O}_2$ -based reactive ion etching (RIE) followed by an ICP etching. After selective removal of the *in situ*  $\text{SiN}_x$  in S/D region, Ti/Al/Ni/Au (20/150/50/80 nm) was deposited by e-beam evaporation and annealed at 850 °C in  $\text{N}_2$  ambient to form ohmic contact. Ni/Au (20/200 nm) gate was formed with a diameter of 200  $\mu\text{m}$  on the *in situ*  $\text{SiN}_x$  by e-beam evaporation and a lift-off process. Gate leakage currents as well as the capacitance–voltage (C–V) characteristics of the MIS diodes were then measured and discussed.

After the investigation of S/D regrowth and *in situ*  $\text{SiN}_x$  gate dielectric, sample H was grown on a 2-in. (0 0 0 1) sapphire substrate by MOVPE for MISHEMTs fabrication. As shown in Fig. 2(a), the

sample consisted of, from bottom to up, a 35 nm AlN nucleation layer, a 300 nm AlN buffer layer and a 2.7  $\mu\text{m}$  u-GaN layer, a 2.5 nm AlN barrier layer and a 7 nm *in situ*  $\text{SiN}_x$  layer. The  $\text{NH}_3$  flow rate for the first 180 nm AlN buffer layer was 1000 sccm and 3500 sccm for the following 120 nm AlN, while the temperature and pressure were kept constant at 1145 °C and 100 mbar, respectively. This is designed for engineering of the buffer resistivity and dislocation density. The 2.5 nm AlN barrier layer was not specifically optimized and was directly grown on the u-GaN layer at 1145 °C and 100 mbar with a  $\text{NH}_3$  flow rate of 3500 sccm. MISHEMTs were fabricated with a gate-last self-aligned process [24]. First, 300-nm-thick  $\text{SiO}_2$  was deposited by PECVD and patterned using a two-step dry and wet etching. Subsequently a layer of PECVD  $\text{SiN}_x$  was blanket deposited (Fig. 2(b)). An anisotropic RIE etching was then implemented to form sidewall spacers and S/D regions were exposed by ICP etching (Fig. 2(c)). The ICP etch depth was about 90 nm. After that, n-GaN was regrown on the exposed GaN buffer and, after mesa isolation etching, S/D electrodes were formed on the regrown layer using Cr/Au (Fig. 2(d)). Then the sample was spin-coated with a layer of low- $\kappa$  BCB material and cured in a vacuum oven at 250 °C, followed by RIE etch back to expose the  $\text{SiO}_2$  dummy gate (Fig. 2(e) and (f)). Finally, the dummy gate was removed with buffered oxide etching (BOE) and replaced with a Ni/Au metal gate (Fig. 2(g) and (h)). The gate head of the T-shaped gate was 1.5  $\mu\text{m}$ , defined by photolithography. The thickness of the BCB supporting layer was about 100 nm and the gate-to-source/gate-to-drain distance ( $L_{\text{GS}}/L_{\text{GD}}$ ) was 90 nm. Device performance of the MISHEMTs was finally characterized and presented.

### 3. Results and discussion

To achieve highly conductive n-GaN as S/D, the first step is to choose a proper Si doping concentration ( $N_c$ ). Samples A and B shared the same structure containing  $\sim 180$  nm regrown n-GaN layer but differentiated Si doping. The  $N_c$  for sample A and B was about  $5 \times 10^{19}$  and  $7 \times 10^{19} \text{ cm}^{-3}$ , respectively. Surface morphology of the two samples was characterized by AFM, as shown in Fig. 3(a) and (b). Notably, sample A presents smooth surface with a root-mean-square

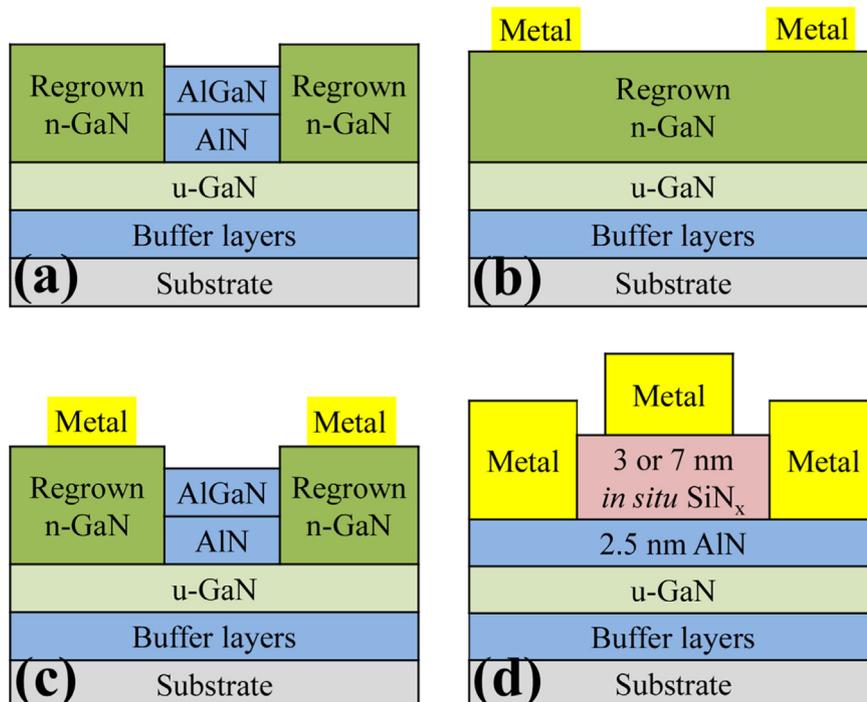


Fig. 1. Cross-sectional schematics of (a) sample A–E, (b) TLM pattern named n-GaN, (c) TLM pattern named n-GaN and 2DEG and (d) sample F–G.

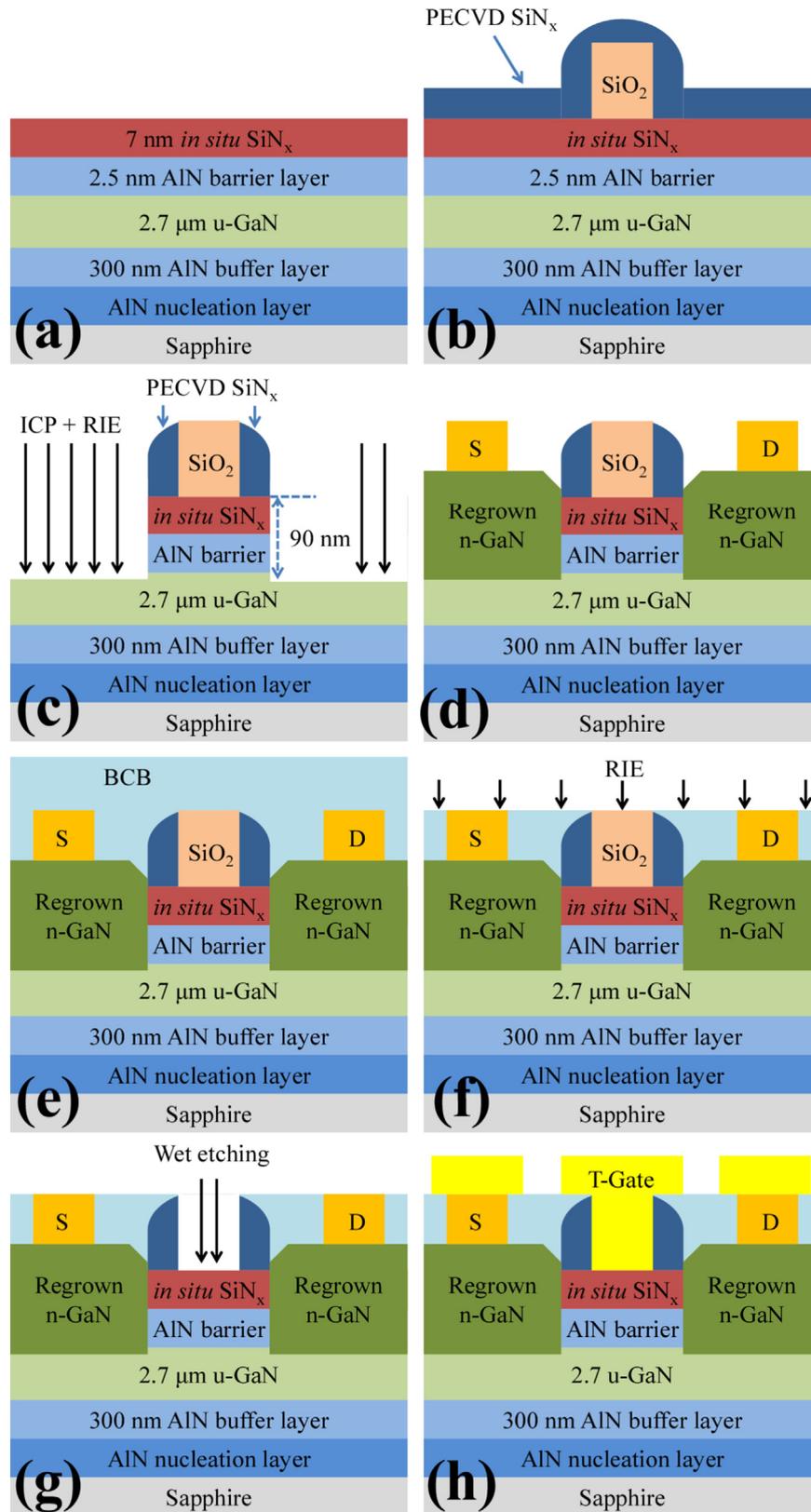


Fig. 2. Process flow of the gate-last self-aligned process.

(RMS) roughness value as small as 0.4 nm. However, sample B exhibits high-density pits on surface, whose depth can be close to the thickness of the regrown n-GaN layer. Such deep pits are probably caused by high Si doping or SiH<sub>4</sub> exposure as reported by some groups [25,26]. The pits are undesirable because they can degrade the contact

between the regrown n-GaN and the 2DEG channel by reducing the contact area when they locate at the n-GaN/channel boundary.

Additionally, samples C and D (containing ~190 nm n-GaN) with  $N_c$  of about  $2 \times 10^{19}$  and  $5 \times 10^{19} \text{ cm}^{-3}$ , respectively, were characterized with TLM methods and the results were listed in

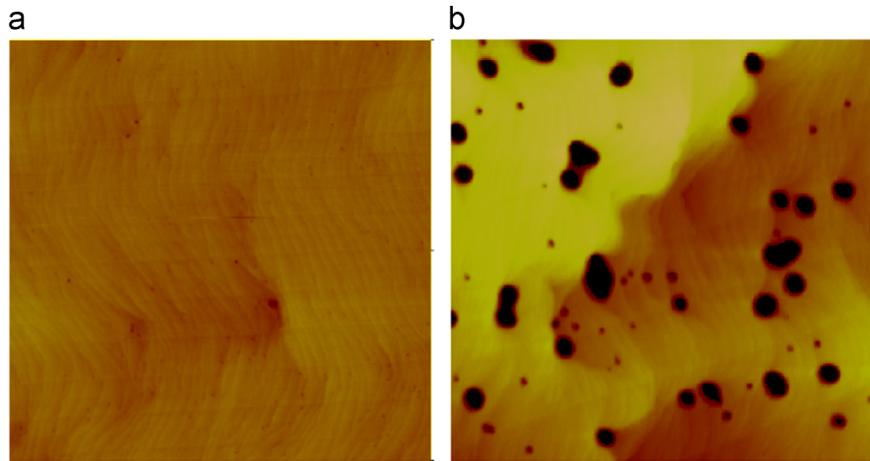


Fig. 3. AFM observation of sample A and B across a scan area of  $5 \times 5 \mu\text{m}^2$ . The vertical scale is 10 nm.

Table 1

Sheet resistances and contact resistances of sample C–E obtained from the TLM measurement.

Sample	n-GaN $R_{sh}$ ( $\Omega/\text{sq}$ )	Metal-to-n-GaN $R_{c1}$ ( $\Omega \text{ mm}$ )	2DEG-to-n-GaN $R_{c2}$ ( $\Omega \text{ mm}$ )
C	256	4.19	0.19
D	85	0.23	1.43
E	165	0.17	0.07

Table 1. As compared to sample C, the contact resistance between the Ti/Al/Ni/Au metal and the regrown n-GaN ( $R_{c1}$ ) of sample D is reduced with increased n-GaN carrier concentration. However, the contact resistance between the 2DEG channel and the n-GaN ( $R_{c2}$ ) for sample D is larger than that of sample C. To explore this phenomenon,  $I$ – $V$  characteristics between two contacts were measured for samples C and D, as presented in Fig. 4. The contact spacing in the measurement was  $2 \mu\text{m}$ . It can be observed that, the Schottky current dominates at low voltage region for sample C, indicating the insufficient  $N_c$  for the regrown n-GaN S/D. With more Si doping, conductivity of the n-GaN is improved for sample D and the current correspondingly increases. But it is noticeable that the saturated current of sample D (n-GaN and 2DEG TLM pattern) is obviously smaller than that of sample C. This can be caused by the intensified electron scattering at the n-GaN/2DEG channel interface with increased Si doping [27,28]. Heavy Si doping at early stages of the regrowth can introduce defects at the n-GaN/channel interface by either  $\text{SiH}_4$  etching or over doping. To resolve this problem, a two-step doping profile was adopted for sample E. The n-GaN thickness for sample E was about 150 nm, and  $N_c$  was adjusted to be  $\sim 2 \times 10^{19} \text{ cm}^{-3}$  of the first 30 nm n-GaN while kept constant as  $\sim 5 \times 10^{19} \text{ cm}^{-3}$  for the following 120 nm n-GaN. It can be observed that, the  $R_{c2}$  of sample E is smaller than that of sample D despite its overall reduced Si doping (Table 1). This can be attributed to the improved crystalline quality of the n-GaN/channel interface which reduces the possibility of electron scattering.

After optimizing the n-GaN regrowth, the *in situ*  $\text{SiN}_x$  was studied to minimize the leakage current and trap states density of the AlN/GaN MIS structure. MIS diodes were fabricated using samples F and G, which had 3 and 7 nm *in situ*  $\text{SiN}_x$  as the gate dielectric, respectively. Gate leakage currents and 100 kHz double mode  $C$ – $V$  characteristics of the two samples are plotted in Fig. 5. It can be observed that, with increasing  $\text{SiN}_x$  thickness, the gate leakage current is reduced by more than two orders of magnitude

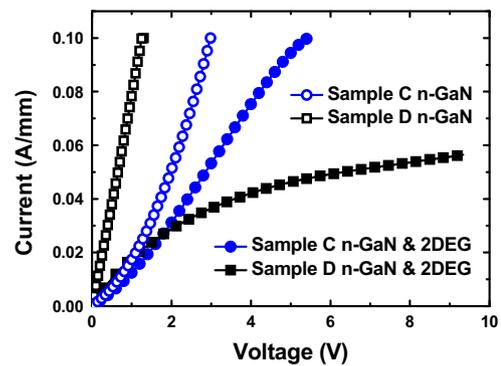


Fig. 4.  $I$ – $V$  characteristics of the sample C and D measured with an electrode spacing of  $2 \mu\text{m}$ .

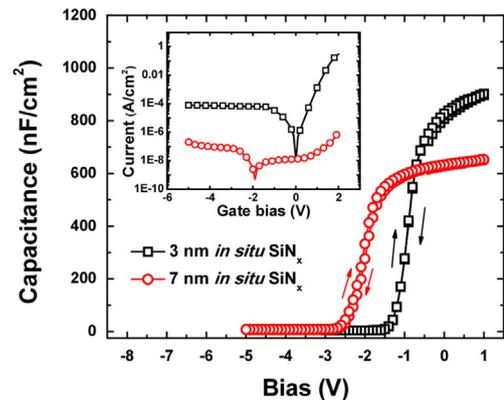


Fig. 5. Double mode  $C$ – $V$  characteristics and leakage currents of the MIS diodes fabricated using sample F and G.

when comparing sample F and G. For sample G with 7 nm *in situ*  $\text{SiN}_x$ , the gate leakage current is close to  $10^{-7} \text{ A/cm}^2$ , which is smaller than the similar MIS structures using other dielectrics [29–33]. In addition to the leakage current, trap state density also has great impact upon the device performance. From the double mode  $C$ – $V$  characteristics, it can be observed that the two samples both exhibit negligible clock wise hysteresis, indicating preminent quality of the *in situ*  $\text{SiN}_x$  and the  $\text{SiN}_x/\text{AlN}$  interface. Previous study has found that the hysteresis is caused by acceptor-like trap states either in the dielectrics or at the dielectric/semiconductor interface [34]. Due to the high-temperature *in situ* growth, the AlN surface is not exposed to the air before the  $\text{SiN}_x$  deposition and the adatom

mobilities were improved during the  $\text{SiN}_x$  growth, resulting in high-quality  $\text{SiN}_x$  and  $\text{SiN}_x/\text{AlN}$  interface.

The XRD GaN (0 0 2) and (1 0 2) full width at half maximum of sample H was measured to be 231 and 449 arcsec, respectively, indicating good crystalline quality of the GaN buffer layer. With room-temperature Hall effect measurement, the sheet resistance of sample H is found to be  $546 \Omega/\text{sq}$ , which is consistent with recent reported values and shows good channel conductivity [18]. The 2DEG concentration is  $1.5 \times 10^{13}/\text{cm}^2$  with an electron mobility of about  $762 \text{ cm}^2/\text{V s}$ . The relatively low mobility can be caused by the unoptimized growth of the AlN barrier layer and will be improved in future work. Fig. 6(a) presents the cross-sectional TEM images of the gate stack of sample H. The images were taken near the GaN [1 -1 0 0] zone axis. An abrupt *in situ*  $\text{SiN}_x/\text{AlN}$  interface can be observed, while a rough interface typically appears in the III-N MIS devices with *ex situ* gate dielectrics which may degrade the interface quality [35,36]. Surface morphology of the sample was also characterized with AFM and the result was shown in Fig. 6(b). Smooth surface can be observed and a RMS value as small as 1.06 nm was achieved.

DC characteristics of the self-aligned MISHEMT with a gate length of about  $0.33 \mu\text{m}$  and gate width of  $2 \times 50 \mu\text{m}$  were plotted in Fig. 7. The device exhibits a high maximum drain current density ( $I_{\text{DS}}$ ) of  $1550 \text{ mA/mm}$  at  $V_{\text{DS}}=5 \text{ V}$  and  $V_{\text{GS}}=3 \text{ V}$ , and the on-resistance is as low as  $1.89 \Omega \text{ mm}$ . The peak transconductance ( $G_{\text{m,peak}}$ ) is  $330 \text{ mS/mm}$  at  $V_{\text{DS}}=6 \text{ V}$  and  $V_{\text{GS}}=-0.3 \text{ V}$ . The achieved results are mainly attributed to the reduced access resistance by the highly conductive regrown n-GaN S/D and the scaled gate-to-source/gate-to-drain distance. Furthermore, gate leakage and off-state drain leakage currents of the device are both below  $10^{-4} \text{ mA/mm}$  at  $V_{\text{GS}}=-8 \text{ V}$  and  $V_{\text{DS}}=6 \text{ V}$ , leading to a large on/off current ratio over  $10^7$  with a small subthreshold slope of  $100 \text{ mV/dec}$ . This indicates that the *in situ* grown  $\text{SiN}_x$  is of high quality and is very effective in reducing the leakage current and passivating the AlN surface.

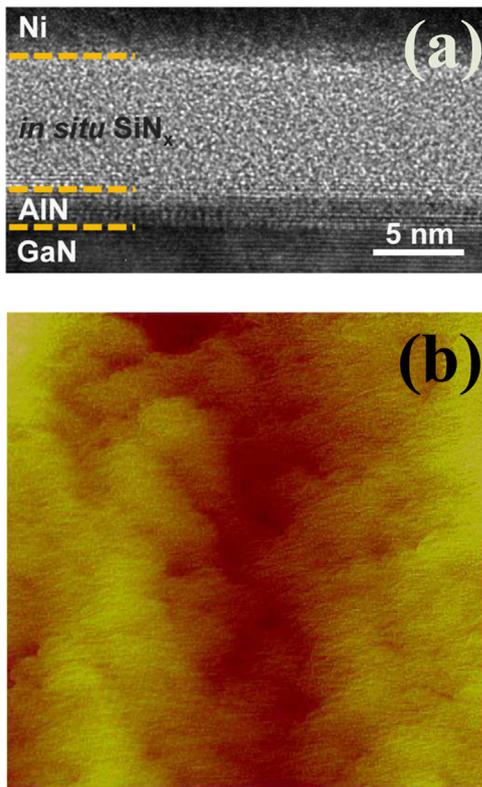


Fig. 6. (a) Cross-sectional TEM and (b) AFM observations of sample H.

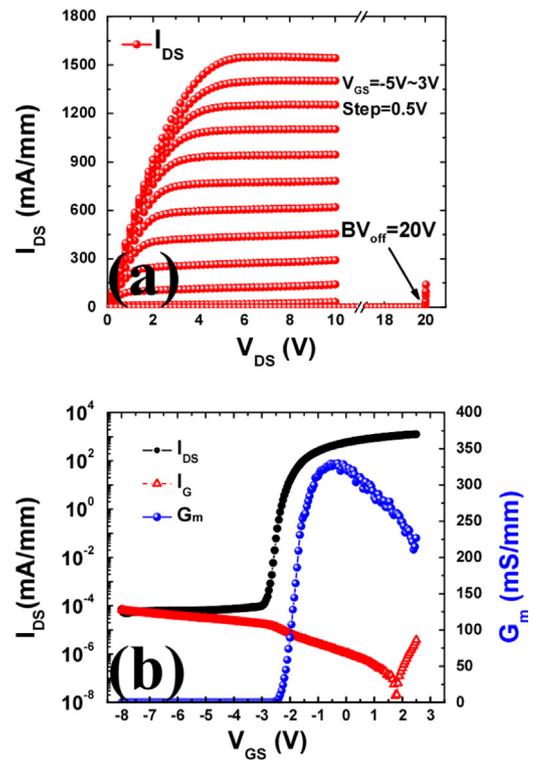


Fig. 7. (a) Output and (b) transfer characteristics of the *in situ*  $\text{SiN}_x/\text{AlN}/\text{GaN}$  MISHEMT.

#### 4. Conclusion

In this work, MOVPE growth of high-performance *in situ*  $\text{SiN}_x/\text{AlN}/\text{GaN}$  MISHEMTs with regrown n-GaN S/D was demonstrated. Both material growth and device architecture of the AlN/GaN MISHEMTs were engineered to reduce the device on-resistance and gate leakage current. The regrowth of highly conductive n-GaN S/D were studied with different Si doping concentrations/profiles. A two-step doping profile for the regrown n-GaN was found to be effective in forming both good n-GaN/metal and n-GaN/2DEG contacts. Additionally, gate leakage current was significantly suppressed and low trap state density was achieved with the *in situ*  $\text{SiN}_x$  as gate dielectric. The fabricated AlN/GaN MISHEMT with a gate length of  $0.33 \mu\text{m}$  exhibited a maximum drain current density of  $1550 \text{ mA/mm}$ , on-resistance of  $1.89 \Omega \text{ mm}$  and an on/off current ratio over  $10^7$ .

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