Off-state Drain Leakage Reduction by Post Metallization Annealing for Al₂O₃/GaN/AlGaN/GaN MOSHEMTs on Silicon

Huaxing Jiang, Xing Lu, Chao Liu and Kei May Lau*

Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong *Email: eekmlau@ust.hk

AlGaN/GaN-based high electron mobility transistors (HEMTs) have demonstrated great potential for power switching and high frequency power amplifier applications. Use of Al_2O_3 gate dielectric by atomic layer deposition (ALD) to form metal-oxide-semiconductor HEMTs (MOSHEMTs) has been adopted to block the gate leakage and suppress drain current collapse[1-2]. However, adding an insulator between the gate metal and barrier layer creates an extra dielectric/AlGaN or GaN interface which could be problematic. High density interface states at the dielectric/semiconductor interface can lead to serious surface leakage current [3], leading to an increase of the off-state drain leakage current. In this work, we investigated the effects of post metallization annealing (PMA) on the reduction of I_{off} for $Al_2O_3/GaN/AlGaN/GaN$ MOSHEMTs. It was found that a PMA at 500 °C can reduce the I_{off} by 3 orders of magnitude. A high on/off current ratio of 10^8 and a steep subthreshold swing (SS) of 71 mV/dec were achieved. A reduction in the accumulation capacitance of the MOS capacitor (MOSCAP) after 500 °C PMA revealed partial oxidation of the GaN surface. This suggests that elimination of the conduction path at the Al_2O_3/GaN interface by annealing might be the reason for the significantly reduced I_{off} .

The AlGaN/GaN heterostructure was grown on a 6-inch n-type Si wafer by metal-organic chemical vapor deposition (MOCVD). As shown in Fig.1. (a), the epilayer, from bottom to top, consists of 1.7 μ m graded AlGaN buffer, 1.2 μ m undoped GaN buffer, 1 nm AlN spacer and 30 nm Al_{0.25}Ga_{0.75}N barrier and 2 nm GaN cap. Hall measurements showed a sheet carrier density of 7 × 10¹² cm⁻² and mobility of 1800 cm²V⁻¹s⁻¹. Fig.1. (b) depicts the MOSHEMT fabrication process flow. Device isolation was carried out by BCl₃/Cl₂-based inductively coupled plasma etching. After Ti/Al/Ni/Au alloyed Ohmic contacts formation, followed by O₂ plasma and HCl cleaning, 10 nm Al₂O₃ by ALD at 300 °C was deposited immediately. Finally the Ni/Au gate and contact metal was deposited. After device fabrication, samples were separated into four pieces, with three annealed at 300 °C, 400 °C and 500 °C by rapid thermal annealing (RTA) process in N₂ ambient for 10 min.

Fig.2 shows the drain current and gate leakage current versus gate bias of the fabricated devices. The gate leakage current remained below 10⁻⁶ mA/mm for all the devices with and without PMA. The device without PMA showed an I_{off} of 10⁻² mA/mm at V_{GS} of -8 V and V_{DS} of 6 V. The I_{off} was dominated by the source-to-drain surface leakage. No obvious change of I_{off} was observed for the devices with PMA at 300 °C and 400 °C. I_{off} was reduced by 3 orders of magnitude for the devices with PMA at 500 °C. A high I_{on}/I_{off} ratio of 10⁸ and a sharp SS of 71 mV/dec were achieved. Fig.3 shows the average I_{off} of ten devices on each sample with different PMA conditions. Fig.4 compares the buffer leakage currents for the four samples. Only the sample with PMA at 500 °C showed one order of magnitude reduction in the buffer leakage current, which is believed to be attributed to the elimination of the current path at the Al₂O₃/GaN interface. Fig.5 showed a reduction in the accumulation capacitance of the GaN surface leading to an increase of EOT (equivalent oxide thickness). The oxidation process passivated the N-vacancies and reduced the interface states. Thus the surface leakage current was reduced [4]. As shown in Fig.6, no degradation of the DC/gate pulsed I_D-V_{DS} dispersion was observed for the MOSHEMTs with 500 °C PMA can be explained by the reduced accumulation capacitance.

References

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Fig. 1. (a) Schematic view and (b) process flow of fabricated $Al_2O_3/GaN/AlGaN/GaN$ MOSHEMTs.



Fig. 3. Average off-state drain leakage of ten devices with same size at each PMA condition. I_{off} is determined at $V_{GS} = -8V$ and $V_{DS} = 6V$.



Fig. 5. Capacitance-voltage characteristics of circular MOSCAP without and with various PMAs.



Fig. 2. Drain current and gate leakage current comparison of devices without and with various PMAs at V_{DS} of 6 V.



Fig. 4. Buffer leakage comparison of samples without and with various PMAs. The space between two Ohmic pads is $100 \ \mu m$.



Fig. 6. DC/gate pulsed output characteristics of devices (a) without PMA and (b) with 500 °C PMA. The pulse period is 1 s and pulse width is 500 μ s. Gate pulse base voltage V_{GS0} is -8 V.