III-V-IV INTEGRATION TOWARD ELECTRONICS AND PHOTONICS CONVERGENCE ON A SILICON PLATFORM

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ABSTRACT

Integration of III-V compound semiconductor devices on a Si manufacturing platform represents one of the most topical challenges today. Potentially, such heterogeneous integration can offer numerous opportunities in combining the unique electronic and photonic functionalities of III-V technology with the large volume, low cost and high density Si CMOS technology. Here we review the major challenges and our recent progress in monolithic integration of III-V materials on Si by direct epitaxy and its device applications. Several importance techniques to achieve high crystalline quality III-V semiconductors on Si are presented and their distinct advantages and limitations are discussed.

INTRODUCTION

Historically, III-V and Si technologies have undergone significant research in parallel. After half of a century of explosive development driven by Moore's Law, the downscaling of Si based metal-oxide-semiconductor field effect transistors (MOSFETs) has led to remarkable advancement in transistor density, switching speed and signal processing capability. It is generally recognized that further shrinking of transistor dimensions is running into many technological challenges. Integrating III-V high mobility semiconductors, like InGaAs and InAs, on large-diameter Si substrates for advanced nMOSFETs has emerged as one of the most promising options for transistors beyond 10 nm CMOS technology node [1]. The transistor supply voltage can be aggressively reduced for such energy-efficient nano-scale field effect transistors as a result of the high carrier velocities in these compound semiconductors. Furthermore, the indirect bandgap of Si precludes its use for efficient light emission. Integration of III-V materials with inherent good photonic properties on Si for next generation on-chip optical interconnects is being actively researched [2].

Compared to hybrid integration schemes, monolithic integration of III-V on Si by direct epitaxy is a cost-effective, reliable and wafer-level approach to achieve an ultimate electronic-photonic integrated system on the Si platform. However, the large mismatch in lattice constant and thermal expansion coefficient as well as the difference in crystal polarities make it difficult to grow III-V on Si. In order to manage the resultant high-density defects, we have explored both blanket heteroepitaxy and selective patterned growth of InP and associated heterostructures on Si by metal-organic chemical vapor deposition (MOCVD). Several important growth techniques have been investigated. The crystalline quality of the metamorphic III-V buffer on Si and its suitability for practical device application were characterized. High-performance InGaAs quantum-well (QW) channel MOSFETs with regrown source/drain and high-speed InGaAs photodetectors were demonstrated.

MATERIAL GROWTH AND DEVICE CHARACTERISTICS

Blanket Heteroepitaxy of III-V on Si for Transistors

Motivated by monolithic integration of photonic and electronic devices, heteroepitaxy of III-V on planar Si has been pursued since the 1980s. Recent advances in III-V n-channel transistors for digital integrated circuits have fueled renewed interest in this research field [3]. To accommodate the desired III-V heterostructures on Si to and manage the defects (threading dislocations, stacking faults, micro/nano twins, and antiphase domains) generated through the hetero-growth process, various buffer technologies, such as InP/GaAs [4], AlSb/GaSb/GaP [5], GaAs/Ge [6, 7] and InAlAs/GaAs [8], as well as defect engineering approaches, such as growth on miscut Si [6-8], graded buffer [8], two-step growth method [9], strained supperlattice [10] and thermal annealing, have been investigated. Here, we present our recent progress on MOCVD growth of ultra-high mobility $In_{0.52}Al_{0.48}As/In_xGa_{1-x}As$ ($x \geq 53\%$) heterostructures on the InP/GaAs-on-Si compliant substrates for transistors. The material growth was carried out in an Aixtron AIX-200/4 low-pressure MOCVD system. Four-inch p-type exact Si (001) wafers were used for the experiments. Prior to growth, the Si wafer was cleaned in a boiling NH_4OH: H_2O_2: H_2O (1:1:5) solution, followed by a brief dip in diluted HF solution to remove native oxide. Afterward, the wafer was loaded into the MOCVD chamber, heated up to ~800 °C and annealed for 30 min at 100 mbar in a pure H_2 ambient for thermal desorption. AsH_3 was introduced at the end of the annealing and the reactor was cooled down to the buffer growth temperature. Both GaAs and InP were grown using a two-step procedure: A nucleation layer was first introduced at a relatively low-temperature (LT), in the

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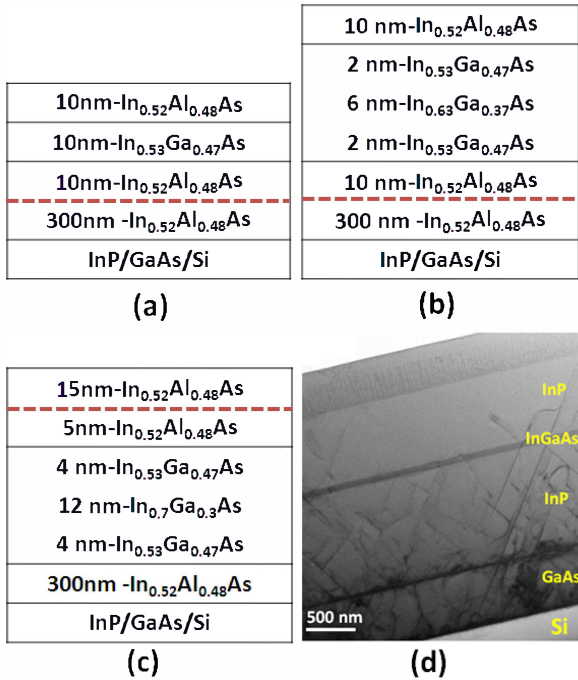

Figure 1: Epi-layer structure for QW-A (a), QW-B (b) and QW (c) and a cross-sectional TEM image of InGaAs QW on Si using InP/GaAs buffer. (Dashed line: Si delta-doping).

surface-reaction limited regime, followed by an overgrowth layer at a typical high temperature (HT), mass-transport limited regime. An InGaAs interlayer was inserted in the HT-InP buffer for dislocation bending and surface smoothing. The detailed growth parameters were reported elsewhere [11]. The 4-inch InP/GaAs/Si template was then cut into quarter wafers for subsequent growth of $In_{0.52}Al_{0.48}As/In_xGa_{1-x}As$ ($x \geq 53\%$) heterostructures. Fig. 1 (a)-(c) illustrate the epi-layer structure for three quantum wells: QW-A, QW-B and QW-C. In QW-A and QW-B, the heterostructure was reversely doped under the $In_{0.52}Al_{0.48}As$ backside spacer. In QW-C, Si delta-doping was inserted above the $In_{0.52}Al_{0.48}As$ upper spacer. An InGaAs step quantum well with higher Indium content in the core layer was used in QW-B and QW-C for mobility enhancement. Van der Pauw Hall measurements were

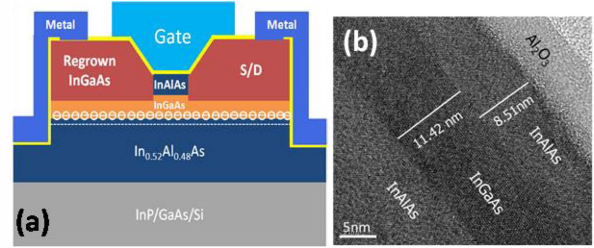

Figure 2: Cross-section view of InGaAs MOSFETs (a) and high-resolution TEM image of the QW channel (b).

conducted to obtain the two-dimensional electron gas (2DEG) density and mobility at 300 and 77 K. As shown in Table I, room-temperature mobilities of 6700 and 8200 $cm^2 \cdot V^{-1} \cdot s^{-1}$ have been achieved in QW-A and QW-B, respectively, with a sheet carrier density around 2.0×10^{12} $/cm^2$. Hall mobilities of 10,080 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at 300 K and 39,600 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at 77 K were achieved by QW-C with a high carrier density suitable for device applications. These values are comparable to the best results obtained by metamorphic InAlAs/GaAs buffers on offcut Si substrates [12, 13], and similar QW structures on lattice-matched InP substrates.

Using the high-mobility heterostructures on Si, we have fabricated nano-scale $In_{0.53}Ga_{0.47}As$ quantum-well MOSFETs with MOCVD source/drain regrowth. Al_2O_3 by atomic layer deposition (ALD) was employed as gate dielectric. Selective source/drain regrowth was incorporated to reduce parasitic resistances. Post-metallization annealing (PMA) was utilized to mitigate the weakened gate electrostatic control over the buried channel. The detailed gate-last process flow can be found elsewhere [14, 15]. Fig. 2 (a) depicts a cross-section view of the InGaAs MOSFETs and Fig. 2(b) displays a high resolution TEM image of the QW channel capped with gate dielectric. The output characteristic for a 30 nm-channel length (L_{ch}) device on Si is presented in Fig. 3. A maximum drain current (I_{dss}) of 1327 mA/mm was obtained at $V_{ds} = 0.5$ V and $V_{gs} = 1.6$ V, with a small R_{ON} of 157 $\Omega \cdot \mu m$. A peak extrinsic transconductance up to 1700 mS/mm has been achieved at $V_{ds} = 0.5$ V, as shown by the transfer characteristic in Fig. 4. The subthreshold slope (SS) was 142 mV/dec at V_{ds} = 50 mV and 186

Table I. 2DEG Density (N_s), Hall Mobility (μ) and Sheet Resistance (R_{sh}) of Three InGaAs QWs on Si.

Structure	300K			77K		
	N_s $(10^{12}/cm^2)$	μ $(cm^2/V s)$	R_{sh} (Ω/□)	N_s $(10^{12}/cm^2)$	μ $(cm^2/V s)$	R_{sh} (Ω/□)
QW-A	2.09	6710	445	1.86	26,800	125
QW-B	2.14	8200	356	1.99	27,500	114
QW-C	3.69	10800	157	3.26	39,600	48

mV/dec at V_{ds} = 0.5 V. Another device with a longer channel length of 60 nm exhibited a lower SS of 101 mV/dec at V_{ds}=0.05 V and SS of 120 mV/dec at V_{ds}=0.5 V. The excellent DC characteristics were demonstrated at low supply voltage, indicating the great potential of these transistors for "post-Si" high-speed, low-power logic applications.

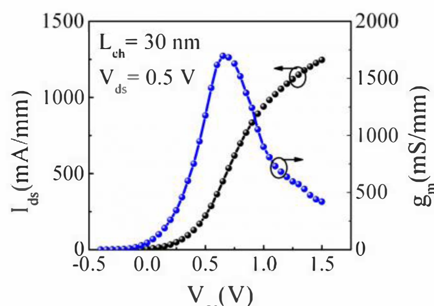

Figure 3: Transfer characteristic of a 30 nm-L_{ch} InGaAs MOSFET on Si.

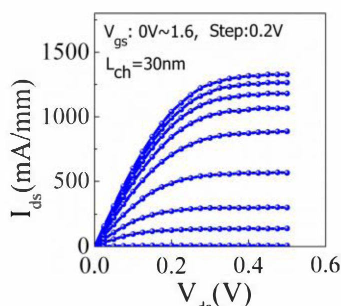

Figure 4: Output characteristic of a 30 nm-L_{ch} InGaAs MOSFET on Si.

Selective Area Growth of InGaAs Photodetectors on SOI Substrates

Based on the well-developed buffer technology on planar Si substrates, we further investigated selective-area growth of InP/GaAs buffers on exact (001)-oriented silicon-on-insulator (SOI) substrates for optoelectronic integration. High-speed normal-incidence photodetectors (NIPDs) and butt-coupled waveguide photodetectors (WGPDs) were fabricated on the same substrate [16]. Fig. 5. shows NIPDs put at the center of the growth well and WGPDs at the edge of the growth well for performance comparison. The devices demonstrated dark currents of 130 and 8 nA at −1V with 3dB bandwidths of 15 and 14 GHz at −5V, respectively. The result demonstrates the potential of integrating photonic and electronic devices on the same Si substrate by direct epitaxial growth.

InP on Nanopatterned Si for Electronic and Photonic applications

Conventional blanket heteroepitaxy of III-V on planar Si wafers usually involves thick transitional buffers for

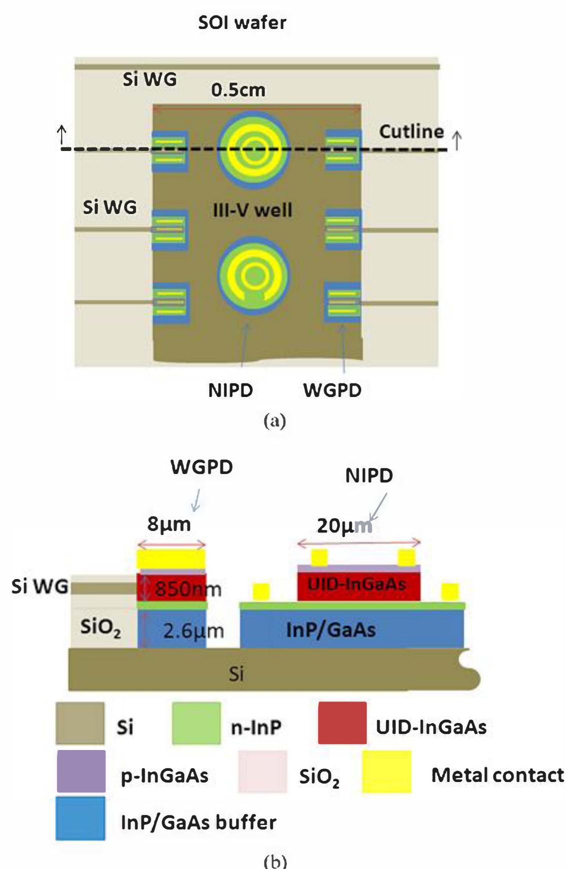

Figure 5: Schematics of the PDs selectively grown on a patterned SOI substrate. (a) Top-view of the patterned structure. (b) Side-view from the cutline.

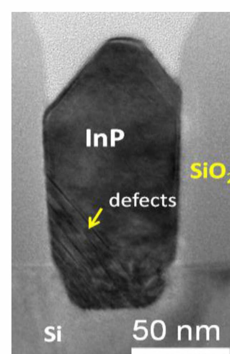

Figure 6: TEM image for InP growth in 65 nm-wide trench pattern on exact Si (001) substrates.

dislocation management. Thick buffers requiring long growth time limits the process throughput. A unique alternative approach is nanopatterned growth. By modifying the lattice relaxation at the early stage of the heteroepitaxy and trapping dislocations using the aspect ratio trapping (ART) technique [17], improved crystalline quality with reduced buffer thickness is possible. Fig. 6 shows the cross-sectional TEM image for InP grown on

on-axis Si with 65 nm-wide ART trench structure. Most of the defects generated at the interface between Si and InP were guided to the SiO_2 sidewall and terminated there. Device fabrication can take advantage of the low-defect density material at the upper portion of the trenches.

The aspect ratio trapping technique opens opportunities for integrating III-V nanoelectronics and nanophotonics on Si. However, for a lot of other device applications, large-area material is preferred. Combining the concept of traditional two-step growth method and epitaxial lateral overgrowth (ELOG), we have developed MOCVD growth of coalesced InP on nanopatterned Si with position-controlled seed arrays [18]. As illustrated by Fig.7, selective area growth of InP seeds inside the 30 nm-wide trenches was first carried out. Then, the growth was stopped and the SiO_2 pattern was removed by buffered oxide etch, leaving a position-controlled nanoscopic InP seed array on the Si surface. On top of such InP seed array template, MOCVD overgrowth of coalesced InP proceeded subsequently. By localizing defects in the buried Si concaves and promoting defect interactions during the coalescence process, a significant reduction in the x-ray linewidth has been observed for InP layers grown on the nanopatterned Si as compared to the blanket epitaxy. From plan-view TEM, the surface defects were dominated by stacking faults and a defect density of $\sim 2\times 10^8/cm^2$ was obtained for ~2 µm InP on nanopatterned Si.

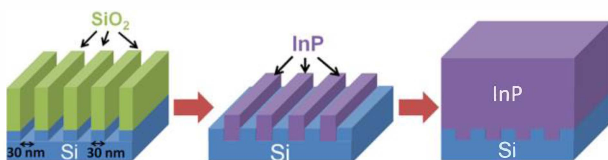

Figure 7: Growth procedure of InP on nanostructured Si with a position-controlled seed array.

CONCLUSION

Integration of III-V materials and devices on large-diameter Si substrates is attracting increasing interest and significant progress has been made by direct epitaxial growth. With the development of novel growth techniques and device integration schemes, an ultimate heterogeneous integrated system could be realized on the Si platform, providing Si CMOS technology with added III-V electronic and photonic functionalities.

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