High-Speed InGaAs Photodetectors by Selective-Area MOCVD Toward Optoelectronic Integrated Circuits

Yu Geng, Shaoqi Feng, Andrew W. O. Poon, *Member, IEEE*, and Kei May Lau, *Fellow, IEEE*

***Abstract*—We report selective-area growth of high-crystalline-quality InGaAs-based photodetectors with optimized InP/GaAs buffers on patterned (100)-oriented silicon-on-insulator (SOI) substrates by metal-organic chemical vapor deposition. The composite GaAs and InP buffer was grown using a two-temperature method. The island morphology of the low-temperature GaAs nucleation layer inside the growth well of the SOI substrate was optimized. A medium temperature GaAs layer was inserted prior to the typical high-temperature GaAs to further decrease the dislocation densities and antiphase boundaries. Both normal-incidence photodetectors and butt-coupled waveguide photodetectors were fabricated on the same substrate and showed a low dark current and high-speed performance. This result demonstrates a good potential of integrating photonic and electronic devices on the same Si substrate by direct epitaxial growth.**

***Index Terms*—Selective growth, buffer, dislocation, antiphase boundary, photodetector (PD), integration.**

I. Introduction

INTEGRATION of III-V photonic devices such as photodetectors (PDs) with electronic components that are nearly lattice-matched to InP on the same Si substrate is a promising solution for inter-chip and intra-chip optical interconnects at 1.55 μm wavelengths. Silicon, transparent at 1.55 μm wavelengths and has a large refractive index contrast with SiO_2, is suitable for use as integrated waveguides. Si also has the advantages of low cost and having a mature industrial infrastructure. Therefore, building an integrated photonic-electronic system on the Si platform has been one of the hottest research topics in the past decade. Various optoelectronic devices, including lasers [1], [2], modulators [3] and PDs [4]–[14] have been demonstrated on Si.

PDs are critical photonic devices that convert optical signals to electrical signals. There are mainly two material candidates for PDs on Si, namely Ge and $In_{0.53}Ga_{0.47}As$ lattice-matched to InP. Ge PDs on Si have been intensively investigated due to their potential compatibility with the standard complementary metal-oxide-semiconductor process [4]–[8]. Although electrically pumped lasing from Ge-on-Si heterojunction diodes were demonstrated recently [15], this technology is still not mature compared with the III-V counterpart, hence limiting the integration of Ge lasers with other devices on the same Si substrate. Emphasis has therefore been put on integrating III-V-based devices with the Si platform [1], [2], [9]–[14]. Conventionally, $In_{0.53}Ga_{0.47}As$, being lattice-matched to InP, is adopted as the active material for PDs operating at 1.55 μm. Due to the challenges in directly growing high-quality III-V on Si, wafer-bonding was adopted by many research groups to integrate InGaAs PDs on Si [9], [10]. However, the strict requirement of flat and smooth surfaces and the size-mismatch between III-V and Si wafers limit the application of wafer-bonding for scalable manufacturing.

Compared with wafer-bonding, direct epitaxial growth of InP, with a GaAs intermediate buffer layer on Si substrates, is an ideal wafer-level solution for low-cost mass production. Good crystalline and smooth GaAs layers on Si substrates can serve as a template for InP-based device growth [16]. However, growth of high-quality GaAs epilayers on Si substrates is not trivial because of the 4% lattice-mismatch, different thermal expansion coefficient and growth of polar III-V materials on non-polar Si [17], [18].

In order to grow GaAs and InP epilayers on Si substrates, many methods have been investigated over the past decades [17], [18]. Various growth techniques to optimize the growth layer quality through suppression of threading dislocations, antiphase boundaries (APBs) and other defects were investigated. Use of germanium buffers, compositional grading of alloy buffers, growth on mis-cut Si substrates, thermal annealing and insertion of strain-balancing layers have also been reported [19]–[21]. One solution we found very effective is the two-temperature growth technique, which consists of a low-temperature (LT) growth of a thin nucleation layer followed by a conventional high-temperature (HT) growth.

Advancements in epitaxial growth have led to a significant progress in various devices including InGaAs PDs on Si. We have reported various electronic devices with excellent DC

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Y. Geng, A. W. O. Poon, and K. M. Lau are with the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong (e-mail: ygeng@ust.hk; eeawpoon@ust.hk; eekmlau@ust.hk).

S. Feng was with the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong. He is now with the Department of Electrical and Computer Engineering, University of California, Davis, CA 95616 USA (e-mail: fengshaoqi@gmail.com).

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and radio-frequency (RF) performance on optimized InP/GaAs buffers directly grown on planer exact (100) oriented Si substrates [22], [23]. W. Prost *et al.* fabricated p-i-n InGaAs/Si PDs with a dark current of 1 μA and an open eye pattern at 10Gb/s, grown by a combination of molecular beam epitaxy and metal-organic chemical vapor deposition (MOCVD) [11]. Recently, we demonstrated high-speed normal-incidence photodetectors (NIPDs) and butt-coupled waveguide photodetectors (WGPDs) grown on Si substrates by MOCVD [12]–[14]. Although various electronic and photonic devices have been demonstrated on Si, not much work has been done on the integration of these devices by direct epitaxial growth. There are many challenges to integrate electronic and photonic devices on the same Si substrate by direct epitaxial growth. Obvious ones are crystalline quality of the buffer and active layers, positioning and connection of photonic and electronic devices and how to grow one kind of devices without much degradation of others. Optimization of the layout design and balancing of growth parameters to fulfill the performance objectives of the integrated components are the key.

In this paper, selective-area growth of InP/GaAs buffers on exact (100)-oriented silicon-on-insulator (SOI) substrates for optoelectronic integration was investigated. Proper balancing and trade-offs of the growth parameters to achieve growth suitable for different applications are the issues to be addressed. Surface morphologies, crystalline qualities, electrical properties, defect densities, and growth topologies for selective-area growth are among the characteristics that trade-offs must be made. A multi-temperature composite (MTC) GaAs buffer, modified from the previously reported process [24], was optimized and InP was grown on such optimized GaAs templates. Atomic force microscope (AFM), scanning-electron microscope (SEM), high-resolution X-ray diffraction (HRXRD) and transmission-electron microscopy (TEM) measurements show that the dislocation density and the APBs are greatly reduced, leading to smooth GaAs and InP surfaces, both at the edge and the center of the growth well. Both WGPDs and NIPDs fabricated on the same substrate showed high-speed performance and their dark currents were comparable with high-performance Ge/Si PDs [7], [8]. These results indicate that using this design and growth method, device-quality InP templates can be selectively grown on Si both at the edge and the center of the growth well, enabling the integration of photonic devices at the edge of the growth well, which can be coupled with other functional regions through waveguides, with possible electronic devices at the center of the growth well.

II. Structure Design

In order to achieve the integration of III-V photonic and electronic devices with Si by direct growth, an extensive structure design is needed.

One challenge is the layout of electronic and photonic devices, as well as waveguides that connect different devices and functional regions. A widely adopted method is to selectively grow III-V devices in a 'growth well' on a Si substrate connected by dielectric waveguides [25]. The region outside the growth well

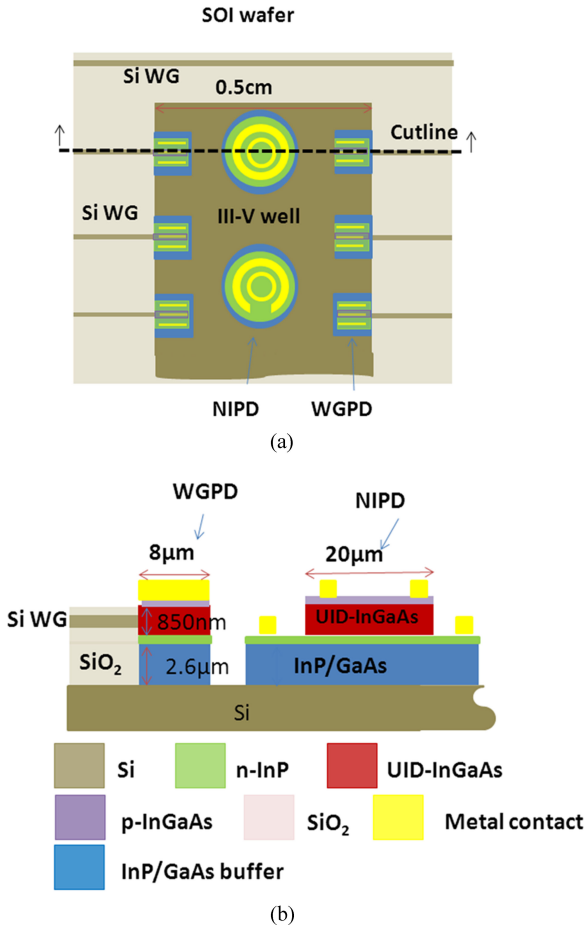


Fig. 1. Schematics of the PDs selectively grown on a patterned SOI substrate. (a) Top-view of the patterned structure. (b) Side-view from the cutline.

is protected by SiO_2 in order to prevent III-V material growth. In this way, the photonic devices could be optically connected by dielectric waveguides and electrically connected with other electronic devices. In this paper, we adopted SOI wafers because the Si device layer could be fabricated into waveguides. The schematic of the module layout is illustrated in Fig. 1.

In order to selectively grow photonic and electronic devices with different sizes and epitaxial structures, there are mainly two approaches of the growth well design. One is that the area of the growth well is matched to the device area. This method has the advantages of a good isolation among different devices and fewer fabrication steps [26]. However, photonic devices are usually much larger than electronic devices, and obtaining InP/GaAs buffers with good crystalline quality and a uniform growth rate in growth wells with various sizes in the same MOCVD run is problematic.

The other method is to grow III-V materials in a relatively large growth well and then fabricate different areas into different devices. In this way, there are only two kinds of regions, which are the edge and the center of the growth well. Thus, less tradeoff is needed and optimization becomes easier. This design requires the photonic devices be located at the edge of the growth well in order to communicate with other photonic devices by waveguides and electronic devices at the center of the growth. The

problem is that, the crystalline quality and the growth rate usually vary from the edge to the center of the growth well because of the loading effect. In this paper, the area of the growth well was designed to be 0.5 cm × 1.5 cm, with WGPDs at the edge and NIPDs at the center of the growth well, as shown in Fig. 1. In this design, light could be launched from the Si waveguide to the unintentionally doped (UID)-InGaAs absorption layer. WG-PDs could communicate with other photonic devices or regions using the Si waveguides and all the devices could be connected with electrical wires.

III. Experimental

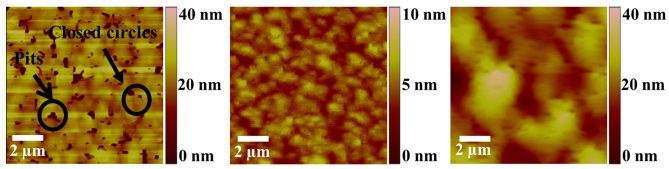
The $In_{0.53}Ga_{0.47}As$ PDs lattice matched to InP were selectively grown on a patterned (100)-oriented SOI substrate. The Si device layer and the buried-oxide (BOX) layer of this SOI substrate was 0.25 μm and 3 μm thick, respectively. The Si device layer was patterned using i-line (365 nm) photolithography followed by CF_4-based plasma etching process. The Si waveguide was designed to be 0.5 μm wide. Low-temperature oxide (LTO) was deposited on top as an upper-cladding for the waveguides as well as a growth mask in order to confine the III-V growth in the growth well. The growth well for the PD growth, with an area of 0.5 cm × 1.5 cm, was opened by dry etching the top LTO layer, the Si layer and the BOX layer followed by wet etching in order to protect the Si surface. The detailed process can be found in [13].

The growth was performed in an Aixtron AIX-200/4 MOCVD system. Growth optimization was first performed on planar Si substrates and then on patterned SOI substrates to investigate the growth conditions at different regions of the growth well. In order to alleviate the 8% lattice-mismatch between InP and Si, GaAs and InP composite buffers were grown on the Si and patterned SOI substrates. Triethylgallium (TEGa), Arsine (AsH_3), Trimethylindium (TMIn) and Phosphine (PH_3) were used as precursors for Ga, As, In and P, respectively. First, an *in-situ* baking in H_2 at 810 °C for 30 min was performed to remove the native oxide. Then, the temperature was ramped down to 400 °C with an AsH_3 pre-flow. When the temperature was stable at 400 °C, a GaAs nucleation layer was grown for different times at 400 °C, with a V/III ratio of 100 at the same growth rate. After the GaAs nucleation layer, the growth was paused and the temperature was ramped to higher temperatures for the subsequent growth. Different temperatures and growth processes were used to optimize the crystalline quality of the GaAs buffer, as shown in Table I. Then, an InP buffer was grown, which included a thin InP nucleation layer and a HT InP layer. The surface morphology was investigated with AFM. Crystalline quality of the GaAs and InP buffer layers were studied by HRXRD and TEM under two-beam condition with g = [220].

The p-i-n structure was grown on an optimized InP/GaAs buffer for WGPDs at the edge and NIPDs at the center of the growth well, with an 850 nm-thick UID-InGaAs as the absorption layer for WGPDs (650 nm for NIPDs). This difference in thickness is due to the loading effect during material growth. The WGPDs and NIPDs, located on the same patterned substrate, were grown and processed together to investigate the compatibility of the different devices at different regions. The process for PD fabrication has been reported in [13]. As shown in Fig. 1, the WGPDs were fabricated at the edge of the growth well for the laser light to be launched from the waveguide to the InGaAs absorption layer. The NIPDs were fabricated at the center of the growth well for the light to illuminate from the top.

TABLE I
GaAs Growth Details of Different Samples (L-TempC and L-TempD are the Corresponding LT Layers of H-TempC and H-TempD, Respectively.)

Samples	Substrate	LT	MT	HT
H-Temp A	Planar Si	400°C / 8min	None	630°C
H-Temp B	Planar Si	400°C / 8min	540°C and 570°C	630°C
H-Temp C	Patterned SOI	400°C / 8min	540°C and 570°C	630°C
H-Temp D	Patterned SOI	400°C / 4min	540°C and 570°C	630°C
H-Temp E	Patterned SOI	400°C / 4min	540°C and 570°C	600°C
L-Temp C	Patterned SOI	400°C / 8min	None	None
L-Temp D	Patterned SOI	400°C / 4min	None	None



(a) (b) (c)

Fig. 2. AFM images of the GaAs HT layers (10 μm × 10 μm scans). (a) Sample H-TempA with a RMS of 10 nm. (b) Sample H-TempB with a RMS of 1 nm. (c) Edge of sample H-TempC with a RMS of 10 nm.

IV. Results and Discussion

A. GaAs Buffer Growth

The growth optimization was first performed on planar Si substrates. Sample H-TempA with the typical two-step growth technique, which consists of LT (400 °C) and HT (630 °C) grown layers, was first attempted but the surface was quite rough according to AFM measurements, with a root-mean-square (RMS) of 10 nm (10 μm × 10 μm area scan), as shown in Fig. 2(a). The pits are evidence of threading dislocations punching through the sample surface and the closed circles are the APBs [27], [28]. The high dislocation and APB densities are detrimental to the device performance as they could give rise to a large dark current [17]. In order to suppress these defects, samples were grown at different temperatures for the HT step, which shows that growth at a temperature below 580 °C leads to much better surface morphologies. However, in general, GaAs growth in the temperature range from 600 °C to 650 °C is optimal for good crystalline quality [29]. Therefore, a MTC growth technique

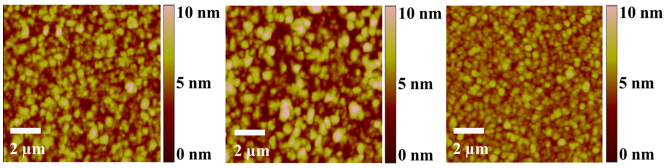


Fig. 3. AFM images of the GaAs LT layers (10 μm $\times$ 10 μm scans). (a) Center of the growth well of sample L-TempC with a RMS of 1.1 nm. (b) Edge of the growth well of sample L-TempC with a RMS of 1.8 nm. (c) Edge of the growth well of sample L-TempD with a RMS of 0.8 nm.

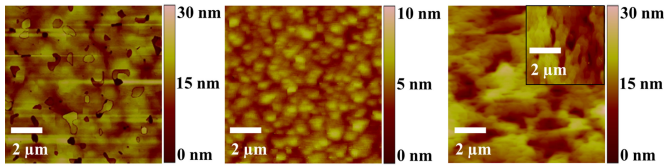


Fig. 4. AFM images of the material surface on the SOI substrate at the edge of the growth well (10 μm $\times$ 10 μm scans). (a) Sample H-TempD with a RMS of 6 nm. (b) Sample H-TempE with a RMS of 1 nm. (c) InP/GaAs with a RMS of 6 nm. Inset: InGaAs PDs grown on this optimized buffer with a RMS of 5 nm.

was used in sample H-TempB with a medium-temperature (MT) layer inserted in between the LT and HT layers to obtain both good surface morphologies and good crystalline qualities. This MT layer consists of two thin sub-layers grown at 540 °C and 570 °C, respectively. The AFM measurement (10 μm $\times$ 10 μm area scan) in Fig. 2(b) shows that the surface is quite smooth with a RMS of 1 nm with much fewer pits and closed circles, indicating much reduced dislocations and APB densities.

After the growth optimization on planar Si substrates, selective-area growth of sample H-TempC was performed on patterned SOI substrates. However, although the surface morphology at the center of the growth well was still as good as that on the planar Si substrates using the MTC growth technique, the surface morphology at the edge of the growth well was very rough, as characterized by a highly non-uniform surface morphology with large dots, as shown in Fig. 2(c). This rough surface was detrimental to the device performance and made integration of devices located at the edge and the center of the growth well difficult.

This significant roughness of the top HT layer of sample H-TempC at the edge of the growth well is believed to be caused by the non-uniform nucleation layer. The nucleation layers were studied by AFM, which shows that the dot size is more uniform at the center of the growth well of sample L-TempC shown in Fig. 3(a) than at the edge of the growth well of sample L-TempC shown in Fig. 3(b). The dot size at the center of the growth well is smaller and the RMS of this surface is 1.1 nm. The dot size at the edge of the growth well is not as uniform as that at the center, characterized with bigger dots and some large coalesced dots. The RMS of this surface is 1.8 nm. Because of the large stress caused by the large lattice-mismatch between GaAs and Si, the dislocation density in the large coalesced dots is high [18]. Those dislocations would propagate to the upper HT layer during the subsequent growth and degrade the crystalline quality and the surface morphology of the GaAs buffer, as shown in Fig. 2(c).

In order to decrease the density of coalesced dots, several solutions were considered. One solution is to reduce the growth temperature, which suppresses the process of coalescence of the dots in the nucleation layer. However, with our growth temperature of 400 °C, it is already very low and a temperature even lower would cause a too low AsH_3 decomposition efficiency, which would cause formation of Ga dots during the growth. The other solution is to reduce the growth time. As the dot size is uniform at the center of the growth well of sample L-TempC,

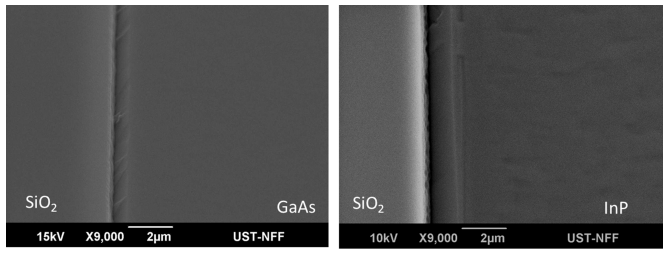


Fig. 5. SEM images of the buffer surfaces on the SOI substrate at the edge of the growth well. (a) GaAs and (b) InP.

this non-uniformity at the edge was caused by the loading effect of selective-area growth, which leads to an enhanced growth rate and accumulated deposition at the edge of the growth well with the same growth time. Thus, by decreasing the growth time to compensate the loading effect, the density of the coalesced dots should also be smaller. After decreasing the growth time from 8 min to 4 min in sample L-TempD, the uniformity of the nucleation layer at the edge of the growth well was much better, with a RMS of 0.8 nm, as shown in Fig. 3(c).

Sample H-TempD was grown on top of sample L-TempD, with a LT growth time of 4 min and with the same MT and HT growth technique introduced above, where the surface morphology was improved but many closed circles and pits appeared, as shown in Fig. 4(a), indicating a large density of APBs and threading dislocations. From the above discussion, temperature plays an important role in the growth. Thus, the temperature of the HT growth was reduced from 630 °C to 600 °C in sample H-TempE. The AFM image in Fig. 4(b) shows a very smooth surface with a RMS of 1 nm. The RMS at the center of the growth well was still 1 nm after this optimization. From the SEM images shown in Fig. 5(a), a good selectivity between the Si growth well and the SiO_2 mask was obtained. This uniformly smooth surface makes it possible to fabricate high-performance devices, both at the edge and the center of the growth well.

B. InP Buffer Growth

After the GaAs buffer on the patterned SOI substrate, the InP buffer was grown subsequently, which included a thin InP nucleation layer deposited at 430°C and a HT InP at 610°C. There is a thin $In_{0.65}Ga_{0.35}As$ insertion layer in the HT InP layer in order to smooth the top surface and filter the threading dislocations [17]. This strained InGaAs insertion layer was kept within

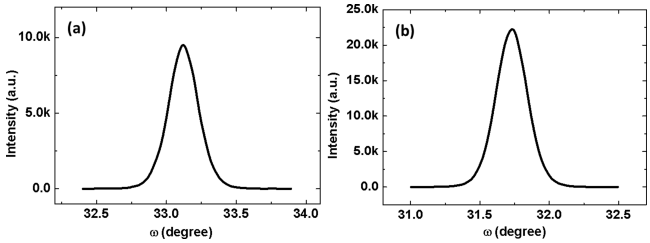


Fig. 6. HRXRD rocking curves of the optimized buffers. (a) GaAs buffer with a FWHM of 820 arcsec. (b) InP buffer with a FWHM of 900 arcsec.

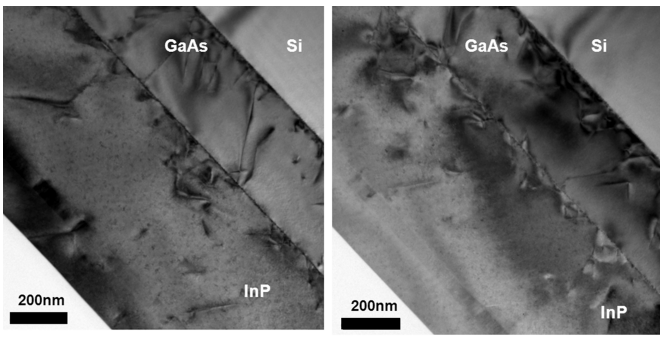


Fig. 7. TEM images of the optimized buffers under two-beam condition with g = [220]. (a) InP/GaAs buffers grown on a planer Si substrate and (b) InP/GaAs buffers selectively grown on a patterned SOI substrate.

a critical thickness to avoid the generation of misfit dislocations at the interfaces. The surface of the InP buffer is smooth, as shown in Fig. 5(b) by SEM. The RMS is 6 nm by AFM (10 μm $\times$ 10 μm scan) at the growth well, as shown in Fig. 4(c). The $In_{0.53}Ga_{0.47}As$ PDs were grown on top of this optimized InP/GaAs buffer with RMS of 5 nm by AFM (10 μm $\times$ 10 μm scan) as shown in the inset of Fig. 4(c).The RMS of the InP layer and $In_{0.53}Ga_{0.47}As$ is relatively large and should be reduced in the future work.

Fig. 6 shows the HRXRD ω-rocking curves of the optimized GaAs and InP buffers. The full-width at half-maximum (FWHM) of GaAs and InP are 820 arcsec and 900 arcsec, respectively, and they can be related to the dislocation density through Ayers' model [30]

$$D = \frac{\beta^2}{4.36b^2} \tag{1}$$

where D is the dislocation density (cm^{-2}), β is the FWHM in radians, b is the length of burgers vector of dislocation. For a 60° dislocation, $b = a/\sqrt{2}$, where a is the lattice constant. The dislocation densities estimated by this model are 2.4×10^9 cm^{-2} for GaAs and 2.6×10^9 cm^{-2} for InP, which are the upper limits of the dislocation densities in our GaAs and InP buffers.

The cross-sectional bright-field TEM images of the optimized samples are shown in Fig. 7. Fig. 7(a) shows the InP/GaAs buffers grown on a planar Si substrate. Fig. 7(b) shows the buffer grown on a patterned SOI substrate. Both of these two TEM pictures show many dislocations generated at the GaAs/Si and InP/GaAs interfaces due to the lattice-mismatch between them. Nevertheless, most of the defects vanished by intersecting

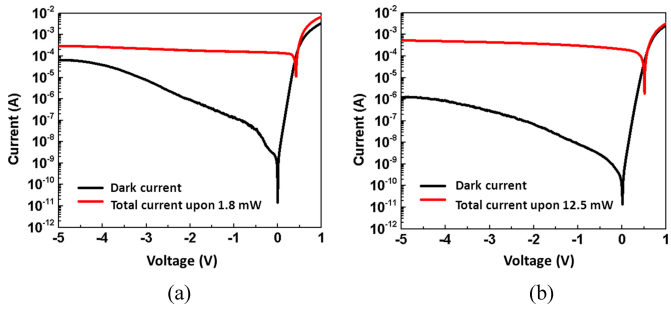


Fig. 8. Measured dark currents and total current densities as a function of bias voltages. (a) NIPD and (b) WGPD.

with each other during the HT growth. Thus, the dislocations in the GaAs and InP buffers are mainly restricted in the lower half of the GaAs and InP buffers, resulting in a relatively smooth surface and a upper half with low defects.

C. Device Characterization

The active area is 64 μm^2 for WGPDs and 314 μm^2 for NIPDs. Fig. 8(a) shows the measured dark current and total current with an optical input power of 1.8 mW at 1550 nm illuminated at the top of the NIPDs. The bias voltage ranged from -5V to 1V. The dark current is 130 nA at -1V bias voltage, corresponding to a dark current density of 40 mA/cm^2. Fig. 8(b) shows the measured dark current and total current with an optical input power of 12.5 mW at 1550 nm by launching the laser light close to the edge of the WGPDs (for the waveguide was partially damaged during the fabrication, as explained below). The bias voltage ranged from -5V to 1V. The dark current is 8 nA at -1V bias voltage, corresponding to a dark current density of 12 mA/cm^2. The larger dark current density of NIPDs should be due to the fact that all the growth optimization was mainly focused on the material at the edge of the growth well and some trade-off was made for the growth between that at the center and at the edge of the growth well.

The responsivity at -1V is measured as 0.02 A/W for WGPDs and 0.6 A/W for NIPDs, as shown in Fig. 8. The low responsivity of the WGPDs is due to a fabrication issue we encountered when fabricating the Si waveguide. The main problem is that the SiO_2 upper-cladding was accidentally damaged when exposing the Si substrate for the selective-area growth. Thus, the Si waveguide propagation loss becomes exceedingly large. This problem could be solved after optimization of the Si waveguide fabrication process, along with the selective-area growth.

A 20 GHz vector network analyzer was used to measure the RF response of the PDs. The optical signal modulated by a 30 GHz $LiNO_3$ modulator was coupled to the PD, and the PD output was measured by a 40 GHz probe. After a calibration by a commercial 30 GHz PD, the frequency response of the PDs was measured upon various reverse-bias voltages, as shown in Fig. 9. The frequency response was normalized to 10 MHz. The 3 dB bandwidths upon -1 and -5V bias voltages are 4 and 14 GHz for WGPDs, and 2.5 and 15 GHz for NIPDs, respectively.

The 3 dB bandwidths of both NIPDs and WGPDs are mainly determined by the carrier transit time in the InGaAs absorption

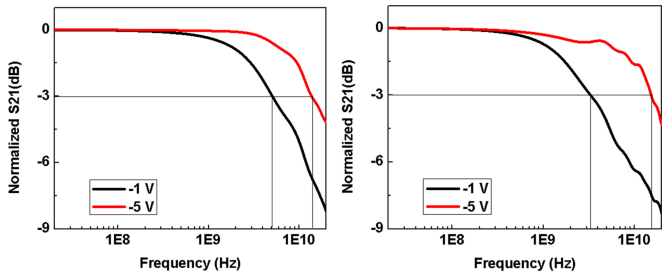


Fig. 9. Measured RF responses of PDs at −1V and −5V. (a) NIPD and (b) WGPD.

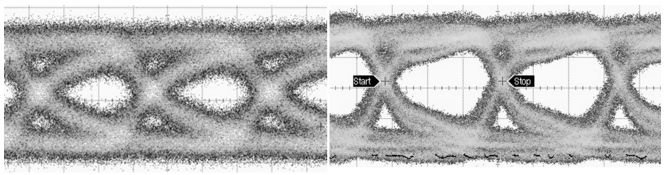


Fig. 10. Measured eye diagrams at 20 Gb/s at −5V (time: 20 ps/div, scale: 17 mV/div). (a) WGPD. (b)NIPD.

TABLE II
COMPARISON OF PDS ON SI SUBSTRATES BY VARIOUS TECHNOLOGY PLATFORMS[a]

	Res. (A/W)	DC Dens. (mA/cm^2)	BW (GHz)	Area (μm^2)
Ge growth [7]	0.8	40	45	5
Ge growth [8]	0.62	27	62	100
III-V bonding [10]	0.45	3	33	50
III-V growth [12]	0.57	64	10	314
III-V growth [13]	0.22	625	9	400
WGPD of this work	0.02	12	14	64
NIPD of this work	0.6	40	15	314

[a] Res.: responsivity; DC: dark current; DC Dens.: dark current density; BW: 3dB bandwidth.

layer and the resistance-capacitance time constant of the device. The calculated transit-time-limited bandwidths are 36 GHz for NIPDs and 28 GHz for WGPDs, given the hole and electron saturation velocities under a high electric field of about 50 kV/cm at −5 V. Thus, the measured PD bandwidths should be limited by the junction capacitance and the parasitic capacitance, which are estimated to be 12 and 20 fF for WGPDs, and 14 and 22 fF for NIPDs, respectively [13].

Non-return-to-zero eye diagrams were measured using an 80 GHz oscilloscope. The RF signal from a pseudorandom bit sequence generator with a pattern length of $2^{31}-1$ was used to modulate the 1550 nm light through the modulator. Open eyes at 20 Gb/s upon a −5V bias voltage were observed for both NIPDs and WGPDs, as shown in Fig. 10.

Device performances of PDs on Si substrates by different technology platforms are compared in Table II. The dark current density of this paper is comparable with that of Ge PDs on Si [7], [8], yet it is still larger than that of III-V PDs bonded on Si substrates [10]. This indicates that the crysalline quality of the InP/GaAs buffers on Si need more optimizations in order to minimize the defects. Some growth technologies such as aspect ratio trapping growth could be used to further improve the crystalline quality [31]. The bandwidth of PDs in this paper is lower than other works on Si [7], [8], [10]. It can be improved by shrinking the size of the active regions and using the design of uni-traveling-carrier PDs [32], [33]. The responsivity of the WGPD device can be much improved with better coupling. The results presented here reveal the potential of integrating multiple devices with good performances within the same growth well.

V. CONCLUSION

In summary, the crystalline quality of InP/GaAs layers was improved with a MTC growth method and high-performance PDs were fabricated both at the edge and the center of the growth well. The growth time of the LT layer was reduced to compensate the loading effect at the edge of the growth well to form a uniform layer of nucleation dots for the subsequent HT growth. By AFM and TEM characterizations, the dislocation density and the APBs in the GaAs buffer were found to be effectively reduced by insertion of the medium-temperature layer in between the LT and HT layers. NIPDs at the center of the growth well and WGPDs at the edge of the growth well demonstrated dark currents of 130 and 8 nA at −1V with 3dB bandwidths of 15 and 14 GHz at −5V, respectively. This shows that the selective-area growth of InP/GaAs buffers on SOI substrates with a large growth well can be made, with tradeoffs between the edge and the center of the growth well optimized. Different devices on the same buffer can then be grown separately on this optimized buffer. Photonic devices could be located at the edge of the growth well for waveguide connections and electronic devices could be located at the center of the growth well for integration with other devices. These results demonstrate that selective epitaxy by MOCVD can be an effective means to integrate photonic and electronic devices on the same Si substrate.

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Yu Geng is currently working toward the Ph.D. degree in the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong. His research interests include MOCVD growth and fabrication of photodetectors, lasers, and integrated optoelectronics.

Shaoqi Feng received the B.E. degree in optoelectronics from Nankai University, Tianjin, China, in 2008 And the Ph.D. degree in electronic and computer engineering from the Hong Kong University of Science and Technology, Hong Kong, in 2013. He is currently a Postdoctoral Researcher in Department of Electrical and Computer Engineering, University of California, Davis, CA, USA.

Andrew W. O. Poon received the B.A. (Hons.) degree from the University of Chicago, Chicago, Illinois, USA, in 1995, and the M. Phil and Ph. D. degrees from Yale University, New Haven, CT, USA, in 1998 and 2001, all in physics. In 2001, he joined the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, as an Assistant Professor, where he is currently an Associate Professor. His research group focuses on experiments and modeling of optical microresonators and silicon photonics.

Kei May Lau received the Ph.D. degree in electrical engineering from Rice University, Houston, TX, USA. She is currently a Chair Professor with the Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong. She was on the faculty of the ECE Department at the University of Massachusetts/Amherst before joining HKUST in 2000. Her group's research interests are primarily III–V and wide bandgap semiconductor materials and devices, for integration on silicon.