High Performance Self-aligned AlN/GaN MISHEMT with In-situ SiNx Gate Dielectric and Regrown Source/Drain

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Abstract
Gate-last self-aligned AlN/GaN MISHEMTs with in-situ grown SiNx gate dielectric for gate leakage suppression and regrown n'-GaN S/D for minimizing contact resistance were demonstrated. The device with a gate length of 0.32 µm exhibited a maximum drain current density of 1310 mA/mm and a high on/off ratio of over 10^7. The current gain cutoff frequency (fT) and maximum oscillation frequency (fmax) were 45 and 73 GHz, respectively, resulting in a high fT×Lg product of 14.4 GHz·µm. The best gate-to-drain breakdown voltage up to 35.2 V was obtained for a 90 nm gate-to-regrown-drain distance, leading to a high breakdown field of 4.46 MV/cm.

INTRODUCTION
AlN/GaN HEMTs have great potential for RF and microwave power applications due to their unique combination of high operation frequency and large output power density. The use of an ultra-thin AlN barrier layer also allows good gate control capability and a high aspect ratio (gate length and gate to channel distance) to mitigate the short-channel effects. In recent years, impressive device performances, such as both fT and fmax well exceeding 300 GHz [1] and an output power density of 2.5 W/mm at 40 GHz [2], have been demonstrated in the literature. Unless the epi-layers are well passivated, the thin AlN barriers may suffer from surface sensitivity and large gate leakage currents, limiting the device performance and reliability. Recently, in-situ SiNx gate dielectric grown by MOCVD has been successfully developed and demonstrated to be advantageous over other ex-situ deposited insulators. The in-situ SiNx on AlN/GaN MISHEMTs resulted in better surface passivation effects, suppression of gate leakage currents and elimination of process- and growth-related defects [2], [3]. On the other hand, the high potential barrier of AlN makes it difficult to form low contact resistance to the channel. One emerging alternative device design is incorporating regrown highly doped S/D for ohmic contacts [1].

In this work, high performance AlN/GaN MISHEMTs have been demonstrated using a gate-last self-aligned fabrication process. By employing the MOCVD-grown in-situ SiNx gate dielectric, low gate leakage current and high on/off ratio have been achieved. The regrown ohmic contact and low-k (κ = 2.65) BCB planarization technologies [4] have enabled a reduction of the access resistance and parasitic capacitance, leading to a simultaneously high fT and fmax, as well as a relatively large fT×Lg product for the sub-micron gated devices.

Fig. 1. The cross-sectional schematic (a) and AFM image (b) of the as-grown in-situ SiNx/AlN/GaN MISHEMT sample.

MATERIAL GROWTH AND DEVICE FABRICATION
The in-situ SiNx/AlN/GaN heterostructure was grown on a 2-inch sapphire substrate in an AIXTRON2000HT MOCVD system. The epi-layers consist of, from bottom to top, a 35 nm AlN nucleation layer, a 300 nm AlN buffer layer, a 2.7 µm undoped GaN layer, a 3.5 nm AlN barrier layer and, finally, a 7 nm in-situ SiNx cap layer, as shown in Fig. 1(a). The in-situ SiNx was deposited immediately following the AlN/GaN heterostructure growth in the MOCVD chamber using silane and ammonia as precursors at 1145 °C [3]. AFM observation of the as-grown sample in Fig. 1(b) shows a smooth surface morphology and uniform coverage of in-situ SiNx. The root mean square (RMS) roughness across a 5μm×5μm scanned surface area was 1.1 nm.

A gate-last self-aligned process (Fig. 2) was developed to fabricate the MISHEMTs. 300-nm-thick SiO2 was first deposited by PECVD on the sample. The initial 1 µm SiO2 dummy gate was defined by photolithography and patterned using a RIE process. Subsequently, the SiO2 gate length was further shrunk down to < 500nm by wet etching in a BOE solution. A layer of PECVD SiNx was then blanket deposited, followed by an anisotropic RIE etching to form sidewall spacers. The pre-regrowth etch depth into the MISHEMT structure was 90 nm, and regrown n'-GaN was...
180 nm thick with a Si doping level of about $6 \times 10^{19}$ cm$^{-3}$. After mesa isolation etching, S/D electrodes were formed on the n$^+$-GaN layer using nonalloyed Cr/Au metal. Then, the planarization process using low-$\kappa$ BCB material was conducted to expose the SiO$_2$ dummy gate [4]. Finally, the dummy gate was removed by BOE and replaced with a Ni/Au metal gate. The gate head of the T-shaped gate was 1.5 $\mu$m, defined by photolithography. The cross-sectional SEM image of the gate region is shown in Fig. 3. The thickness of the BCB supporting layer was about 100 nm and the gate-to-regrown-S/D distances ($L_{GS}/L_{GD}$) 90 nm, defined by the SiN$_x$ sidewall spacers.

**RESULTS AND DISCUSSION**

Fig. 4 shows the DC characteristics of a 0.32 $\mu$m gated self-aligned MISHEMT with a gate width of 2 $\times$ 50 $\mu$m. The device exhibited a high maximum drain current ($I_{DS}$) of 1310 mA/mm at $V_{DS} = 5$ V and $V_{GS} = 3$ V, and the on-resistance was as low as 1.7 $\Omega$•mm. The peak transconductance was 330 mS/mm at $V_{DS} = 6$ V and $V_{GS} = -0.3$ V. The achieved results are mainly attributed to the reduction of access resistance by the heavily doped S/D regrowth, as well as the reduced $L_{GS}$ and $L_{GD}$ by the self-aligned process. Moreover, the gate leakage and off-state drain leakage of the device were both below $10^{-4}$ mA/mm at $V_{GS} = -8$ V and $V_{DS} = 6$ V, leading to a large on/off ratio of over $10^7$. This indicated that the high quality in-situ SiN$_x$ was very effective in suppressing the leakage current and protecting the AlN surface.

S-parameter measurements were carried out in the frequency range of 0.1 - 39 GHz. The system was calibrated with an off-wafer short-open-load-through calibration standard. On-wafer open pads were used to de-embed the parasitic pad capacitances from the measured S-parameters. Fig. 5 shows the RF characteristics of the 0.32 $\mu$m gated device measured at maximum $f_T$ bias condition ($V_{DS} = 9$ V, $V_{GS} = 0$ V). A simultaneously high $f_T/f_{max}$ of 45/73 GHz was obtained by extrapolating the current gain ($|h_{21}|^2$) and unilateral power gain ($U$) using ~20 dB/dec slope. The $f_T$ product was 14.4 GHz-$\mu$m, favorably comparable to the state-of-the-art results in the literature [1], [2], [5-10].

As shown in Fig. 4, the three-terminal off-state breakdown voltage ($BV_{off}$) of the 0.32 $\mu$m gated device at $V_{GS} = -5$ V ($I_{DS} = 1$ mA/mm) was 22.5 V. This compromised
breakdown voltage was due to the non-ideal buffer quality of the epi rather than the device gate configuration, since it was found that the buffer leakage dominated the off-state leakage, as shown in Fig. 6(a). Because of non-uniformity, a breakdown voltage up to 35.2 V was obtained for another device on the same sample with similar gate length, where the real gate dielectric breakdown happens, as shown in Fig. 6(b). For 90 nm $L_{GD}$, a breakdown field of 4.46 MV/cm, well above the critical breakdown field of GaN, was deduced. This was attributed to the high quality in-situ SiN$_x$ gate dielectric used in the devices.

CONCLUSIONS

Gate-last self-aligned AlN/GaN MISHEMTs with in-situ SiN$_x$ gate dielectric and regrown S/D have been demonstrated. A 0.32 μm gated device exhibited high performances, including a low gate leakage current, a high on/off ratio, and a relatively large $f_T \times L_G$ product. Further improvement can be achieved by scaling the gate footprint and gate head.

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REFERENCES


ACRONYMS

MISHEMT: metal-insulator-semiconductor high electron mobility transistor
RF: radio frequency
2DEG: two-dimensional electron gas
MOCVD: metal-organic chemical vapor deposition
S/D: source/drain
BCB: benzocyclobutene
AFM: atomic force microscopy
PECVD: plasma-enhanced chemical vapor deposition
RIE: reactive ion etching
BOE: buffered oxide etchant
SEM: scanning electron microscopy
DC: direct current