Characterization of in situ SiNx thin film grown on AlN/GaN heterostructure by metal-organic chemical vapor deposition

Xing Lu, Jun Ma, Huaxing Jiang, and Kei May Lau

Citation: Applied Physics Letters **104**, 032903 (2014); doi: 10.1063/1.4862664
View online: http://dx.doi.org/10.1063/1.4862664
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/104/3?ver=pdfcov
Published by the AIP Publishing

APPLIED PHYSICS LETTERS **104**, 032903 (2014)

Characterization of *in situ* SiN_x thin film grown on AlN/GaN heterostructure by metal-organic chemical vapor deposition

Xing Lu, Jun Ma, Huaxing Jiang, and Kei May Lau[a)]
Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong

(Received 15 October 2013; accepted 5 January 2014; published online 21 January 2014)

We report an investigation of *in situ* SiN_x gate dielectric grown on AlN/GaN heterostructures by metal-organic chemical vapor deposition. It is revealed that the *in situ* SiN_x is Si-rich, with a N/Si ratio of 1.21 and a relatively high effective dielectric constant of ~8.3. The 7 nm *in situ* SiN_x film exhibited a large resistivity of $>10^{14}\ \Omega\cdot cm$ and a breakdown field of 5.7 MV/cm. Furthermore, interface trapping effects in the *in situ* SiN_x/AlN/GaN heterostructures were investigated by frequency dependent conductance analysis. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4862664]

Due to the relatively large bandgap and strong polarization effects of AlN, AlN/GaN heterostructures can result in a high two-dimensional electron gas (2DEG) concentration and good carrier confinement with thin barrier layers. AlN/GaN high electron mobility transistors (HEMTs) are very attractive for high frequency and high power applications.[1–4] In addition, ultrathin AlN barriers allow good gate control capability and a high aspect ratio (gate length and gate to channel distance) to mitigate the short channel effects. However, low quality thin AlN and poor interfaces can lead to problems such as large leakage current and surface sensitivity, limiting the device performance and reliability. Several dielectrics such as Al_2O_3,[3–6] SiN_x,[7] HfO_2, and Ta_2O_5 (Refs. 8 and 9) have been explored as gate insulators in AlN/GaN HEMTs. Most of these insulators are deposited *ex situ*, which may introduce additional growth- and process-related defects on the devices. In contrast, an metal-organic chemical vapor deposition (MOCVD) *in situ* grown SiN_x layer immediately after the transistor structure would be advantageous over existing *ex situ* deposited insulators for better surface passivation effects and suppression of gate leakage current.[1,10–13] High temperature growth by MOCVD can facilitate the formation of high quality *in situ* SiN_x films. However, limited work has been reported with successful use of *in situ* SiN_x as gate dielectric for AlN/GaN metal-insulator-semiconductor (MIS) devices. Higashiwaki *et al.* even found that the *in situ* SiN_x gate dielectric can lead to larger gate leakage when compared with the *ex situ* deposited ones.[14] On the other hand, high performance AlN/GaN HEMTs have been reported with *in situ* SiN_x cap layer for surface passivation rather than gate dielectric. The SiN_x in the gate region was selectively removed during the device fabrication.[1] Hence, detailed characterization of *in situ* SiN_x layer over AlN/GaN heterostructures is very useful, specifically for gate dielectric applications in AlN/GaN MIS devices.

In this letter, we report a study of *in situ* SiN_x thin film grown on AlN/GaN heterostructures by MOCVD. Both material structural and electrical characterizations were performed to evaluate the performance of the *in situ* SiN_x film as a gate insulator.

The *in situ* SiN_x/AlN/GaN heterostructures were grown on 2-in. Si (111) substrates in an AIXTRON2000HT MOCVD system.[10] The epi-layers consist of, from bottom to top, a 45 nm AlN nucleation layer, 1.3 μm strain/resistivity-engineering buffer layers, a 1 μm GaN layer, a 1.5 nm AlN barrier layer and finally an *in situ* SiN_x cap layer. The *in situ* SiN_x was deposited immediately following the AlN/GaN heterostructure growth in the MOCVD chamber using silane and ammonia as precursors. The chamber pressure and substrate temperature were 100 mbar and 1145 °C, respectively. For the characterization of electrical properties, circular MIS diodes were fabricated. Firstly, mesa etching for device isolation was performed using a CF_4/O_2-based reactive ion etching (RIE) followed by a Cl_2-based inductively coupled plasma (ICP) etching. After selective removal of the SiN_x cap layer in the Ohmic contact region by RIE, Ti/Al/Ni/Au (20/150/50/80 nm) was deposited by e-beam evaporation and annealed at 850 °C in N_2 ambient for 30 s. Finally, the Ni/Au (20/200 nm) gate metal was deposited on the *in situ* SiN_x by e-beam evaporation. The diameter of the circular metal gate was 200 μm. Similar metal-oxide-semiconductor (MOS) diode structures fabricated with 7 nm Al_2O_3 deposited by atomic layer deposition (ALD) on AlN/GaN heterostructures[6] were used as a reference for comparison in this work.

Atomic force microscopy (AFM) and transmission electron microscopy (TEM) observations in Fig. 1 show good surface morphology and uniform coverage of the thin SiN_x. The root mean square (RMS) roughness across a 5 μm × 5 μm scanned area is 2.15 nm. The thickness of the *in situ* SiN_x film is 7 nm. The growth time was 28 min, and thus the growth rate is determined to be 2.5 Å/min.

To quantify the nitrogen composition in the SiN_x film, x-ray photoelectron spectroscopy (XPS) measurements were carried out. The XPS spectra were acquired after sputter removal of about 2 nm material from surface by argon. The binding energy measurement was calibrated by correcting C1s peak to be 285 eV. Fig. 2 shows the results of the peak fitting performed on the Si2p core-level XPS spectrum of the 7 nm *in situ* SiN_x. Two components corresponding to Si-N

[a)]Email: eekmlau@ust.hk. Tel.: (852) 23587049. Fax: (852) 23581485.

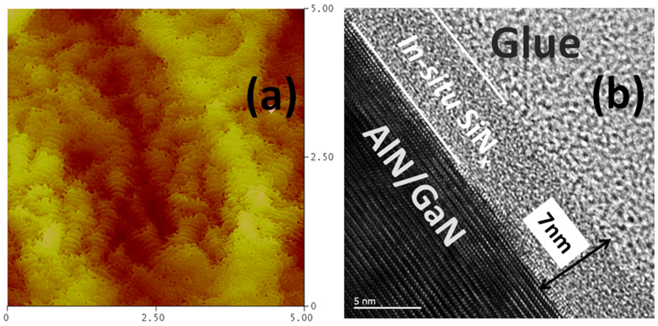

FIG. 1. AFM (a) and TEM (b) observations of the 7 nm *in situ* SiN_x film deposited by MOCVD.

bonds (101.5 eV) and a mixing of Si-N and Si-Si or Si-H bonds (100.6 eV) were extracted from the spectrum.[15,16] It was found that the *in situ* SiN_x in this study is Si-rich with a N/Si ratio of 1.21, similar to the reported results in Ref. 17.

Leakage current measurements of the MIS diodes with 3 nm and 7 nm *in situ* SiN_x were carried out, with the samples biased in the accumulation region. Fig. 3 shows the current density (J_L) versus electric field (E_F) plots, along with data of MOS diodes made with various thickness of Al_2O_3. Direct tunneling current was observed for the 3 nm *in situ* SiN_x film, while the film with a thickness of 7 nm shows no significant direct tunneling. On the other hand, the reference sample with 7 nm Al_2O_3 shows direct tunneling phenomenon. Leakage current plots for the thicker Al_2O_3 on conventional AlGaN/GaN heterostructures in Refs. 18 and 19 are also included in Fig. 3 for comparison. At low field, the leakage current of the 7 nm *in situ* SiN_x diode is comparable with that of much thicker Al_2O_3 MOS diodes. The breakdown field (E_{BD}) for the 7 nm *in situ* SiN_x on AlN/GaN heterostructures is around 5.7 MV/cm, as shown in the inset of Fig. 3.

To determine precisely the nature of conduction in the *in situ* SiN_x film, $log(J_L/E_F)$ vs $E_F^{1/2}$ of the 7 nm *in situ* SiN_x sample for E_F up to its breakdown limit is plotted in Fig. 4. It is revealed that the *in situ* SiN_x exhibits a typical silicon nitride behavior.[20–22] The curve can be fitted accurately by the combination of an Ohmic conduction mechanism and a Frenkel-Poole emission mechanism, described by

$$J_L = \frac{E_F}{\rho_{ohm}} \tag{1}$$

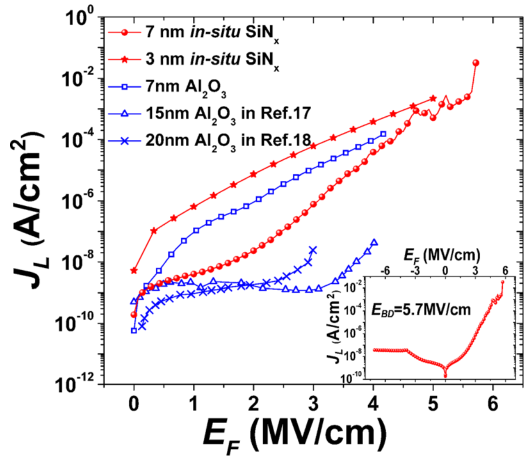

FIG. 3. Leakage current density (J_L) versus electric field (E_F) plots for the *in situ* SiN_x MIS diodes and the Al_2O_3 MOS diodes biased in accumulation region. The inset shows the breakdown field (E_{BD}) of 7 nm *in situ* SiN_x.

and

$$J_L = C \times E_F \times \exp\left\{-\frac{q}{kT}\left[\varnothing_D - \left(\frac{q}{\pi\varepsilon_0\varepsilon_{dyn}}E_F\right)^{1/2}\right]\right\}, \tag{2}$$

respectively. A high resistivity (ρ_{ohm}) of $>10^{14}\ \Omega\cdot$cm was obtained at a field lower than 1.3 MV/cm for the 7 nm *in situ* SiN_x film. The Si-rich *in situ* SiN_x in this study contained relatively high concentrations of Si dangling bonds and distorted excess Si-Si bonds, which may result in midgap defect states or bulk traps inducing more electrical conduction by Frenkel–Poole emission.[20,21] Thus, the resistivity and breakdown field can be further improved by optimizing *in situ* SiN_x growth conditions by MOCVD, such as temperature, pressure, and the gas flow of silane and ammonia, by adjusting the N/Si ratio.

Fig. 5 illustrates the typical double mode capacitance-voltage (*C-V*) characteristics of *in situ* SiN_x/AlN/GaN MIS diodes at two different temperatures, 300 K and 550 K. The measurements were set up with an up-and-down sweep rate of 0.05 V/s and a voltage variation of 50 mV at 100 KHz. A sharp transition from depletion mode to accumulation mode with very small hysteresis for both diodes was observed. The slight temperature shift from 300 K to 550 K suggests

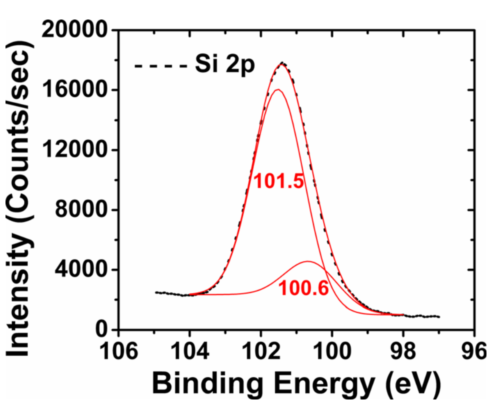

FIG. 2. XPS results of Si2p core-level spectra of the *in situ* SiN_x thin film deposited by MOCVD.

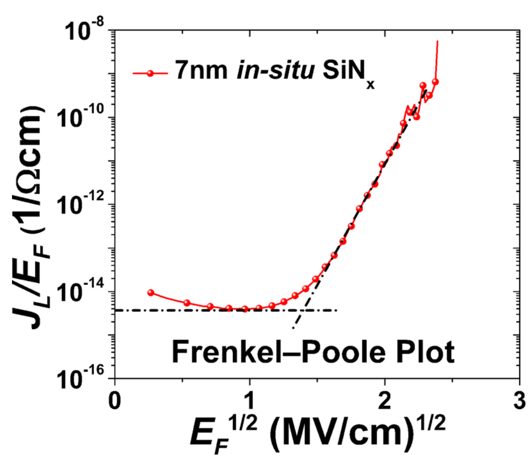

FIG. 4. Frenkel-Poole plot for the MIS diodes with 7 nm *in situ* SiN_x.

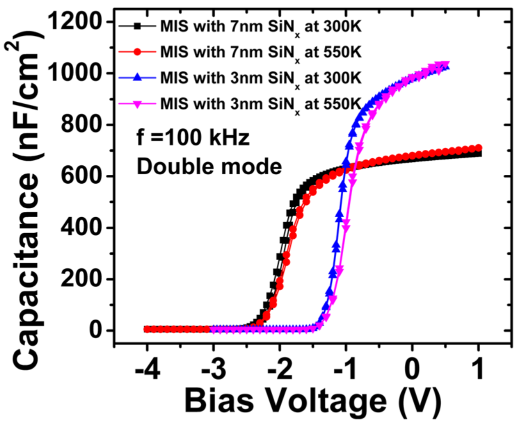

FIG. 5. Double mode *C-V* characteristics of the *in situ* SiN_x/AlN/GaN MIS diodes at 300 K and 550 K.

the presence of a high quality interface between the *in situ* SiN_x layer and the AlN/GaN heterostructure.[19,23] Using the measured capacitances of the MIS diodes with 3 nm and 7 nm *in situ* SiN_x, 1037 nF/cm^2 and 661 nF/cm^2, respectively, and series capacitance combination with the 2DEG accumulation region $1/C_{MIS} = 1/C_{SiN_x} + 1/C_{AlN}$, the capacitance of 7 nm *in situ* SiN_x was determined to be 1042 nF/cm^2. The effective dielectric constant of the *in situ* SiN_x in this work was deduced to be ~8.3, higher than the typical value of 7.5 for stoichiometric Si_3N_4. The higher value could be due to the higher silicon content in the film,[21,22] as determined by the XPS composition analysis.

A frequency dependent conductance analysis was performed in the frequency range of 1 kHz to 1 MHz to evaluate the trapping effects in the *in situ* SiN_x/AlN/GaN MIS diodes. Fig. 6 shows the plot of parallel conductance (G_P/ω) as a function of the radial frequency (ω) for selected gate voltages near the threshold voltage (V_{th}) of the MIS diode with 3 nm *in situ* SiN_x. The trap state density (D_T) and the time constant (τ_T) can be extracted by fitting the experimental $G_P(\omega)$ data using[24]

$$\frac{G_p}{\omega} = \frac{qD_T}{2\omega\tau_T}\ln\left[1 + (\omega\tau_T)^2\right]. \tag{3}$$

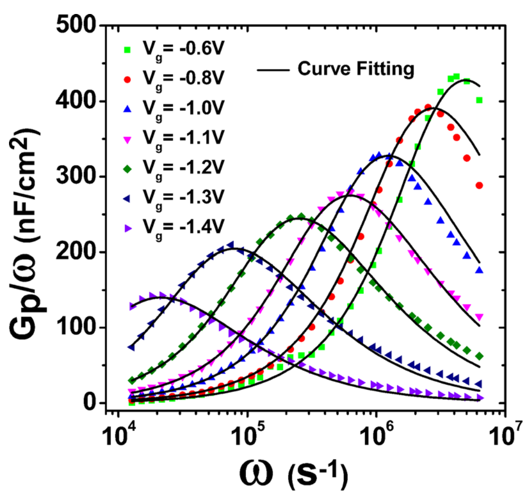

FIG. 6. Frequency dependent parallel conductance as a function of radial frequency for the MIS diode with 3 nm *in situ* SiN_x biased with selected gate voltages near V_{th}.

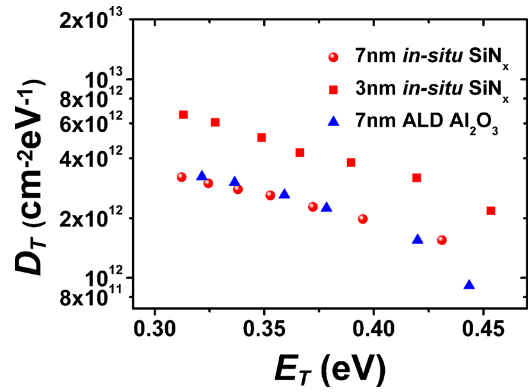

FIG. 7. Trap states density as a function of their energy level depth below conduction band for the MIS and MOS diodes.

A good fitting was obtained, as demonstrated by the continuous curves in Fig. 6, indicating excellent quality of the *in situ* SiN_x gate dielectric.[24,25] The trap energy level below the conduction band, designated as interfacial states (E_T), can be deduced from τ_T by the Shockley–Read–Hall statistics

$$\tau_T = \frac{1}{v_{th}\sigma_n N_c}\exp\left(\frac{E_T}{kT}\right), \tag{4}$$

where $N_c = 4.3 \times 10^{14} \times T^{3/2}\,cm^{-3}$ is the effective density of states in the conduction band in GaN, $\upsilon_{th} = 2 \times 10^7\,cm\,s^{-1}$ is the average thermal velocity of electrons, and $\sigma_n = 1 \times 10^{-14}$ cm^2 is the capture cross section of the trap states.[19,24] The density of trap states (D_T) as a function of their energy (E_T) for the MIS and MOS diodes are shown in Fig. 7. The trap states density for the MIS diodes with 7 nm *in situ* SiN_x decreased from about $7 \times 10^{12}\,cm^{-2}\,eV^{-1}$ at an energy of 0.31 eV to about $1.2 \times 10^{12}\,cm^{-2}\,eV^{-1}$ at $E_T = 0.43$ eV. The value is similar to the trap states density of the reference MOS diodes with 7 nm Al_2O_3, but slightly higher than the reported data on conventional Al_2O_3/AlGaN/GaN structures in Ref. 25. The relatively high trap states density is believed to be stemmed from the low quality thin barrier layer of the AlN/GaN heterostructures grown on a Si substrate. On the other hand, the trap states density for the MIS diodes with 3 nm *in situ* SiN_x is about two times higher than that of the MIS diodes with 7 nm *in situ* SiN_x. This phenomenon has also been observed on Al_2O_3/AlGaN/GaN structures[25] and could be explained by the different surface passivation effects of the SiN_x layers with different thicknesses.[10,26]

In conclusion, MOCVD grown *in situ* SiN_x on AlN/GaN heterostructures has been investigated by AFM, TEM, XPS and electrical characterization of MIS diodes. It was found that the *in situ* SiN_x is Si-rich, with a N/Si ratio of 1.21. The *I-V* and *C-V* characteristics of the *in situ* SiN_x/AlN/GaN MIS diodes exhibit a high resistivity of $>10^{14}\ \Omega\cdot$cm and a breakdown field of 5.7 MV/cm for the 7 nm *in situ* SiN_x film and reveal a high effective dielectric constant of ~8.3. The trap states density for the MIS diodes with 7 nm *in situ* SiN_x was evaluated to be on the order of $10^{12}\,cm^{-2}\,eV^{-1}$ by frequency dependent conductance analysis. The achieved results demonstrate the feasibility of *in situ* SiN_x as gate dielectric for high performance AlN/GaN MIS devices.

This work was supported in part by the Research Grants Council (RGC) theme-based research scheme (TRS) of the Hong Kong Special Administrative Region Government under Grant No. T23-612/12-R. The authors would like to thank Z. Liu, T. Huang, and Q. Li for many helpful discussions and the staff of the NFF and MCPF of HKUST for technical support.

[1]F. Medjdoub, M. Zegaoui, N. Rolland, and P. A. Rolland, Appl. Phys. Lett. **98**, 223502 (2011).
[2]Y. Cao, K. Wang, A. Orlov, H. Xing, and D. Jena, Appl. Phys. Lett. **92**, 152112 (2008).
[3]T. Zimmermann, D. Deen, Y. Cao, J. Simon, P. Fay, D. Jena, and H. G. Xing, IEEE Electron Device Lett. **29**, 661 (2008).
[4]T. Huang, X. Zhu, and K. M. Lau, IEEE Electron Device Lett. **33**, 1123 (2012).
[5]S. Taking, D. MacFarlane, and E. Wasige, IEEE Trans. Electron Devices **58**, 1418 (2011).
[6]T. Huang, X. Zhu, K. M. Wong, and K. M. Lau, IEEE Electron Device Lett. **33**, 212 (2012).
[7]M. Higashiwaki, T. Mimura, and T. Matsui, IEEE Electron Device Lett. **27**, 719 (2006).
[8]D. Deen, D. Storm, D. Meyer, D. S. Katzer, R. Bass, S. Bi-nari, and T. Gougousi, Phys. Status Solidi C **8**, 2420 (2011).
[9]D. A. Deen, S. C. Binari, D. F. Storm, D. S. Katzer, J. A. Roussos, J. C. Hackley, and T. Gougousi, Electron. Lett. **45**, 423 (2009).
[10]X. Lu, J. Ma, Z. Liu, T. Huang, and K. M. Lau, paper presented at International Conference on Nitride Semiconductor, ICNS10 (2013).
[11]E. Cho, S. Seo, C. Jin, D. Pavlidis, G. Fu, J. Tuerck, and W. Jaegermann, J. Vac. Sci. Technol. B **27**, 2079 (2009).
[12]J. Derluyn, S. Boeykens, K. Cheng, R. Vandersmissen, J. Das, W. Ruythooren, S. Degroote, M. R. Leys, M. Germain, and G. Borghs, J. Appl. Phys. **98**, 054501 (2005).
[13]M. Kuroda, T. Murata, S. Nakazawa, T. Takizawa, M. Nishijima, M. Yanagihara, T. Ueda, and T. Tanaka, in Proceedings of IEEE Compound Semiconductor Integrated Circuits Symposium (2008), pp. 1–4.
[14]M. Higashiwaki, Z. Chen, R. Chu, Y. Pei, S. Keller, Y. K. Mishra, N. Hirose, T. Matsui, and T. Mimura, Appl. Phys. Lett. **94**, 053513 (2009).
[15]J. L. Dupuie, E. Gulari, and F. Terry, J. Electrochem. Soc. **139**, 1151 (1992).
[16]E. Bêche, R. Berjoan, J. Viard, B. Cros, and J. Durand, Thin Solid Films **258**, 143 (1995).
[17]E. Ogawa, T. Hashizume, S. Nakazawa, T. Ueda, and T. Tanaka, Jpn. J. Appl. Phys. Part 2 **46**, L590 (2007).
[18]S. Huang, S. Yang, J. Roberts, and K. J. Chen, Jpn. J. Appl. Phys. Part 1 **50**, 110202 (2011).
[19]C. Mizue, Y. Hori, M. Miczek, and T. Hashizume, Jpn. J. Appl. Phys. Part 1 **50**, 021001 (2011).
[20]M. Arps and A. Markwitz, J. Vac. Sci. Technol. A **15**, 1864 (1997).
[21]D. G. Park, M. Tao, D. Li, A. E. Botchkarev, Z. Fan, Z. Wang, S. N. Mohammad, A. Rockett, J. R. Abelson, H. Morkoc, A. R. Heyd, and S. A. Alterovitz, J. Vac. Sci. Technol. B **14**, 2674 (1996).
[22]K. D. Vargheese and G. M. Rao, J. Vac. Sci. Technol. A **19**, 2122 (2001).
[23]M. Miczek, C. Mizue, T. Hashizume, and B. Adamowicz, J. Appl. Phys. **103**, 104510 (2008).
[24]P. Kordos, R. Stoklas, D. Gregusova, S. Gazi, and J. Novak, Appl. Phys. Lett. **96**, 013505 (2010).
[25]P. Kordos, R. Stoklas, D. Gregusova, and J. Novak, Appl. Phys. Lett. **94**, 223512 (2009).
[26]P. Yi, S. Rajan, M. Higashiwaki, C. Zhen, S. P. DenBaars, and U. K. Mishra, IEEE Electron Device Lett. **30**, 313 (2009).