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Growth of ultra-high mobility $In_{0.52}Al_{0.48}As/In_xGa_{1-x}As$ ($x \geq 53\%$) quantum wells on Si substrates using InP/GaAs buffers by metalorganic chemical vapor deposition

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InGaAs quantum wells (QWs) cladded by InAlAs barriers were grown on Si by metalorganic chemical vapor deposition. InP/GaAs/Si buffer templates were first prepared using a two-step growth method. We were able to significantly reduce the dislocation density in the upper InP buffer and obtain smooth surface morphology by fine-tuning the growth parameters and inserting an InGaAs interlayer in the InP buffer. On these InP/GaAs/Si compliant substrates, we investigated InGaAs QWs with various well/barrier parameters and Si-delta doping. We obtained two-dimensional electron gas mobilities over 10,000 $cm^2 V^{-1} s^{-1}$ at 300 K and above 39,000 $cm^2 V^{-1} s^{-1}$ at 77 K on Si substrates.

Since the 1980s numerous efforts, motivated by the monolithic integration of III–V photonic and electronic components with Si based circuitry, have been devoted to the heteroepitaxy of III–V semiconductors on Si substrates.[1–7] Recent advances in the development of III–V n-channel transistors for digital integrated circuits have fueled renewed interest in this research topic.[8–16] Amongst the III–V alloys, $In_{0.52}Al_{0.48}As/In_xGa_{1-x}As$ ($x \geq 53\%$) based transistor technology has exhibited the best balanced high-frequency response,[17] with excellent figures of merit for logic functions.[18,19] In addition, these n-channel devices may be integrated with compressively-strained (In)GaSb p-channel FETs for complementary III–V circuits in the post-Si era.[20] Perfecting the growth of $In_{0.52}Al_{0.48}As/In_xGa_{1-x}As$ ($x \geq 53\%$) quantum well devices on Si substrates will provide numerous benefits. However, epitaxy of these heterostructures on Si is challenging due to the 8% lattice mismatch, large thermal expansion coefficient mismatch and difference in crystal polarities. The resulting high-density defects in the heteroepitaxial layers degrade material properties, adversely affecting device performance and reliability. Recently, using molecular beam epitaxy (MBE) and metal-organic chemical vapor deposition (MOCVD) with metamorphic InAlAs/GaAs buffers, $In_{0.52}Al_{0.48}As/In_xGa_{1-x}As$ ($x \geq 53\%$) quantum wells with Hall mobility comparable to those grown on lattice-matched InP substrates were reported.[21,22] The main drawback of using thick InAlAs/GaAs buffers is the relatively poor thermal conductivity of III–V ternary alloys,[23] which is undesirable for heat dissipation via the buffer to the substrate. An alternative is to use InP or composite InP/GaAs buffer. However, early studies[2–5,12,13,15] of such buffers did not result in ultra-high mobility quantum wells on Si.

In this study, we investigated the MOCVD growth and optimization of the InP/GaAs buffers and ultra-high mobility $In_{0.52}Al_{0.48}As/In_xGa_{1-x}As$ ($x \geq 53\%$) heterostructures on exact Si(001) substrates. We managed the dislocation density in the InP/GaAs buffer by tuning parameters in a two-step growth procedure and inserting an InGaAs interlayer in the middle of the InP buffer. Smooth InP/GaAs/Si buffer templates allowed for the subsequent growth of abrupt and flat InGaAs quantum wells. We were able to achieve room-temperature Hall mobilities above 10,000 $cm^2 V^{-1} s^{-1}$. These are comparable to the best results obtained using metamorphic InAlAs/GaAs buffers on Si substrates, and similar QW structures on InP substrates.

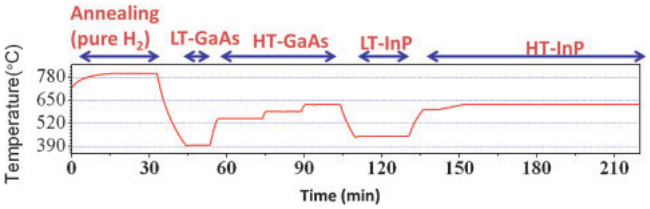

Fig. 1. Growth temperature profile for InP/GaAs composite buffer on Si substrate.

The epitaxy was carried out in an Aixtron AIX-200/4 low-pressure MOCVD system, with a LayTec EpiRAS-2000 system for reflectance anisotropy monitoring. Four-inch p-type exact Si(001) wafers were used for the experiment. Prior to growth, the Si wafer was cleaned in boiling $NH_4OH : H_2O_2 : H_2O$ (1 : 1 : 5) solution to remove surface contamination, followed by a dip in $HF : H_2O$ (1 : 50) solution for 1 min to remove surface native oxides. The wafer was loaded into the MOCVD chamber, heated to ~800 °C and annealed for 30 min at 100 mbar in a pure H_2 ambient to remove the remaining native oxides and promote double-step formation on the Si surface. At the end of the annealing process AsH_3 was introduced and the reactor was cooled down to the buffer growth temperature.

Both GaAs and InP were grown using a two-step procedure: A nucleation layer was first introduced at a relatively low-temperature (LT) in the surface-reaction limited regime, followed by an overgrowth layer at a typical high temperature (HT) in the mass-transport limited regime. The temperature profile is illustrated in Fig. 1. A GaAs nucleation layer, with a fixed V/III ratio of 100, was deposited at a temperature between 390 and 420 °C using triethylgallium (TEGa) and AsH_3 as sources. Then, a 0.5–1 μm thick GaAs buffer was grown with gradual increase in temperature from 550 to 630 °C. Subsequently, an InP buffer was grown on the GaAs/Si template using trimethylindium (TMIn) and PH_3 as precursors. The LT-InP layer was grown at 450 °C, whereas the HT-InP layer was deposited at temperatures ranging from 600 to 630 °C. A 100 nm-$In_{0.58}Ga_{0.42}As$ interlayer was inserted in the HT-InP buffer for dislocation bending and surface smoothing. The 4-in. InP/GaAs/Si template was then cleaved into quarter wafers for subsequent growth of $In_{0.52}Al_{0.48}As/In_xGa_{1-x}As$ ($x \geq 53\%$) heterostructures.

The surface morphology evolution from the buffer to the upper QWs was studied using atomic force microscopy

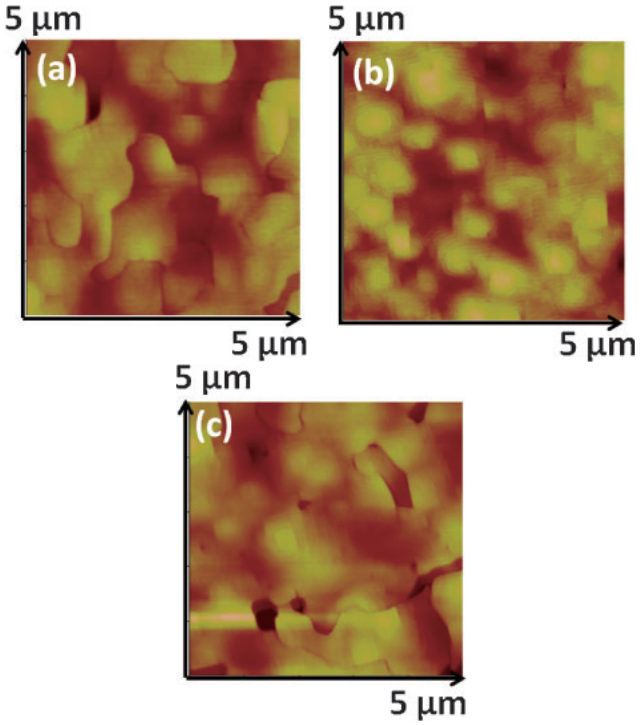

Fig. 2. $5 \times 5\,\mu m^2$ AFM images of GaAs grown on Si with nucleation temperature of 390 (a), 410 (b), and 420 °C (c), and the corresponding RMS value is 1.8, 1.1, and 3.1 nm, respectively.

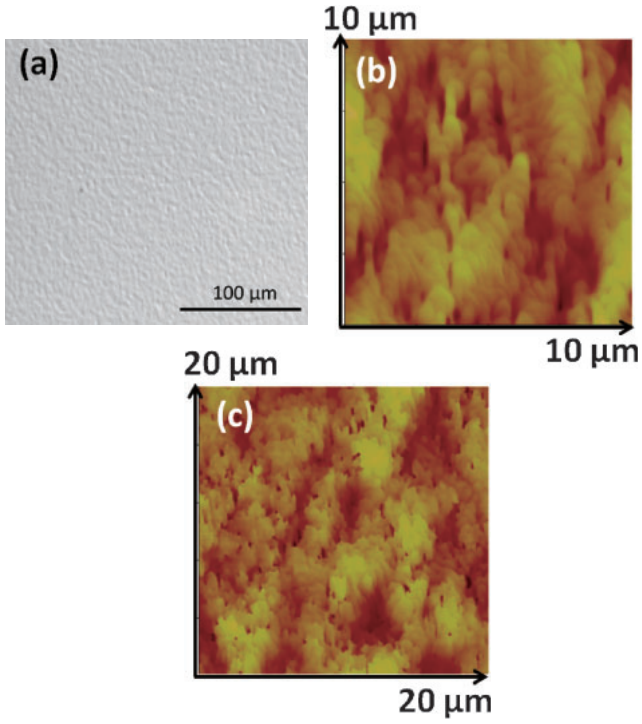

Fig. 3. (a) Optical microscope image of the InP surface. (b) $10 \times 10\,\mu m^2$ AFM image of the InP buffer. (c) $20 \times 20\,\mu m^2$ AFM image of the InAlAs/InGaAs heterostructure.

(AFM). The exact alloy composition and lattice relaxation of the epi-layers was determined by high-resolution x-ray diffraction (HRXRD). Transmission electron microscopy (TEM) was used to investigate the structural properties and crystalline quality. The electron transport properties of the $In_xGa_{1-x}As$ ($x \geq 53\%$) QWs were investigated by Van der Pauw Hall measurements, using ohmic contacts formed by alloyed Indium dots on the InAlAs barrier. The results were benchmarked with those for In-rich InGaAs heterostructures on off-cut Si deposited using InAlAs/GaAs buffers by MBE and MOCVD, as published in the literature.

Figures 2(a)–2(c) display the AFM images of the GaAs buffer for different nucleation deposition temperatures (T_n). It was found that T_n plays a critical role in the self-annihilation of antiphase domain boundaries and elimination of deep pinholes on the GaAs surface. At the optimized T_n of 410 °C, a root-mean-square (RMS) value of 1.1 nm across a 5×5 μm^2 scanned area was achieved, with atomic-step flow as shown in Fig. 2(b). The InP buffer was continuously grown on the GaAs/Si template. The surface morphology of the InP buffer was studied through optical microscopy [Fig. 3(a)] and AFM [Fig. 3(b)]. An RMS roughness of 2.7 nm across a $10 \times 10\,\mu m^2$ scanned area, indicating a smooth InP surface, was determined from the AFM measurement.

Using the InP/GaAs/Si template, a 200 nm LT-$In_{0.52}Al_{0.48}As$ buffer was first grown at 525 °C. Note, the enhanced carbon incorporation at such a low-temperature compensated the n-type background impurities, thereby increasing the resistivity of the InAlAs, which is essential for high-performance transistors. This was followed by the growth of a 100 nm HT-$In_{0.52}Al_{0.48}As$ backside buffer/barrier at a typical temperature of 670 °C to improve the crystalline quality. Figure 4 shows four different QW structure designs. In

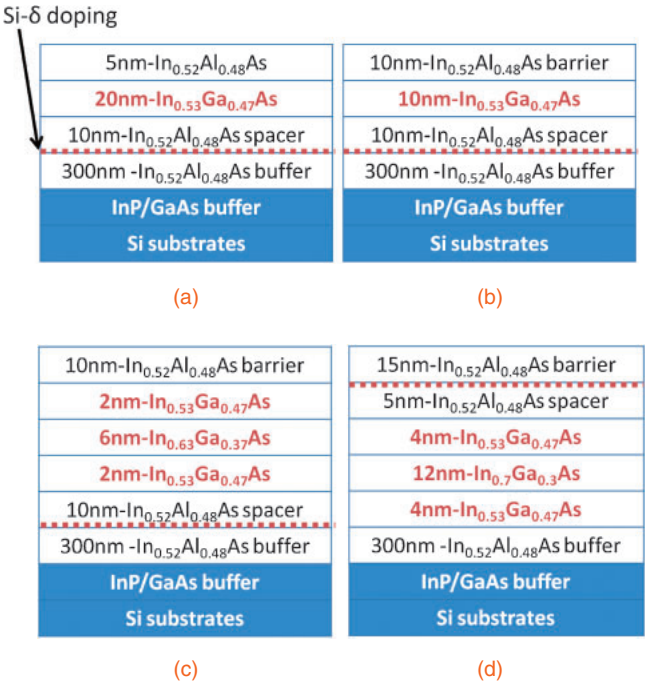

Fig. 4. Four heterostructures with varied channel/barrier and Si-delta doping position: QW-A (a), QW-B (b), QW-C (c), and QW-D (d).

QW-A, QW-B, and QW-C, the heterostructure was reversely doped under the $In_{0.52}Al_{0.48}As$ backside spacer. In QW-D, Si delta-doping was inserted above the $In_{0.52}Al_{0.48}As$ upper spacer. An InGaAs step quantum well with higher Indium content in the core layer was used in QW-C and QW-D for mobility enhancement. This strained $In_xGa_{1-x}As$ ($x > 53\%$) core layer was kept within critical thickness to avoid the

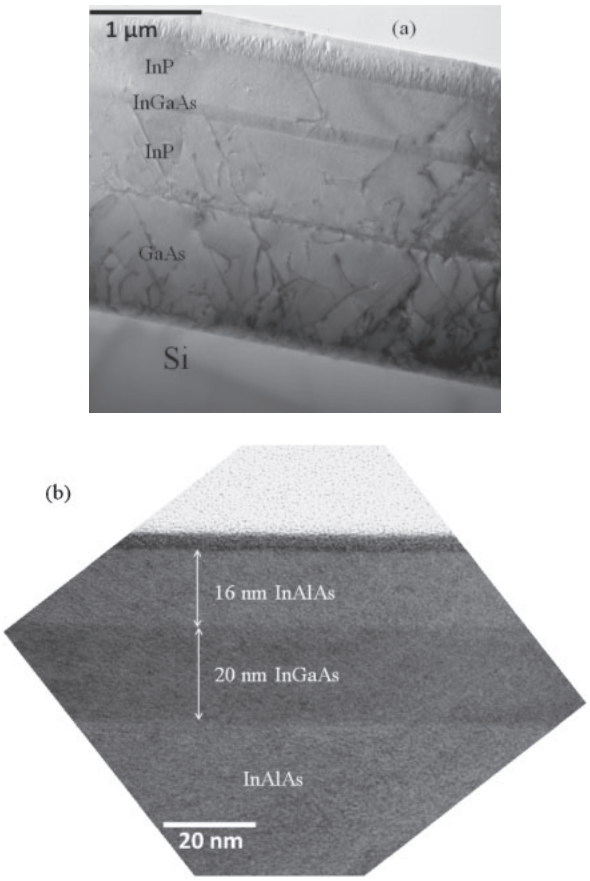

Fig. 5. (a) Cross-sectional TEM image of InGaAs QW on Si with InP/GaAs buffer. (b) High-resolution TEM image of InGaAs QW-D.

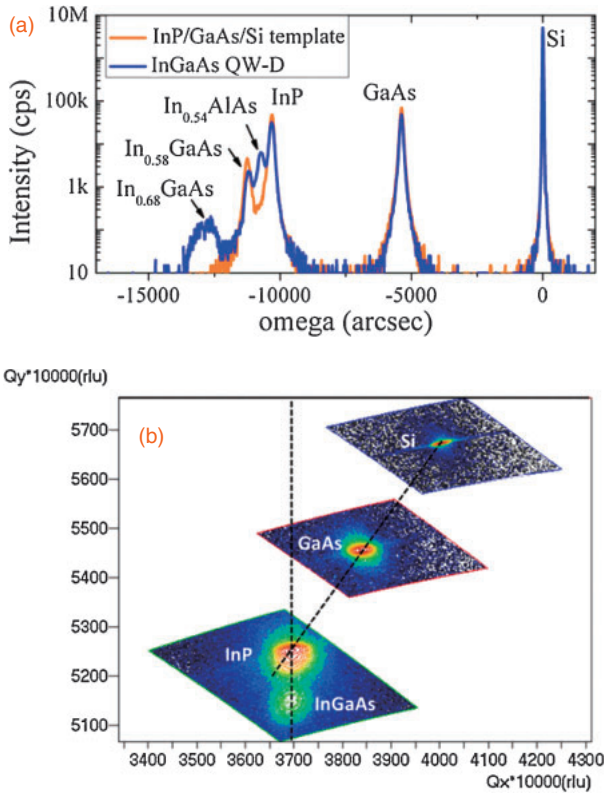

Fig. 6. (a) (004) plane $\omega/2\theta$ coupled scan measured from the InP/GaAs/Si buffer template and from the QW-D on Si. (b) Asymmetric (224) reciprocal space mapping of QW-D.

generation of misfit dislocations at the interfaces. A 20 × 20 μm^2 AFM image of QW-D is displayed in Fig. 3(c). An RMS roughness of 5.0 nm was achieved, and is comparable to the best results reported by MBE.[22)]

Figure 5(a) displays a cross-sectional TEM image of a QW structure with composite InP/GaAs buffer layers on a Si substrate. Many dislocations were generated at both the GaAs/Si and InP/GaAs interfaces due to the 4% lattice mismatch. Nevertheless, most of the defects vanished after they intersected with each other within the growing buffer. The single $In_{0.58}Ga_{0.42}As$ interlayer in the middle of the InP buffer further prevented some of the dislocations from propagating into the upper active layers. A high-resolution TEM image of the InGaAs step quantum-well cladded by InAlAs (corresponding to QW-D) is shown in Fig. 5(b). Abrupt InAlAs/InGaAs interfaces can be observed.

High-resolution X-ray diffraction (XRD) was used to determine the actual alloy composition of the various layers. Figure 6(a) shows the (004) plane $\omega/2\theta$ coupled scan from the InP/GaAs/Si buffer template and from the complete QW-D on Si. The Indium fraction in the channel is around 68% according to XRD fitting, close to the targeted composition. The crystalline quality and lattice relaxation behavior was further investigated by asymmetric (224) reciprocal space mapping (RSM) measurements, and the result is shown in Fig. 6(b). The diffracted intensity spots from GaAs and InP lie on the diagonal line joining the (224) reciprocal lattice point of the Si substrate and the origin of the reciprocal space. This indicates that both the GaAs and InP buffer were fully relaxed. In addition, the diffracted intensity spot from the $In_{0.68}Ga_{0.32}As$ aligns vertically with that from the InP, suggesting a fully strained $In_{0.53}Ga_{0.47}As$ /$In_{0.68}Ga_{0.32}As$ step well.

To characterize the suitability of these heterostructures for transistor applications, Van der Pauw Hall measurements were conducted to obtain the two-dimensional electron gas (2DEG) density and mobility at 300 and 77 K. Figure 7(a) plots the electron mobility at 300 K as a function of the carrier density measured from the four sets of QWs shown in Fig. 4. Identical InAlAs/InGaAs heterostructures grown on GaAs substrates using InP buffers were also studied for comparison. For QW-A, QW-B, and QW-C, the electron mobilities were found to be 10–20% lower on Si than those on GaAs substrates. We found that increasing the InAlAs upper barrier thickness and incorporating a higher Indium content in the QW substantially enhanced the mobility of the reversely doped heterostructure on Si from ~4000 cm^2 V^{-1} s^{-1} in QW-A to above 8000 cm^2 V^{-1} s^{-1} in QW-C. For the QW-D structure, multiple samples with varying doping concentration were grown on Si with SiH_4 flow rate increasing from 1.2×10^{-5} to 1.4×10^{-5} mol/min. Room-temperature mobilities above 10,000 cm^2 V^{-1} s^{-1} have been achieved on both GaAs and Si substrates. The electron mobilities of QW-C and QW-D we obtained were benchmarked with the best results in literature as demonstrated by InAlAs/InGaAs high-electron-mobility transistors on Si substrates using metamorphic InAlAs/GaAs buffers.[21,22)] As shown in Fig. 7(b), 2DEG with Hall mobility of 10,080 cm^2 V^{-1} s^{-1} at 300 K and 39,600 cm^2 V^{-1} s^{-1} at 77 K was achieved by QW-D with a high carrier density suitable for

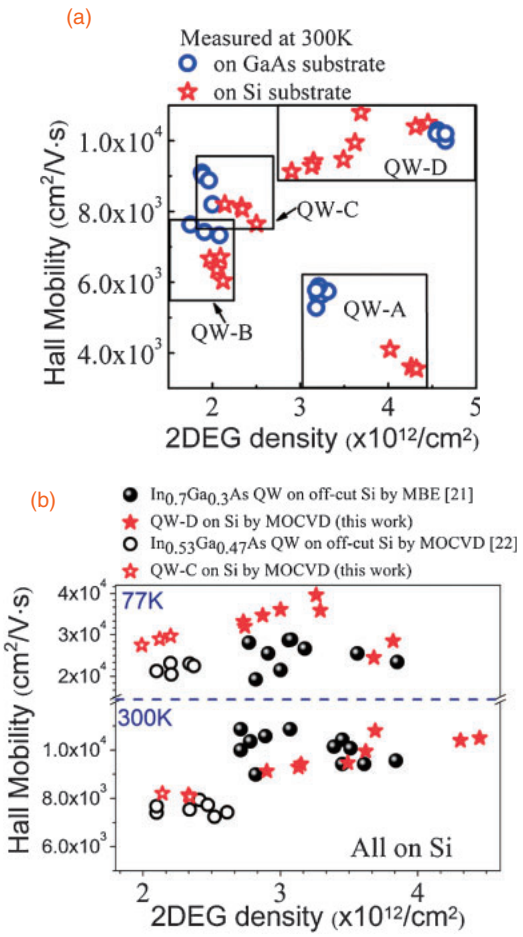

Fig. 7. (a) Comparison of electron mobility measured from four sets of QWs on GaAs and Si substrates at 300 K. (b) Benchmarking of electron mobility of QWs on Si at 300 and 77 K.

device applications. The ultra-high mobility led to a sheet resistance as small as 157 Ω/□ at 300 K and 48 Ω/□ at 77 K.

In conclusion, in this study we demonstrated heteroepitaxy of ultra-high mobility $In_{0.52}Al_{0.48}As/In_xGa_{1-x}As$ ($x \geq 53\%$) quantum wells on on-axis Si(001) substrates, using InP/GaAs buffers, by metalorganic chemical vapor deposition. The material properties and crystalline quality were studied using AFM, TEM, XRD, and Hall measurements. The high electron mobilities achieved in this work indicate excellent electron transport properties in these heterostructures on Si, which could be useful for monolithic integration of III–V electronic devices with Si complementary metal–oxide–semiconductor circuitry.

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