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In situ growth of SiN_x as gate dielectric and surface passivation for AlN/GaN heterostructures by metalorganic chemical vapor deposition

Jun Ma, Xing Lu, Huaxing Jiang, Chao Liu, and Kei May Lau*

Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Clear Water Bay, Kowloon, Hong Kong
E-mail: eekmlau@ust.hk

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SiN_x grown in situ by metalorganic chemical vapor deposition (MOCVD) has shown great potential as a high-quality gate dielectric and surface passivation for AlN/GaN heterostructure transistors. In this paper, we present a thorough study on how the growth conditions affect the film quality of SiN_x and correlate the observed material properties with the electrical characteristics of the heterostructures. Lowering the growth pressure and SiH₄/NH₃ ratio can improve the SiN_x/AlN interface roughness, leading to a reduced interfacial trap state density. The gate leakage current can be suppressed by increasing the resistivity of SiN_x, which can be tailored with growth temperature and SiH₄/NH₃ ratio.

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II-nitride-based high-electron-mobility transistors (HEMTs) have shown great potential for radio frequency/microwave power applications. To achieve higher speed and lower power operations, the scaling of transistor dimensions has recently been widely studied.^{1–4} However, short channel effects become an issue as the gate length decreases.^{5,6} Better gate control by reducing the gate-to-channel distance is therefore desirable. AlN/GaN heterostructures are promising because a well-confined, high-concentration two-dimensional electron gas (2DEG) can be achieved with only a few nanometers of AlN barrier.^{7–9} Nevertheless, AlN/GaN transistors typically exhibit a large gate leakage owing to defects in the AlN layer.^{10–12} Moreover, significant degradation in channel conductivity can occur as a result of barrier layer relaxation during the postgrowth cooling.^{13,14} Various schemes have been proposed to overcome these challenges by surface passivation.^{15–18} Among all the material systems, SiN_x is a very promising candidate since it can effectively reduce the relaxation of AlN^{14,19} and can be deposited in situ during the device growth by metalorganic chemical vapor deposition (MOCVD).²⁰ Moreover, the high-temperature in situ deposition can result in a high-quality dielectric and reduce interface traps when compared with other ex situ dielectrics deposited at much lower temperatures.^{21,22} Despite all the potential advantages, the successful demonstration of suppressed gate leakage in AlN/GaN devices passivated with in situ SiN_x is uncommon.^{14,23} Higashiwaki et al. even found that devices passivated with in situ SiN_x can have a larger gate leakage than those passivated with ex situ SiN_x.²⁴ It is therefore of great importance to study the growth behavior of SiN_x by MOCVD so that the full potential of the in situ passivation dielectric layer can be exploited.

In this letter, we report a thorough study of the in situ deposition of SiN_x by MOCVD. We studied the effect of various growth conditions on the film quality and correlated the observed material properties with the electrical characteristics of SiN_x/AlN/GaN diode structures. Notably, low growth pressure and SiH₄/NH₃ ratio favor the growth of a perfectly smooth SiN_x/AlN interface, which is crucial for the reduction of the interfacial trap density. In addition, elevated growth temperature and NH₃ partial pressure greatly improve the resistivity of the SiN_x passivation layer. This efficiently suppresses the gate leakage current across the heterostructure. The results presented here reveal the potential for high-

quality in situ SiN_x as an effective passivation and dielectric layer for ultrathin-barrier AlN/GaN transistors.

The SiN_x/AlN/GaN HEMT structures were grown on Si(111) substrates in an Aixtron 2000HT MOCVD reactor. Details of the AlN/GaN heterostructure growth have been reported elsewhere.¹⁶ After the 1.5 nm AlN barrier layer, the SiN_x cap layer was deposited in situ under various growth conditions, using SiH₄ and NH₃ as precursors. We focused on studying three major growth parameters—temperature (*T*), pressure (*P*), and SiH₄/NH₃ ratio (*R*). Transmission electron microscopy (TEM), atomic force microscopy (AFM), and X-ray photoelectron spectroscopy (XPS) were used to study the material properties of the heterostructures. Circular metal-insulator-semiconductor (MIS) diodes were fabricated to characterize the electrical properties of the devices with in situ SiN_x as the passivation layer and gate dielectric. Device isolation was achieved through mesa etching, using CF₄/O₂-based reactive ion etching (RIE) and Cl₂-based inductively coupled plasma (ICP) etching. Ti/Al/Ni/Au ohmic electrodes were formed after the selective removal of the in situ SiN_x cap by RIE. A circular metal gate (Ni/Au) of 200 μm diameter was formed on the in situ SiN_x by e-beam evaporation.

The SiN_x deposition rate dependence on the three growth parameters (*T*, *P*, and *R*) was first explored. The thickness of the in situ SiN_x was measured by cross-sectional TEM. The nominal deposition rate was then obtained by normalizing the thickness with the corresponding growth time. Figure 1(a) shows the deposition rate plotted as a function of growth temperature. A sharp increase in the deposition rate was observed when *T* was increased from 1080 to 1145 °C, resulting from the elevated reaction rate. A further increase in temperature, however, enhances parasitic gas phase reactions as well as the premature decomposition of SiN_x, leading to a drop in the deposition rate at 1175 °C. This temperature dependence is different from the low-pressure chemical vapor deposition (LPCVD) of SiN_x using the SiH₄-NH₃ system²⁵ because the in situ deposition is mass-transport-limited at high deposition temperature. The dependences of deposition rate on pressure and SiH₄/NH₃ ratio, on the other hand, are much more straightforward. As shown in Figs. 1(b) and 1(c), the deposition rate increases linearly with *P* and *R* [Figs. 1(b) and 1(c)]. This is consistent with that reported for the LPCVD deposition of SiN_x.^{25,26}

In addition to the growth rate, it is crucial to understand how the material quality varies with the three important

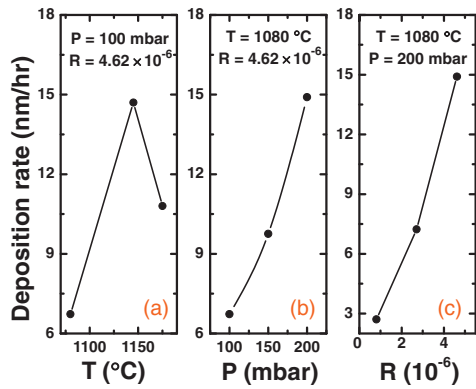


Fig. 1. Dependences of deposition rate on (a) temperature, (b) pressure, and (c) SiH_4/NH_3 ratio.

Table I. Growth parameters of SiN_x in samples A–D.

| | Temperature ($^{\circ}\text{C}$) | Pressure (mbar) | SiH_4/NH_3 ($\times 10^{-6}$) |
|---|---------------------------------------|--------------------|--|
| A | 1080 | 200 | 4.62 |
| B | 1080 | 100 | 4.62 |
| C | 1145 | 100 | 4.62 |
| D | 1145 | 100 | 3.16 |

growth parameters. In the following, we focus on correlating the material and electrical properties of four $\text{SiN}_x/\text{AlN}/\text{GaN}$ heterostructures (labeled A to D) with the SiN_x layer (5–7 nm) grown under various conditions toward optimized device performance. Details of the growth parameters are summarized in Table I. The abruptness of the SiN_x/AlN interface has a profound impact on the electrical performance of the device. To study the interface, we performed high-resolution TEM on the four $\text{SiN}_x/\text{AlN}/\text{GaN}$ heterostructures, as shown in Fig. 2. Note that the images were taken near the GaN [1100] zone axis. Sample A exhibits a bumpy interface with the SiN_x/AlN boundary not very well defined [Fig. 2(a)]. Energy-dispersive X-ray spectroscopy showed that the bumps are composed of Al(Ga)N. The interface roughness is due to the etching effect of SiH_4 on III–nitride.²⁷⁾ Initially, SiN_x deposits as a discontinuous fractal film on top of the AlN barrier layer. The porous film then acts as the mask for selective SiH_4 etching of the Al(Ga)N. The etch pits are then covered by the subsequently deposited SiN_x , thus resulting in the observed bumpy interface. To suppress this SiH_4 etching, one choice is to adopt a temperature much lower than 1080 $^{\circ}\text{C}$ for the SiN_x growth.²⁸⁾ However, the AlN layer, grown at 1145 $^{\circ}\text{C}$, can partially relax during the cooling between the AlN and SiN_x growths.¹⁹⁾ Instead of slowing down the self-etching, a better interface can be obtained by promoting the lateral growth of SiN_x for better coverage uniformity at the early stages. It can be seen that the interface roughness was considerably reduced by lowering the pressure to 100 mbar in sample B [Fig. 2(b)]. The average depth and diameter of the etch-induced pits were also reduced from about 7 and 37 nm to approximately 3 and 7 nm, respectively. This is attributed to the enhanced adatom mobility at reduced pressure. Although sample B exhibits a much smoother interface, the low SiN_x growth temperature (1080 $^{\circ}\text{C}$) is undesirable since the temperature ramp-down can adversely affect the quality of the high-temperature AlN barrier layer. Therefore, we increased the growth temperature

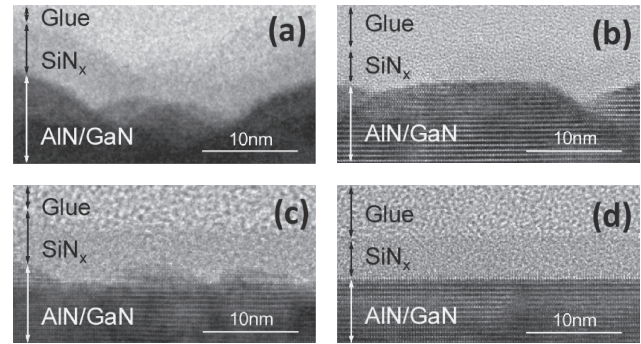


Fig. 2. Cross-sectional TEM images of samples (a) A, (b) B, (c) C, and (d) D.

of SiN_x to that of AlN (i.e., 1145 $^{\circ}\text{C}$) in sample C, under a reactor pressure of 100 mbar. Unfortunately, the interface became rough again owing to the faster SiH_4 etching at elevated temperature [see Fig. 2(c)]. While the depth of the etching-induced pits does not change much, the diameter and density of the pits increase. Finally, a completely smooth interface was achieved at a reduced SiH_4/NH_3 ratio, as shown in Fig. 2(d). The higher NH_3 partial pressure further improves the lateral growth of the SiN_x and suppresses the decomposition of the AlN. The interface quality strongly correlates with the device performances, and will be discussed in more detail below.

In addition to interface abruptness, it is also of great importance to provide a smooth surface morphology for device fabrication. Another four samples (A1, B1, C1, and D1) were grown under the same growth conditions as samples A, B, C, and D, respectively. The thickness of the in situ SiN_x in samples A1–D1 was set to be 3 nm to ensure a fair comparison of the surface morphology as well as a full SiN_x coverage for the following device fabrication and comparison. Surface morphologies are observed to be highly correlated with the interface roughness. Sample A1 shows a rather rough surface as a result of poor lateral growth owing to the limited adatom surface migration. By enhancing the lateral growth at lower pressure, the root-mean-square (RMS) roughness across a $5 \times 5 \mu\text{m}^2$ area was reduced to 0.80 nm in sample B [Fig. 3(b)]. As the growth temperature increases to 1145 $^{\circ}\text{C}$ in sample C, the surface roughness increases to 1.52 nm [Fig. 3(c)] owing to enhanced SiH_4 etching. The surface becomes completely smooth when the SiH_4/NH_3 ratio decreases to 3.16×10^{-6} , as shown in Fig. 3(d). The observed morphologies agree well with the interface roughness observed by cross-sectional TEM, and can probably affect the channel mobilities of lateral transistors.

$\text{SiN}_x/\text{AlN}/\text{GaN}$ MIS diodes were fabricated with the four samples (A1–D1). I – V characteristics of the MIS diodes were plotted with an AlN/GaN Schottky diode as a reference, as shown in Fig. 4. All of the MIS diodes exhibit significantly smaller gate leakage currents than the Schottky diode, attesting to the leakage suppression capability of SiN_x . While samples A1 and B1 show similar reverse leakage currents ($\sim 10^{-3}$ A/cm²), samples C1 and D1 have leakage currents reduced to be 4.6×10^{-5} and 3.0×10^{-6} A/cm² at -5 V, respectively. This is because the leakage current is closely related to the stoichiometry of the SiN_x film. XPS analysis revealed that the N/Si ratios of samples A1–D1 were 1.12, 1.13, 1.19, and

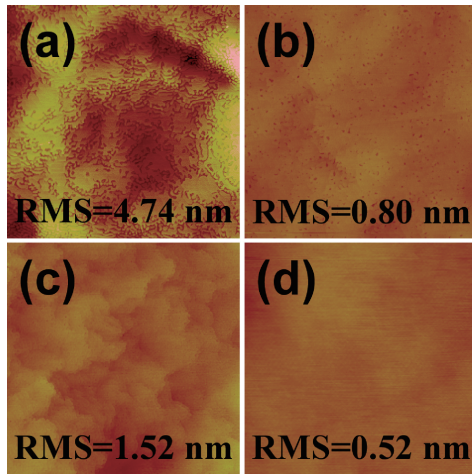


Fig. 3. AFM images ($5 \times 5 \mu\text{m}^2$) showing surface morphologies of the four samples. (a)–(d) correspond to samples A1–D1, respectively.

1.23, respectively. Samples C1 and D1 show considerably higher N/Si ratios than samples A1 and B1. While the stoichiometry is not sensitive to growth pressure, raising the temperature from 1080 to 1145 °C effectively boosts up the nitrogen content in the in situ passivation layer, likely owing to the enhanced NH_3 decomposition efficiency at higher temperature. The N/Si ratio further increases with a smaller SiH_4/NH_3 ratio as a result of a higher NH_3 partial pressure (sample D1). Studies have shown that a higher N/Si ratio increases the bandgap and decreases the number of Si dangling bonds of the amorphous film.^{29–31} Therefore, an enhancement in nitrogen composition increases the resistivity of the SiN_x film. This explains the observed leakage current improvements of sample D1 compared with those of the other MIS diodes.

To explore the dielectric constant of the in situ SiN_x , capacitance–voltage (C – V) characteristics of samples A1–D1 were measured at a frequency of 1 MHz. The capacitances of the MIS diodes (C_{MIS}) at the accumulation region for samples A1–D1 were determined to be 947, 832, 1037, and 878 nF/cm², respectively. In our previous work, C_{AIN} was found to be 1807 nF/cm² (corresponding to sample C1).³² Using $1/C_{\text{MIS}} = 1/C_{\text{AIN}} + 1/C_{\text{SiN}_x}$ and assuming that the four samples share the same C_{AIN} , the dielectric constant of SiN_x in samples A1–D1 was calculated to be 6.7, 5.2, 8.2, and 5.8, respectively. However, the calculated results are not reasonable or consistent with their Si/N ratio obtained by the XPS measurement.³³ We believe that this is due to the mistaken assumption of the same C_{AIN} for samples A1, B1, and D1. From the AFM and TEM observations, the AlN barriers of the four samples have different surface roughnesses and probably also different thicknesses, owing to the different SiH_4 etching effects. Therefore, the C_{AIN} values for the four samples should not be simply treated as the same and may not be accurately estimated in this experiment. On the other hand, the C – V plots of samples A1 and C1 in the accumulation region were found to be not as flat as those of samples B1 and D1. This could also be explained by the more severe SiH_4 etching effects on the AlN barriers in samples A1 and C1. The AlN barriers in samples A1 and C1 are therefore leakier, which leads to another obstacle for the accurate determination of C_{AIN} . Consequently, the current calculation method is not suffi-

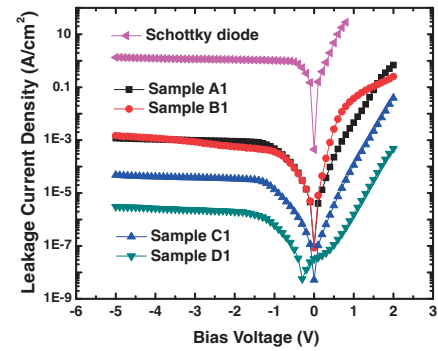


Fig. 4. I – V characteristics of the fabricated MIS diodes.

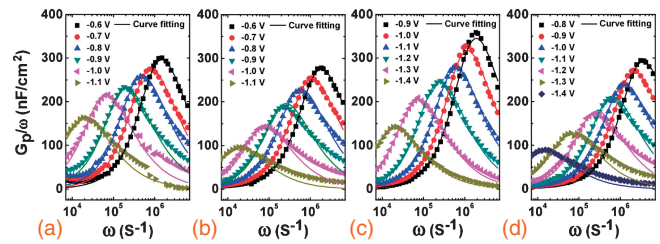


Fig. 5. Frequency-dependent parallel conductance as a function of radial frequency of the MIS diodes biased with selected gate voltages near V_{th} for samples (a) A1, (b) B1, (c) C1, and (d) D1.

ciently reliable for determining the dielectric constant of the in situ SiN_x . To eliminate the impact of the variation of AlN barriers and the inaccurate estimation of C_{AIN} , two samples with different SiN_x thicknesses grown under the same growth conditions have to be prepared in another study.³²

In addition to the leakage current, the trap state density has a significant impact on transistor performances. The trap states of the four samples were characterized and investigated by frequency-dependent conductance analysis.^{34,35} The trap state density (D_{T}) and time constant (τ_{T}) can be extracted through fitting the measured parallel conductance $G_{\text{P}}(\omega)$ data using

$$\frac{G_{\text{P}}}{\omega} = \frac{qD_{\text{T}}}{2\omega\tau_{\text{T}}} \ln[1 + (\omega\tau_{\text{T}})^2]. \quad (1)$$

Fitted curves are shown in Fig. 5. The trap energy level below the conduction band (E_{T}) can be deduced from τ_{T} using the Shockley–Read–Hall statistics

$$\tau_{\text{T}} = \frac{1}{v_{\text{th}}\sigma_{\text{n}}N_{\text{c}}} \exp\left(\frac{E_{\text{T}}}{kT}\right), \quad (2)$$

where $N_{\text{c}} = 4.3 \times 10^{14} \times T^{3/2} \text{ cm}^{-3}$ is the effective density of states in the conduction band in GaN, $v_{\text{th}} = 2 \times 10^7 \text{ cm} \cdot \text{s}^{-1}$ is the average thermal velocity of electrons, and $\sigma_{\text{n}} = 1 \times 10^{-14} \text{ cm}^2$ is the capture cross section of the trap states.^{31,36} D_{T} values of the four samples are plotted as a function of E_{T} in Fig. 6. Interestingly, the trap state densities of samples B1 and D1 are lower than those of samples A1 and C1, which is in good consistency with the interface characteristics presented in Fig. 2. This phenomenon indicates that the interface roughness induces trap states at the insulator/semiconductor interface. In the presence of etching-induced pits, the Ehrlich–Schwoebel barrier reduces the mobility of SiN_x adatoms on the uneven morphology.^{37–39} Incomplete coverage of SiN_x leads

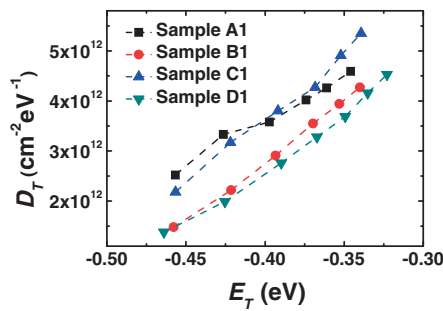


Fig. 6. Trap state densities of MIS diodes plotted as a function of their energy level depth below conduction band.

to a high density of dangling bonds and hence interface trap states on the unpassivated Al(GaN) surfaces. With the smoothest interface and the highest N content in the in situ SiN_x film, sample D1 exhibits the lowest trap state density and gate leakage current, underscoring its potential for high-performance AlN/GaN transistors.

In conclusion, we investigated the in situ growth of SiN_x for gate insulation and surface passivation of AlN/GaN heterostructures. The SiN_x/AlN interface quality and surface morphology depend strongly on the growth temperature, pressure, and SiH₄/NH₃ ratio. A lower growth pressure and a higher NH₃ partial pressure can reduce the interface roughness through enhanced lateral growth of the amorphous film, thereby reducing the interface trap state density. In addition, the stoichiometry of SiN_x plays an important role in the resistivity of the film. By increasing the growth temperature and decreasing the SiH₄/NH₃ ratio, the N/Si ratio was boosted and thus the resistivity of the film was improved. We observed a prominent suppression of the gate leakage in the SiN_x/AlN/GaN MIS diodes with SiN_x with higher N content. The results presented here are useful not only for achieving high-quality in situ SiN_x as a gate dielectric and a surface passivation layer for ultrathin-barrier AlN/GaN MISHEMTs, but also for any applications that require high-quality in situ SiN_x, e.g., masked growth of GaN for dislocation reduction.

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