Material and Device Characteristics of Metamorphic $In_{0.53}Ga_{0.47}As$ MOSHEMTs Grown on GaAs and Si Substrates by MOCVD

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***Abstract*— We report a comparison of material and device characteristics of metamorphic $In_{0.53}Ga_{0.47}As$ channel metal–oxide–semiconductor high-electron mobility transistors (MOSHEMTs) grown on GaAs and Si substrates by metal–organic chemical vapor deposition. A gate-last process was developed to simplify the fabrication of nanoscale channel length devices. Selective source/drain regrowth was incorporated to reduce parasitic resistances. Post-metallization annealing (PMA) was utilized to mitigate the weakened gate electrostatic control in the buried channel. The effect of PMA on the Ti/Al_2O_3 gate-stack was investigated in detail. Record-low ON-state resistance of 132 and 129 $\Omega \cdot \mu$m has been achieved in enhancement-mode InGaAs MOSHEMT on GaAs and on Si substrate, respectively. A 120-nm channel length device on GaAs exhibited a figure of merit Q (g_m/SS) of 12, whereas a 60-nm channel length $In_{0.53}Ga_{0.47}As$ MOSHEMT on Si demonstrated Q up to 14.**

***Index Terms*— High-electron mobility transistors, metal–oxide–semiconductor, post-metallization annealing and selective source/drain regrowth.**

I. Introduction

BECAUSE of inherent excellent transport properties, InGaAs channel high-electron mobility transistors (HEMTs) have demonstrated outstanding high-frequency performance as indicated by their high f_t and $f_{\max}$ [1]–[3], making them attractive for terahertz electronics. Recent advances in incorporating high-k gate dielectrics on III–V compounds have also enabled InGaAs metal-oxide-semiconductor field effect transistors (MOSFETs) with high current deliverability and good scalability [4]–[13] appealing for post-Si logic applications. Traditionally, these transistors are epitaxially grown on lattice-matched InP substrates, relatively more expensive and mechanically vulnerable in large sizes. Fabricating similar high-performance devices on GaAs or Si can take advantage of larger and more robust wafers, thereby lowering the manufacturing cost. In addition, monolithic integration of advanced compound semiconductor devices on Si can eventually enable single-chip integration of RF communication and logic blocks on a system-on-chip platform [14]. Previously, we have reported 120-nm channel length ($L_{\rm ch}$) $In_{0.53}Ga_{0.47}As$ MOSHEMTs on GaAs exhibiting peak transconductance ($g_{m,\max}$) of 1126 mS/mm at $V_{\rm ds} = 0.5$ V with an ON-state resistance ($R_{\rm ON}$) of 156 $\Omega \cdot \mu$m [15]. Due to the presence of relatively thick InAlAs upper barrier, high effective carrier mobility was obtained. However, the downside of this structure is the weakened gate electrostatic control over the buried InGaAs channel. Recently, a low-pressure post-metallization annealing (PMA) process was developed by our group to enhance gate electrostatic control and achieve enhancement-mode MOSHEMTs on Si substrates [13]. In this paper, similar PMA was applied to $In_{0.53}Ga_{0.47}As$ MOSHEMTs with regrown source/drain (S/D) on GaAs substrates. Both material and device characteristics were presented and compared with those obtained from devices on Si substrates. The effects of PMA on the gate-stack were analyzed using transmission electron microscopy (TEM), secondary ion mass spectrometry (SIMS), and X-ray photoelectron spectroscopy (XPS). Benchmarking the figure of merit Q, transconductance to subthreshold slope ratio (g_m/SS) [16] with state-of-the-art $In_xGa_{1-x}As$ ($x \geq 53\%$) MOSFETs, the device results of $In_{0.53}Ga_{0.47}As$ MOSHEMTs on GaAs and Si substrates in this paper are comparable with the best achieved by planar $In_{0.7}Ga_{0.3}As$ or InAs quantum well-channel MOSFETs on lattice-matched InP substrates at the 100-nm gate length regime.

II. Material Characterization and Device Fabrication

The epitaxy in this paper was carried out in a commercial low-pressure MOCVD system (AIX200/4) with a horizontal reactor. InP buffer templates were grown on 4-in exact (100) orientated GaAs or Si substrates using a two-temperature step method [17]. A 60-nm $In_{0.53}Ga_{0.47}As$ interlayer was inserted in the InP buffer for dislocation filtering and surface smoothing. After surface characterization, the InP/GaAs and InP/GaAs/Si templates were cleaved for subsequent growth runs of inverted-type $In_{0.53}Ga_{0.47}As$ HEMT structure with reverse modulation doping under an $In_{0.52}Al_{0.48}As$ backside spacer. From bottom to the top, the device active layers include 400-nm $In_{0.52}Al_{0.48}As$ back buffer/barrier, Si delta doping using SiH_4, 10-nm $In_{0.52}Al_{0.48}As$ backside spacer, 10-nm InGaAs channel, and 10-nm $In_{0.52}Al_{0.48}As$ undoped upper barrier. Here, the nominal thickness of various

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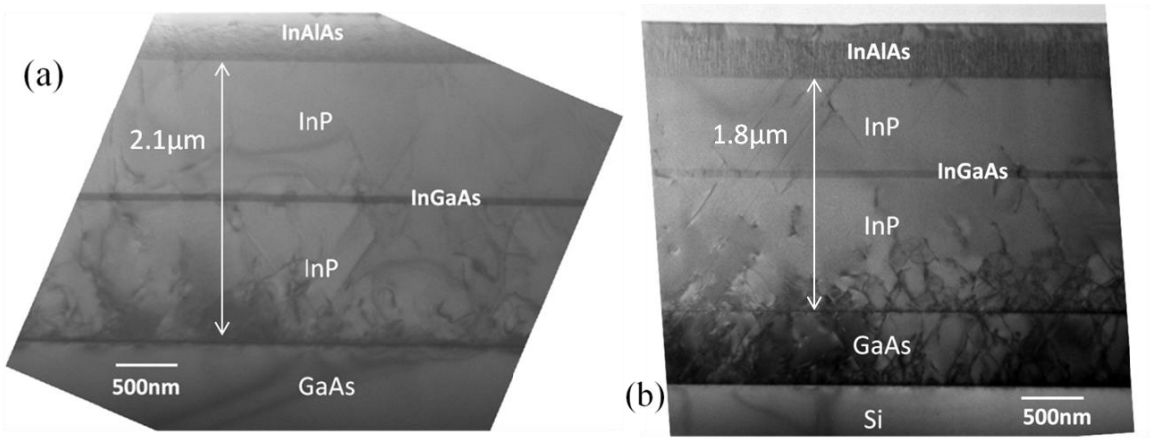

Fig. 1. Cross-sectional TEM images of inverted InGaAs HEMTs grown on (a) GaAs and (b) Si substrates.

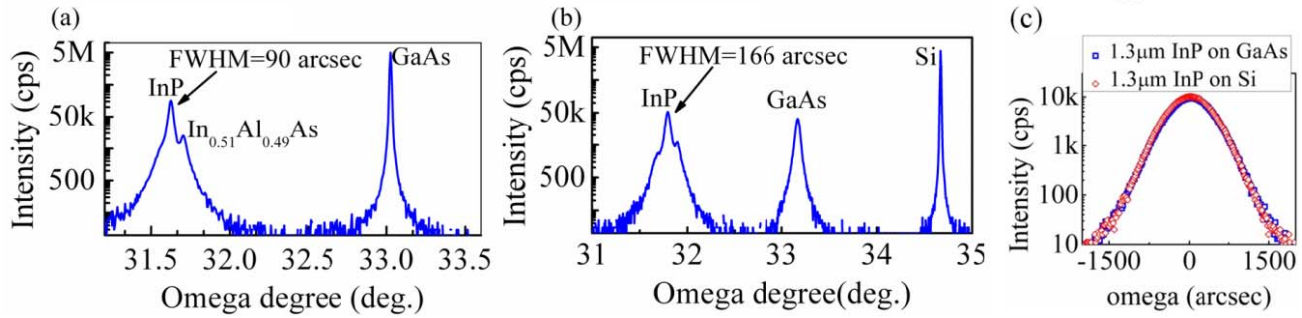

Fig. 2. (a)–(c) High-resolution XRD (004) plane $\omega/2\theta$ curve for the complete device stack epitaxially grown on GaAs and Si substrates, as well as ω-rocking curve comparison of InP buffer grown on GaAs and Si substrates. (a) On GaAs substrate. (b) On Si substrate. (c) ω-rocking curve.

layers was estimated based on calibrated growth rates. Fig. 1(a) and (b) shows the cross-sectional TEM images of the inverted HEMT grown on GaAs and Si, respectively. The dislocation density was significantly reduced in the upper InP buffer.

Fig. 2(a) and (b) shows high-resolution X-ray diffraction (HRXRD) (004) plane $\omega/2\theta$ scans of the complete device stack on two different substrates. Although the nominal device layer structure is lattice matched to InP, there were minor deviations as shown by the shoulders around the InP peak in the XRD $\omega/2\theta$ scans. Nevertheless, the full-width at half-maximum (FWHM) values of the InP peak determined from the HRXRD $\omega/2\theta$ curves were 90 and 166 arcsec on GaAs and Si, respectively. To quantify the threading dislocation density (D) of the InP buffer, HRXRD (004) plane ω-rocking curves were measured. The FWHM of the ω-rocking curve can be related to D (cm^{-2}) through Ayers' model [18]

$$\mathrm{D} = \frac{\beta^2}{4.36b^2}$$

where β is the FWHM in radians, b is the length of burgers vector of dislocation. For 60° dislocations in InP, $b = \sqrt{2}a/2$, where $a = 5.87$ Å is the lattice constant of InP. D provides an estimate of upper limit of dislocation density in the InP. A comparison of ω-rocking curve measured from 1.3-μm InP buffer on different substrates was shown in Fig. 2(c). The two curves overlap with each other, suggesting the same dislocation density ($D = 2.1 \times 10^9$ cm^{-2}) for both InP buffers of equal thickness grown on GaAs and Si substrates. Dislocation density was further reduced to 1.5×10^9 cm^{-2} with a thicker (1.8 μm) InP buffer. It should be noted that the dislocation density deduced is an average over all the epitaxial layers that could be significantly higher from the dislocation density at the surface, as indicated by the cross-sectional TEM in Fig. 1.

The quality of the InP buffers was further assessed by the electron transport properties of InAlAs/InGaAs heterostructures grown on top. Van der Pauw Hall measurement was performed by alloying indium contacts to the InAlAs barrier. As shown in Table I, for inverted $In_{0.53}Ga_{0.47}As$ channel HEMT on GaAs, the measured Hall mobility of 2-D electron gas (2-DEG) was 8200 $cm^2/V{\cdot}s$ at 300 K and 33 900 $cm^2/V{\cdot}s$ at 77 K, with a sheet carrier density of $2 \times 10^{12}/cm^2$. The identical inverted $In_{0.53}Ga_{0.47}As$ HEMT structure on Si showed a 2-DEG mobility of 6710 $cm^2/V{\cdot}s$ at 300 K and 26 800 $cm^2/V{\cdot}s$ at 77 K, with a similar sheet carrier density of $2.1 \times 10^{12}/cm^2$. The electron mobility can be further enhanced using higher InAs fraction in the channel. By inserting a 6-nm strained $In_{0.63}Ga_{0.37}As$ in the channel, the room-temperature Hall mobility of inverted HEMTs on GaAs and Si exceeds 9000 and 8000 $cm^2/V{\cdot}s$, respectively. The higher mobility on GaAs substrates was attributed to the smoother InP buffer. Fig. 3 shows typical 10×10-μm^2 AFM images of an InP/GaAs template and an InP/GaAs/Si template, and the corresponding root mean square (rms) value are 1.6 and 2.5 nm, respectively.

$In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ MOSHEMTs with regrown S/D were fabricated for high-speed and low-power logic

TABLE I
COMPARISON OF 2-DEG DENSITY (N_s), HALL MOBILITY (μ), AND SHEET RESISTANCE (R_{sh}) OF INVERTED HEMTS WITH DIFFERENT CHANNEL DESIGN

Substrate	Channel	300K			77K		
		N_s (10^{12}/cm^2)	μ (cm^2/V·s)	R_{sh} (Ω/□)	N_s (10^{12}/cm^2)	μ (cm^2/V·s)	R_{sh} (Ω/□)
Si	10nm $In_{0.53}Ga_{0.47}As$	2.09	6710	445	1.86	26,800	125
Si	2nm $In_{0.53}Ga_{0.47}As$/6nm $In_{0.63}Ga_{0.37}As$ / 2nm $In_{0.53}Ga_{0.47}As$	2.14	8200	356	1.99	27,500	114
GaAs	10nm $In_{0.53}Ga_{0.47}As$	2.00	8200	381	1.77	33,900	104
GaAs	2nm $In_{0.53}Ga_{0.47}As$/6nm $In_{0.63}Ga_{0.37}As$ / 2nm $In_{0.53}Ga_{0.47}As$	1.88	9100	365	1.86	36,000	93

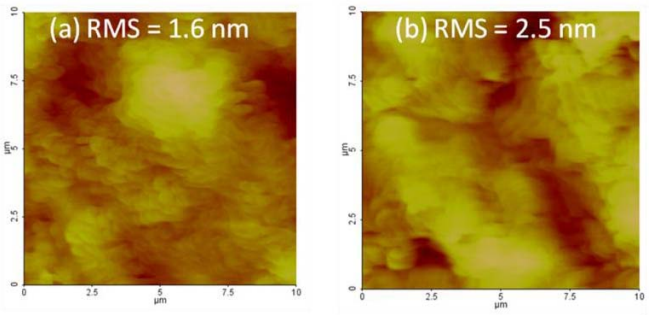

Fig. 3. 10×10-μm^2 AFM images of InP buffer on (a) GaAs and (b) Si.

applications. The process started with the deposition of 1000-Å SiO_2 as regrowth mask. S/D regions were opened by selectively removing the SiO_2 with buffered oxide etch. The exposed S/D areas were further etched down to the InGaAs channel using a phosphoric-based solution. Fig. 4(a) and (b) shows 10×10-μm^2 AFM images of the as-grown inverted HEMT on GaAs substrate and S/D region after recess etching, respectively. The recess depth was calibrated to be ~12 nm, as shown in Fig. 4(c). Considering the 8-nm InAlAs upper barrier and ~2-nm native oxide (determined by TEM), ~2 nm of the InGaAs channel layer was etched away. This confirmed that the top InAlAs was completely removed and InGaAs was exposed at the S/D regions. Using SiO_2 as mask, 60-nm n^+ $In_{0.53}Ga_{0.47}As$ S/D was selectively regrown by MOCVD. The surface morphology of the regrown $In_{0.53}Ga_{0.47}As$ is illustrated by the AFM image in Fig. 4(d). A smooth surface with slightly larger rms value than the as-grown sample was realized. Mesa isolation was then formed and the SiO_2 regrowth mask was removed. After surface cleaning using HCl:H_2O (1:10) for 2 min and $(NH_4)_2S$ passivation for 20 min, the sample was immediately loaded into an Oxford OpAL atomic layer deposition (ALD) system. Trimethylaluminum (TMA) pretreatment was performed in the ALD chamber using 20 cycles of TMA/Ar. Then, Al_2O_3 was deposited at 300 °C using TMA and water as precursors, followed by *in situ* post-deposition annealing (PDA) at 380 °C for 30 min in an H_2 atmosphere. S/D contact holes were opened and nonalloyed ohmic contacts were formed using e-beam evaporated Ni/Ge/Au/Ge/Ni/Au and liftoff. After gate metal (300-Å Ti/200-Å Pt/2500-Å Au) deposition and lift-off, PMA was conducted at 300 °C and 170

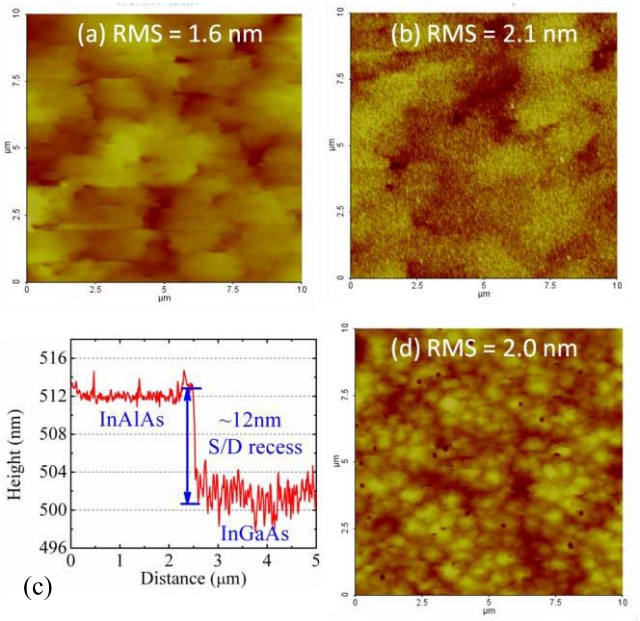

Fig. 4. (a) 10×10-μm^2 AFM image of as-grown inverted HEMT on GaAs. (b) 10×10-μm^2 AFM image of S/D recess. (c) S/D recess depth profile after removing SiO_2. (d) 10×10-μm^2 AFM image of S/D region after regrowth.

mTorr in a N_2 ambient. Fig. 5(a) shows the high-resolution TEM image of the $In_{0.53}Ga_{0.47}As$ quantum channel with the composite Ti/Al_2O_3/ $In_{0.52}Al_{0.48}As$ gate-stack on GaAs substrates. The actual thickness of $In_{0.52}Al_{0.48}As$ upper barrier and $In_{0.53}Ga_{0.47}As$ channel under the gate dielectric was 8 and 11 nm, respectively. A cross-sectional schematic of a device after fabrication is shown in Fig. 5(b).

III. DEVICE RESULTS AND DISCUSSION

The transfer characteristics of a 120-nm L_{ch} MOSHEMT with 5-nm Al_2O_3 gate oxide on GaAs was shown in Fig. 6. Threshold voltage (V_T) was extracted by linear extrapolation of the I_{ds}–V_{gs} curves. After 5-min PMA, V_T was increased from −1.6 to −0.5 V, with $g_{m,max}$ increasing from 1126 to 1684 mS/mm at $V_{ds} = 0.5$ V. An additional 8-min PMA further increased V_T to +0.1 V and $g_{m,max}$ to 1881 mS/mm.

To investigate the effects of PMA on threshold voltage change, the Au/Pt/Ti/Al_2O_3 gate-stack was examined by

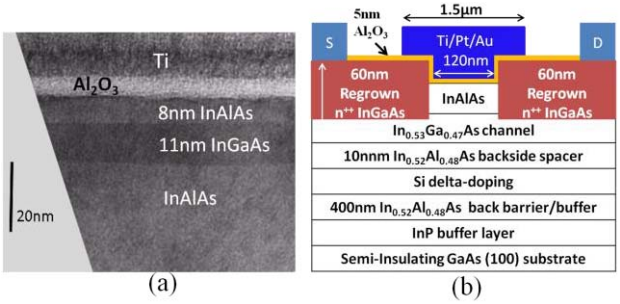

Fig. 5. (a) High-resolution TEM image of quantum well channel with composite gate-stack. (b) Schematic of inverted MOSHEMT on GaAs (note: figure is not drawn to scale).

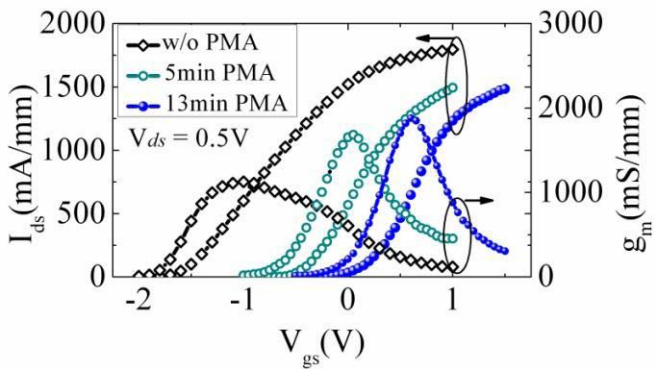

Fig. 6. Transfer characteristics of a 120-nm L_{ch} MOSHEMT on GaAs before and after PMA.

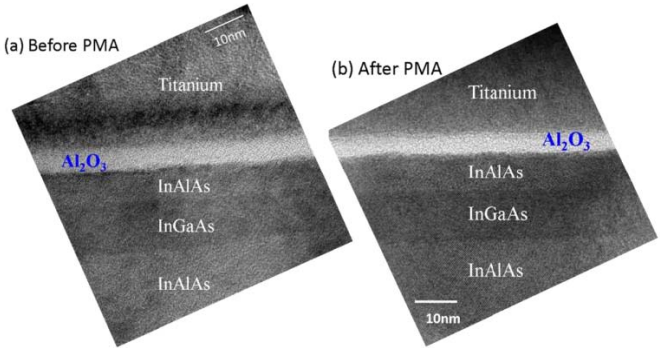

Fig. 7. TEM images of Ti/Al_2O_3 gate-stack (a) before and (b) after PMA.

TEM. After (5 + 8)-min PMA, the gate oxide shrank 20% from 5 to ~4 nm. A darkened region inside the Ti gate metal clearly observed by the contrast in the cross-sectional TEM image [Fig. 7(a)] disappeared after PMA [Fig. 7(b)]. The exact reason behind this observation is still unclear. On the other hand, the reduction of gate oxide thickness by PMA can only account for ~0.5-nm reduced equivalent oxide thickness, which cannot fully explain the ~1.7 V shift in the threshold voltage. Recently, one research group suggested that PMA treatment can efficiently reduce the interface positive net charges originated from defects at atomic layer deposited dielectric/III-nitrides interfaces [19]. But this charge reduction might have already happened at the Al_2O_3/InAlAs interface in PDA carried out at 380 °C for 30 min after gate dielectric deposition and before gate metallization. More likely, the PMA process resulted in flatband voltage shift by changing

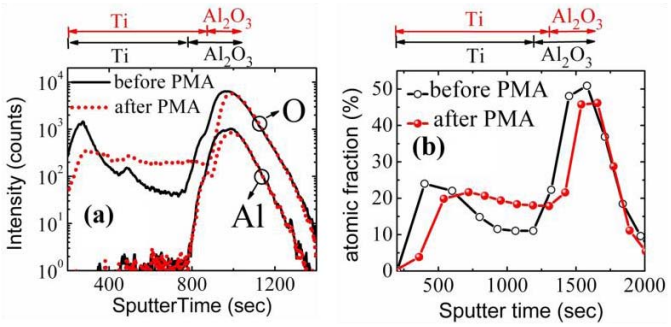

Fig. 8. (a) Oxygen and aluminum profiles in Ti and Al_2O_3 before and after PMA measured from SIMS. (b) Oxygen atomic fraction in Ti and Al_2O_3 before and after PMA measured from XPS.

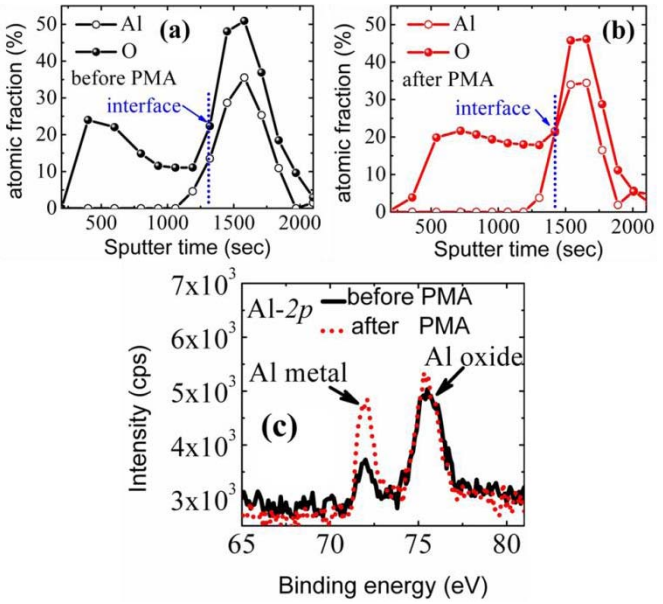

Fig. 9. (a) and (b) Atomic fraction of oxygen and aluminum measured from XPS before and after PMA. (c) Al-2*p* XPS spectrum at Ti/Al_2O_3 interface indicated by the dotted line in (a) and (b).

the Ti/Al_2O_3 interface. To examine the interface, a GaAs sample capped with 5-nm Al_2O_3/30-nm Ti/10-nm Pt/10-nm Au using the same condition as the MOSHEMTs was probed by SIMS and XPS before and after PMA treatment. A considerable amount of oxygen in the Ti has been detected by both SIMS [Fig. 8(a)] and XPS [Fig. 8(b)]. The oxygen profile measured from both methods agrees well with each other, showing flattened oxygen concentration in Ti after PMA. It is also noted that oxygen fraction doubled from ~10% to ~20% in the vicinity of the Ti/Al_2O_3 interface [Fig. 8(b)]. Similar observation of oxygen gettering by Ti overlayer has been reported in Ti/HfO_2 stacks [20]. In the meantime, shift of Ti/Al_2O_3 interface was also confirmed in Fig. 8, indicating gate sinking at the interface. This is consistent with the reduced Al_2O_3 thickness in the TEM observations. Fig. 9(a) and (b) shows the atomic fraction of aluminum and oxygen measured from XPS before and after PMA, respectively. In the XPS spectra (not shown here) inside Al_2O_3, the Al-2*p* peak was found only at 75.5 eV, which is characteristic for oxidized aluminum. Fig. 9(c) shows Al-2*p*

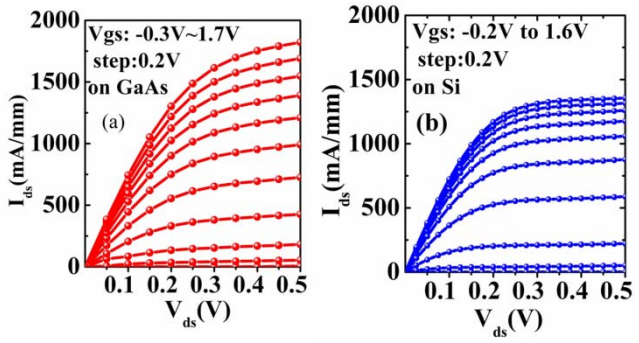

Fig. 10. Output characteristics of (a) 120-nm L_{ch} MOSHEMT on GaAs and (b) 60-nm L_{ch} MOSHEMT on Si substrate after PMA.

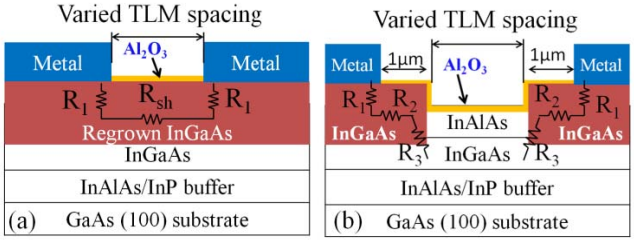

Fig. 11. TLM patterns for access resistance components extraction.

XPS spectrum in the vicinity of Ti/Al_2O_3 interface [indicated by the dotted line in Fig. 9(a) and (b)]. Both metallic aluminum and oxidized aluminum peaks were detected, which indicates a transient region. It is evident that the intensity of metallic aluminum peak was substantially enhanced after PMA. These observations suggested intermixing occurred at the Ti/Al_2O_3 interface during PMA, coupled with oxygen redistribution and Al-Ti interfacial bonding formation [21], which can alter the effective work function and net charge density.

Fig. 10(a) shows the output characteristics of a 120-nm L_{ch} MOSHEMT on GaAs after PMA. A maximum drain current (I_{dss}) of 1821 mA/mm was obtained at $V_{ds} = 0.5$ V and $V_{gs} = 1.7$ V, with a R_{ON} of 132 $\Omega \cdot \mu$m. To facilitate comparison, the output characteristics of a 60-nm L_{ch} MOSHEMT on Si [13] is shown in Fig. 10(b). I_{dss} of 1356 mA/mm was obtained at $V_{ds} = 0.5$ V, with R_{ON} of 129 $\Omega \cdot \mu$m. The R_{ON} in this paper is the lowest ever achieved in any III–V FET technology and outperforms state-of-the-art strained Si MOSFETs [22]. The excellent R_{ON} obtained for both includes contributions from the contact resistance (R_1) between the metal and the regrown S/D, series resistance (R_2) of the regrown S/D, and interface resistance (R_3) between the regrown layer and the InGaAs channel. These access resistances can be extracted using transmission-line matrix (TLM) measurement individually, as shown in Fig. 11. The obtained R_1, R_2, R_3, as well as sheet resistance R_{sh} of regrown InGaAs, and S/D parasitic resistance (R_s) were summarized in Table II. It should be noted that these access resistance components were measured from TLM patterns before PMA. A low contact resistance $R_1 = 8$ $\Omega \cdot \mu$m was achieved by non-alloyed metal/InGaAs ohmic contact due to the low resistivity (electron density $\sim 4.5 \times 10^{19}/\text{cm}^3$) in the regrown InGaAs. The series resistance R_2 contributed by regrown InGaAs was ~ 26 $\Omega \cdot \mu$m on GaAs and ~ 22 $\Omega \cdot \mu$m on Si. Experimental thermal study by TLM showed no obvious change of R_1 and R_2 after the 300 °C PMA. In terms of R_3, depending on the electron density at the regrowth interface [23], it would be influenced by the gate bias and 2-DEG density in the channel. Here, the listed R_3 were measured from TLM before PMA when the 2-DEG channel was fully turned on, similar to the condition when the device was biased at high gate voltage after PMA. It is worth noting that ITRS targets R_s of 110 $\Omega \cdot \mu$m for fully depleted high-performance logic devices at 12-nm technology node [24]. Previously, R_s as low as 93 $\Omega \cdot \mu$m has been reported in recessed-gate InGaAs MOSFETs with n^+ $In_{0.53}Ga_{0.47}As/n^+$ InP S/D contact [25]. Our results indicate that the ITRS objective can be alternatively achieved using regrown n^+ $In_{0.53}Ga_{0.47}As$ S/D technique developed in this paper, with further minimized R_2 through self-aligned metal contacts and/or thicker regrown S/D.

TABLE II
ACCESS RESISTANCE COMPONENTS EXTRACTED FROM TLM

Substrate	R_1 (Ω·μm)	R_{sh} (Ω/□)	R_2 (Ω·μm)	R_3 (Ω·μm)	$R_s = 2 \times (R_1+R_2+R_3)$ (Ω·μm)
GaAs	8	26	26	31	130
Si	8	22	22	32	124

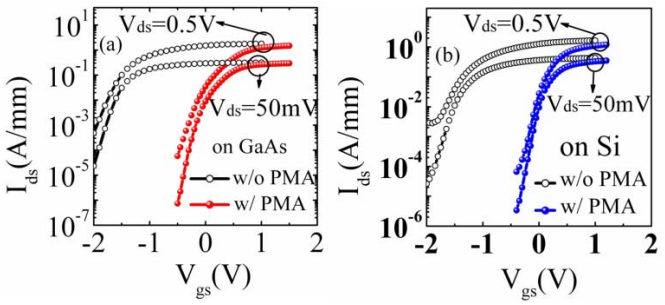

Fig. 12. Semilog plots of I_{ds}–V_{gs} curves of (a) 120-nm L_{ch} MOSHEMT on GaAs and (b) 60-nm L_{ch} MOSHEMT on Si substrate after PMA.

For transistors working as a switch in logic applications, sharp transition between ON- and OFF-states is essential. Fig. 12(a) shows semilog plots of I_{ds}–V_{gs} curves of a 120-nm L_{ch} MOSHEMT on GaAs. After PMA, SS at $V_{ds} =$ 50 mV was reduced from 135 to 93 mV/decade, whereas the SS at $V_{ds} = 0.5$ V decreased from 182 to 153 mV/decade. Similar effects have been observed for devices on Si substrates, as shown in Fig. 12(b). After PMA, SS at $V_{ds} = 50$ mV was reduced from 164 to 101 mV/decade, and the SS at $V_{ds} = 0.5$ V decreased from 262 to 120 mV/decade.

Finally, the devices in this paper were benchmarked with state-of-the-art $In_xGa_{1-x}As$ ($x \geq 53\%$) channel MOSFETs at ~100-nm gate length regime using the figure of merit $Q = g_m/\text{SS}$ [16], where SS is measured at saturation region. As shown in Fig. 13, the 120-nm $In_{0.53}Ga_{0.47}As$ channel MOSHEMTs grown on lattice-mismatched GaAs by MOCVD exhibited a Q up to 12, and the 60-nm $In_{0.53}Ga_{0.47}As$ channel MOSHEMTs grown on Si showed a Q of 14. These results are significantly better than InGaAs surface-channel MOSFETs on InP substrates reported a few years ago [5], [7], [8], and approaching the best performance achieved by $In_{0.7}Ga_{0.3}As$

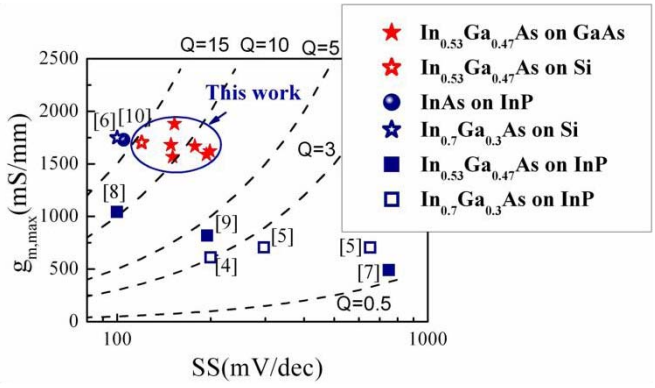

Fig. 13. Benchmarking of InGaAs MOSFETs using the figure of merit $Q = g_m/SS$ (all the data in literature except [9] were from devices grown by MBE).

buried-channel MOSFETs on off-cut Si [6] or InAs quantum well-channel MOSFETs on InP [10] grown by MBE.

IV. Conclusion

In this paper, we presented the material and device characteristics of inverted-type $In_{0.53}Ga_{0.47}As$ MOSHEMTs metamorphically grown on GaAs and Si substrates by MOCVD. Significantly improved ON- and OFF-state device characteristics were obtained after a low-temperature PMA process. The outstanding logic figures of merit exhibited by $In_{0.53}Ga_{0.47}As$ MOSHEMTs in this paper can be primarily attributed to the significantly reduced access resistance using selective S/D regrowth by MOCVD. In addition, PMA further enhanced the gate electrostatic control over the buried quantum well channel. Enhancement-mode operation was attained without reducing the InAlAs upper barrier too much. As a result, the 2-DEG in the InGaAs channel was kept relatively far away from the oxide/III–V interface and high channel mobility can be maintained. This paper suggests that heteroepitaxy of InP on GaAs or Si by MOCVD is a practical, cost-effective process for fabricating high-performance InP lattice-matched, or strained-channel transistors. Comparable device performance can be obtained on GaAs and Si substrates using heteroepitaxy, in spite of different lattice mismatch. The device characteristics at low supply voltage also indicate that the inverted-type InAlAs/InGaAs MOSHEMT design is promising for "post-Si" high-speed logic applications.

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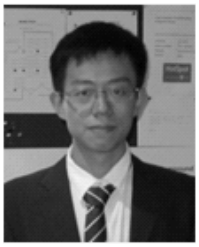

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