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DC and RF Performance of Gate-Last AlN/GaN MOSHEMTs on Si With Regrown Source/Drain

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***Abstract*— This paper presents the fabrication and characteristics of self-aligned gate-last AlN/GaN metal–oxide–semiconductor high electron mobility transistors (MOSHEMTs) featuring regrown source/drain for low ON-state resistance (R_{ON}). Previously, we demonstrated conventional enhancement-mode AlN/GaN MOSHEMTs on Si substrate with excellent DC performance but limited RF characteristics by large parasitic gate-to-source/drain overlap capacitance. In this paper, the self-aligned gate-last process was developed to minimize the parasitic capacitance. SiN_x sidewall and supporting layer were inserted to separate the gate head and source/drain. In the gate-last devices, f_T has been improved to be ~40 GHz with a channel length (L_g) of 210 nm. Delay time analysis showed that drain delay was relatively small compared with gate transit and parasitic charging time because of the self-aligned structure.**

***Index Terms*— AlN/GaN, atomic-layer-deposited (ALD) Al_2O_3, enhancement-mode (E-mode), gate-last, metal–oxide–semiconductor high electron mobility transistor (MOSHEMT), self-aligned.**

I. Introduction

COMBINED high frequency and high breakdown characteristics offer GaN high-electron mobility transistors (HEMTs) practical advantages in applications of RF/millimeter-wave power amplifier and power switching. After demonstration of the first AlGaN barrier HEMT two decades ago [1], several emerging barrier designs, including AlN [2]–[5], lattice matched InAlN [6]–[8], and quaternary InAlGaN [9], [10], have been implemented to improve the transistor performance and reliability, leading to state-of-the-art results in terms of f_T/f_{max} and output power density [9], [11]. Scaled gate lengths down to <100 nm have been employed for accelerated device speed (v_e/L_g), whereas the barrier thickness (t_d) must be maintained to provide high enough aspect ratio (L_g/t_d) for mitigation of short channel effects. AlN barriers, having the highest spontaneous polarization among all the III-nitride materials, can lead to maximized 2-D electron gas (2DEG) density even at thicknesses <10 nm [12]. Ultrathin AlN barriers allow good gate control capability over channel carriers, which results in high frequency performance up to W-band (75–110 GHz). Both Ga- and N-polar AlN barrier HEMTs grown on SiC substrate by molecular beam epitaxy have been demonstrated. Ga-polar based AlN HEMTs achieved a record f_T/f_{max} of 342/518 GHz with $L_g = 20$ nm by advanced T-gate fabrication technology [13]. The N-polar AlN HEMTs fabricated with self-aligned and selectively etching process also achieved a f_T/f_{max} of 115/35 GHz for $L_g = 120$ nm [14]. The f_{max} was limited by the thin gate metal with high resistivity.

Although metal organic chemical vapor deposition (MOCVD) is widely used for growth of III-nitride, it is difficult to grow high quality thin AlN layers with excellent AlN/GaN interfaces required by devices. There are limited reports concerning AlN/GaN HEMTs grown on Si (111) substrates by MOCVD. Until recently, AlN/GaN HEMTs grown by MOCVD on Si substrates have been reported with *in situ* SiN_x cap layer for strain relaxation [12], [15], [16]. The SiN_x in the gate region must be selectively etched before gate metal deposition.

In this paper, a GaN cap was used as a protective layer for the AlN barrier underneath. All the AlN/GaN heterostructure was grown by MOCVD on high resistive Si substrate. The corresponding heterostructure is similar to that described in [17]. Section II compares two AlN/GaN metal-oxide-semiconductor high electron mobility transistors (MOSHEMTs) architectures fabricated with former process [17] and this gate-last process. In Section III, the thermal stability of different ohmic metals is discussed. Cr/Au instead of previously reported Ti-based metal system [18] has been used because of better thermal stability. Section IV describes the self-aligned gate-last process developed to minimize the parasitic capacitance. Then, DC and RF performances of the fabricated devices by former and gate-last process are discussed in Section V. Increased value of $f_T \cdot L_g$ confirmed the improved RF performance by the self-aligned process. The delay time analysis was conducted in Section VI. This is the first time that self-aligned gate-last process is implemented in GaN MOSHEMT. The gate-first process has been previously used in [14].

II. Design of Gate-Last Devices

In [17], enhancement-mode (E-mode) AlN/GaN MOSHEMTs were fabricated with 6-nm Al_2O_3. A record transconductance (G_m) of 509 mS/mm and drain current (I_d) of 860 mA/mm was demonstrated for E-mode devices on Si. Despite of excellent DC performance, the fabricated

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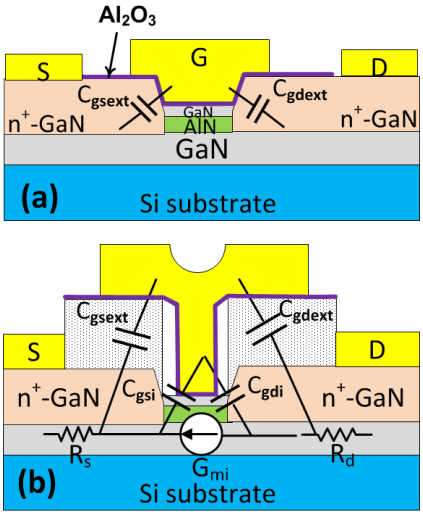

Fig. 1. (a) Cross-sectional schematic view of AlN/GaN MOSHEMTs fabricated with former process. (b) Schematic view of gate-last device. C_{gsext} and C_{gdext} are gate head-induced parasitic capacitance. C_{gsi} and C_{gdi} are gate intrinsic capacitance, which are a function of gate length. G_{mi} is the intrinsic transconductance. R_s and R_d are source and drain access resistance, respectively.

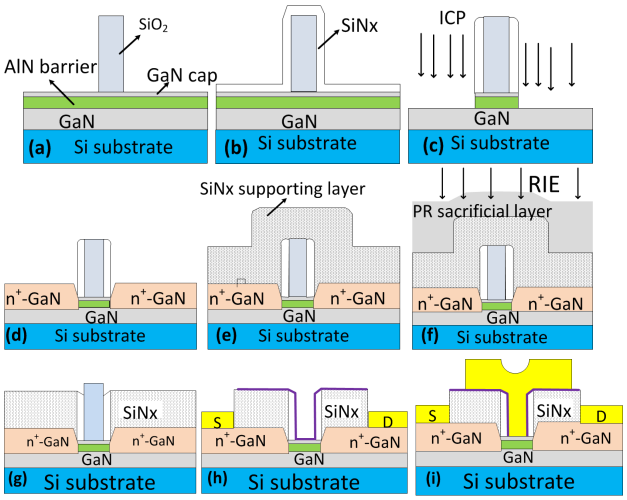

Fig. 2. Schematic diagrams of the overall process flow. (a) SiO_2 dummy gate deposition and patterning. (b) SiN_x blanket deposition. (c) Sidewall formation by ICP etching. (d) Selective regrowth of highly doped GaN for source/drain. (e) SiN_x supporting layer deposition. (f) Planarization by photoresist sacrificial layer. (g) Photoresist removal after planarization. (h) Dummy gate removal and high-k Al_2O_3 deposition. (i) Source/drain and gate metal formation.

devices suffer from serious parasitic capacitance because of the overlap between the gate and the source/drain access regions. The huge extrinsic capacitances of both C_{gsext} and C_{gdext} [Fig. 1(a)] in this device architecture degrade the RF performance significantly, resulting from large charging/discharging loss. A self-aligned gate-last process was developed for III-nitride, which is similar to the Si CMOS gate-last technology. The corresponding device architecture is shown in Fig. 1(b). To reduce the C_{gsext} and C_{gdext}, SiN_x supporting layer and sidewall were inserted to separate the gate head from the n^+-GaN source/drain.

III. Self-Aligned Gate-Last Process and Ohmic Contact Optimization

The self-aligned gate-last process was realized by means of a dummy gate, which was eventually removed after planarization and replaced with a metal gate. The detailed process flow is shown in Fig. 2. Firstly, 350-nm-thick SiO_2 dummy gate was deposited by plasma-enhanced chemical vapor deposition. The initial 1-μm SiO_2 length was defined by photolithography and patterned by a dry etching process in reactive ion etch (RIE) system. Subsequently, the SiO_2 length was further shrunk by wet etching in a buffered oxide etchant (BOE) solution from 1 μm to <500 nm. A 50-nm SiN_x was then blanket deposited at 300 °C, followed by anisotropic dry etching with Cl_2 based plasma in an inductively coupled plasma (ICP) system. This leaves SiN_x only on the vertical surfaces. It should be noted that the GaN in the source/drain region [Fig. 2(c)] was further recessed by 70 nm for n^+-GaN regrowth. The total regrown n^+-GaN thickness was $\sim$100 nm. The n^+-GaN consists of two-level doped layers (Si: $2.5\times10^{19}/\mathrm{cm}^3$ and a highly doped layer up to $6\times10^{19}/\mathrm{cm}^3$). The lighter doped GaN was used to provide a better transition to the highly doped layer with good surface morphology. The sheet resistance of n^+-GaN is 298 Ω/sq. Then, a 300-nm SiN_x was deposited as the supporting layer. To expose the SiO_2 dummy gate, planarization was conducted. In Si CMOS technology, the common planarization tool is chemical-mechanical planarization (CMP). To replace CMP, we used AZ5200 photoresist as the sacrificial mask to realize planarization by RIE [Fig. 2(f)], which has also been used by another group [18]. The etching gas in the RIE system was a CHF_3/O_2 mixture, and the ratio of the two gas flow was adjusted to equalize the etching rate of photoresist with that of SiN_x during etch back. Over etching was always required to guarantee exposure of the SiO_2 for the following removal by BOE solution. High etching selectivity of SiO_2 to SiN_x in BOE solution is important to assure the SiN_x not to be removed. Rapid thermal annealing (850 °C for 1 min) was performed to increase the sustainability of SiN_x to BOE. Before annealing, the SiN_x was patterned by RIE leaving areas in the gate region only. This patterning process can also release the huge thermal stress between SiN_x and GaN during annealing. Low plasma etching power was used to avoid any plasma damage to the n^+-GaN ohmic contact. After planarization and removal of the dummy gate by BOE solution, atomic-layer-deposited (ALD) Al_2O_3 (6 nm) was deposited as the gate dielectric. Pre-ALD treatment was with diluted HCl solution for 5 min. The amorphous Al_2O_3 was deposited at 300 °C using trimethylaluminum and H_2O as precursors after 10 cycles of H_2O pretreatment. Then, source/drain (Cr(30 nm)/Au(100 nm)) and gate metals (Ni(50 nm)/Au(350 nm)) were deposited. A postgate annealing was performed at 400 °C to achieve E-mode operation. It is noted that the Cr ohmic contact is stable up to 400 °C.

In our previously reported research, Ti-based alloy was chosen as the ohmic contact metal for the n^+-GaN. The thermal stability of the Ti/n^+-GaN interface is, however, poor at 300 °C. I–V characteristics [Fig. 3(a)] confirm that the current curves display a Schottky behavior after annealing at 300 °C.

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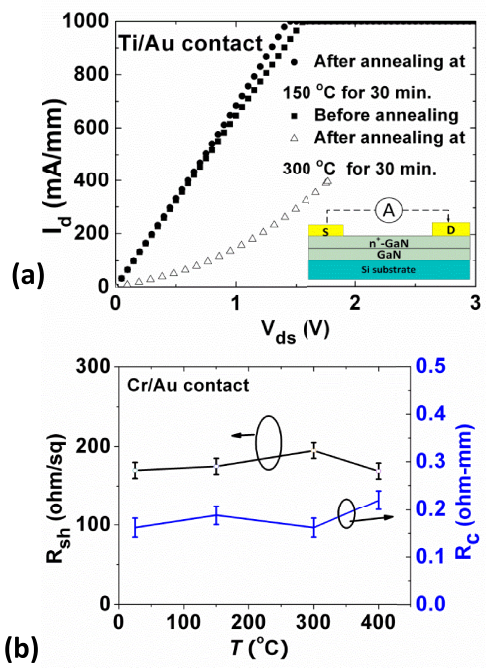

Fig. 3. (a) Drain current measured on the TLM pattern (inset) with source–drain spacing of 3 μm. (b) Dependence of sheet and contact resistances on temperature for Cr/n$^+$-GaN.

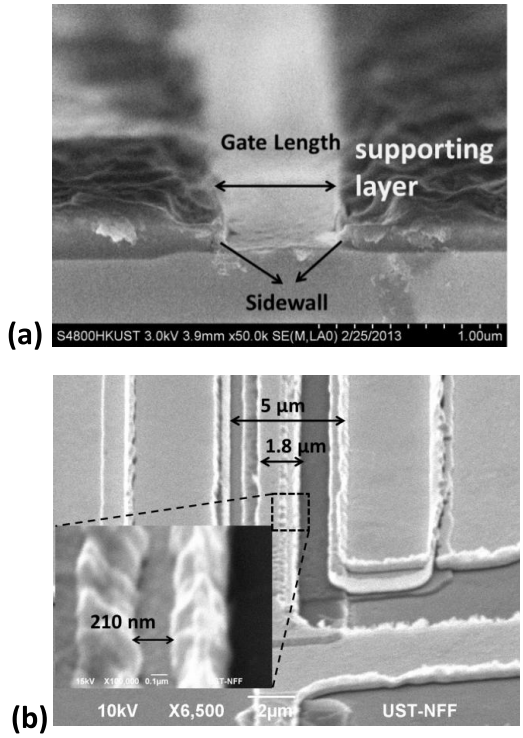

Fig. 4. (a) SEM image of the device on a control sample for monitoring the whole process. The SiN_x sidewall width is ~50 nm. (b) SEM image of the fabricated device with a tilt angle of 60°. The L_g = 210 nm from inset image with zoomed-in-view gate region, source–drain spacing L_{sd} = 5 μm, and gate head length = 1.8 μm.

This rectifying behavior is an irreversible process because of the formation of TiN in the Ti/n$^+$GaN interlayers [19]. Alternatively, Cr/n$^+$-GaN provides better thermal stability. The contact resistance (R_c) of Cr/n$^+$-GaN keeps nearly constant at ~0.2 $\Omega \cdot$mm at a temperature up to 400 °C [Fig. 3(b)]. There is no obvious R_c difference between Cr/n$^+$-GaN and Ti/n$^+$-GaN under the same n$^+$-GaN sheet resistance at room temperature. Fig. 3(b) shows that the sheet resistance (R_{sh}) is independent of the temperature within measurement uncertainties as the electron concentration in the n$^+$-GaN remains unchanged > 200 K and the carrier mobility is dominated by doping impurity scattering. Cr-based alloy for ohmic contacts is necessary if device operation is > 300 °C. We replaced Ti with Cr alloy as ohmic contact metal for III-nitride transistors after this research.

Using the described process, we fabricated devices with gate length between 200 and 500 nm. A cross-sectional scanning electron microscope (SEM) image on the control sample before gate metal deposition is shown in Fig. 4(a). The supporting SiN_x around the channel is thinner than that far away from the channel, which was caused by the slightly higher etching rate of SiN_x than that of AZ5200 photoresist. This thickness step could be eliminated by adjusting the CHF_3/O_2 flow ratio. The surface of the SiN_x supporting layer is rough and over etched. The SEM image of the fabricated sample with L_g = 210 nm is shown in Fig. 4(b).

IV. Characteristics of Devices by Former and Gate-Last Process

A. DC Characteristics

Fig. 5(a) compares the transfer curve results for different gate-length E-mode MOSHEMTs fabricated by former and gate-last process. The 5.5-nm ALD Al_2O_3 layer was deposited as gate dielectric in former process, whereas the Al_2O_3 thickness is 6 nm in gate-last process. It should be stressed that a post-gate annealing at 400 °C for 10 min was performed in nitrogen ambient. The post-gate annealing

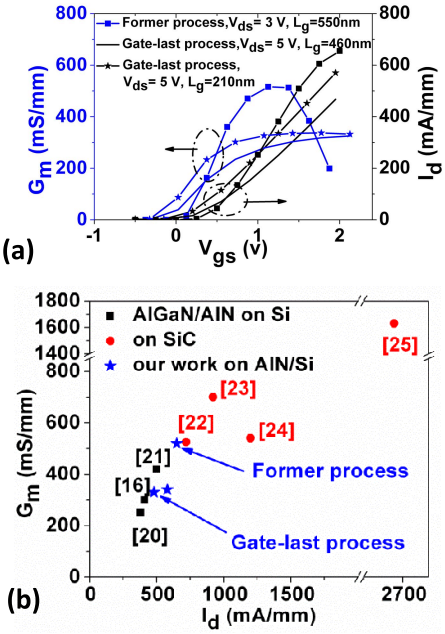

Fig. 5. (a) Transfer curve of E-mode AlN/GaN MOSHEMTs by former and self-aligned process with different gate length. (b) Comparison of G_m and I_d with results from literatures.

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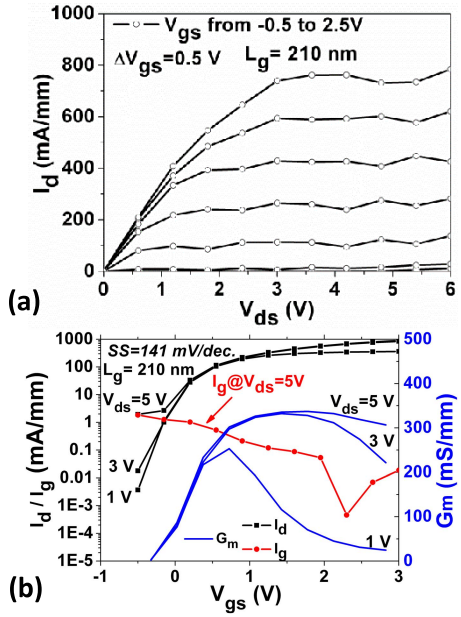

Fig. 6. DC results of 210-nm E-mode AlN/GaN MOSHEMTs by gate-last process. (a) Output and (b) transfer characteristics of MOSHEMTs with gate leakage current measured at $V_{ds} = 5$ V.

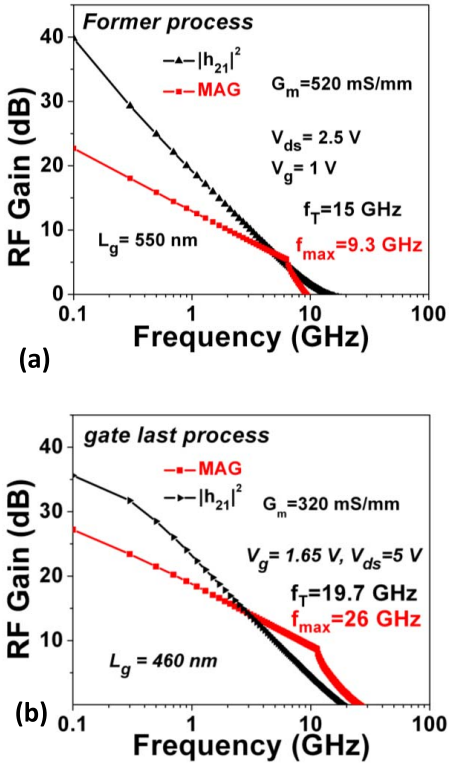

Fig. 7. RF characteristics of AlN/GaN MOSHEMTs fabricated by (a) former process and (b) gate-last process. The channel width is 2×50 μm.

could push the threshold voltage toward positive direction. Detailed analysis of the mechanism would be conducted in future publication. The excellent DC performance of E-mode AlN/GaN MOSHEMTs has been demonstrated by former process with G_m of 520 mS/mm [17] [schematic view as shown in Fig. 1(a)], which exhibited much higher G_m in comparison with devices by gate-last process. Fig. 5(b) shows a comparison of reported G_m as a function of I_d for E-mode GaN HEMTs on sapphire, Si, and SiC substrates [16], [20]–[25]. Although the gate length of our device is much longer than the others, the E-mode transistor by former process exhibited the highest G_m and I_d among all HEMTs on Si substrates. The lower G_m in gate-last devices is mainly caused by large source resistance because of high sheet resistance of n^+-GaN in access region.

Fig. 6 shows typical common-source I–V characteristics of a 210-nm channel length AlN/GaN MOSHEMTs by gate-last process. The threshold voltage (V_{th}), obtained by linear extrapolation of the transfer curves was +0.2 V. At $V_{gs} = 2.5$ V, a maximum I_d of 780 mA/mm was reached, and the R_{ON} at $V_{gs} = 2.5$ V is 2.8 $\Omega \cdot$mm. For devices with $\sim$5-μm long source–drain spacing, the large R_{ON} of self-aligned device is mainly contributed by the huge sheet resistance of n^+-GaN (298 Ω/sq, 100-nm thick), whereas the n^+-GaN sheet resistance in the former device is only $\sim$132 Ω/sq (200-nm thick) [17]. Therefore, the R_{ON} can be further reduced by decreasing the sheet resistance of n^+-GaN via higher doping concentration and thicker regrown layer. It should be stressed that there would be no carrier depletion in the access region under the SiN_x sidewall. Similar to Al_2O_3, SiN_x can also increase the 2-DEG density underneath the channel [26]. Therefore, sidewall would not introduce large parasitic access resistance. At $V_{ds} = 5$ V, a maximum extrinsic DC G_m of 340 mS/mm was obtained. With the increase of drain voltage from 1 to 5 V, the OFF-state current mainly consist of gate–drain leakage current. There is no observed drain-induced barrier lowering. The subthreshold slope is estimated to be 141 mV/decade at $V_{ds} = 1$ V [Fig. 6(b)].

B. Small Signal RF Characteristics Comparison

S-parameter measurements were carried out in the frequency range 100 M–39.1 GHz using an Agilent 8722ES network analyzer with HP4142B monitoring the DC bias conditions. The system was calibrated with an off-wafer short-open-load-thru calibration standard. On-wafer open pads were used to deembed parasitic pad capacitances from the S-parameters. Fig. 7 compares the RF characteristics of MOSHEMTs fabricated with our former process [T_1, schematic view shown in Fig. 1(a)] and gate-last process [T_2, schematic view shown in Fig. 1(b)]. Similar channel lengths obtained in T_1 and T_2 (550 and 460 nm) were chosen for comparison. The resulting $f_T \cdot L_g$ for T_2 ($\sim$20 GHz) is $\sim$9.1 GHz $\cdot \mu$m, which is almost 11% higher than that of T_1. The $f_T \cdot L_g$ is related to the parasitic delay, channel velocity, and gate control in the device. In this paper, T_1 and T_2 were fabricated using the same heterostructure and approximated gate length. Therefore, the enhanced $f_T \cdot L_g$ is caused by the reduction of the parasitic capacitance. This also could be confirmed by the increased f_T even when G_m is lower than that of former device. The large overlap region in T_1 introducing a gate–drain capacitance (C_{gd} is $\sim$400 fF) almost equal to the gate-source capacitance (C_{gs} is $\sim$400 fF). Large C_{gd} translates into low impedance, rendering the f_{max} (9.3 GHz) even smaller than the f_T (15 GHz).

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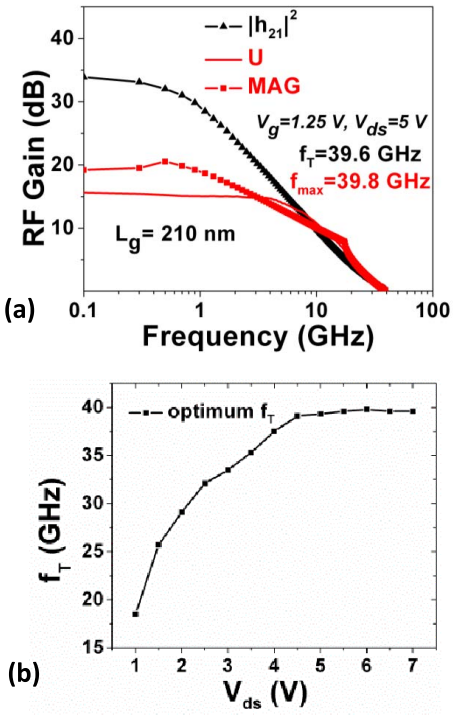

Fig. 8. Gate-last 210-nm gate-length E-mode AlN/GaN MOSHEMTs. (a) RF characteristics. (b) Peak f_T as a function of V_{ds} at optimized V_{gs} ~1 V.

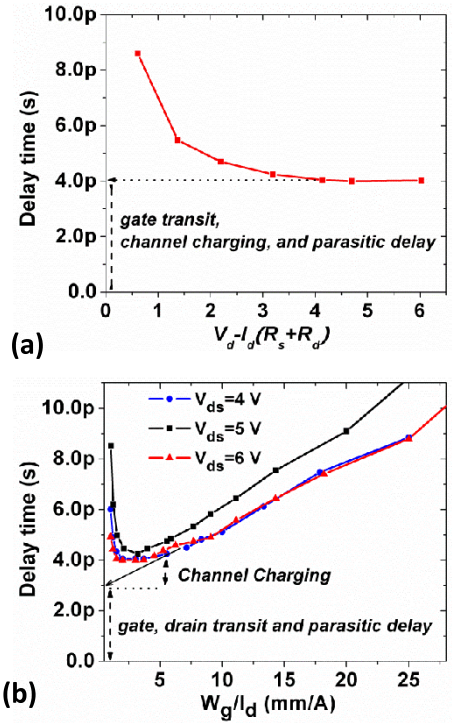

Fig. 9. (a) Delay time as a function of voltage across the channel under the gate. (b) Delay time as a function of reciprocal drain current density.

On the other hand, the C_{gd} (~72 fF) in T_2 was almost one order of magnitude lower than its C_{gs}. This result confirms the significant reduction of parasitic capacitances (C_{gsext} and C_{gdext}) because of the SiN_x supporting layer and sidewall. It should be noted that, like advanced CMOS technology, other low-k stable materials also could be employed for supporting layer.

V. Time Delay Analysis of Gate-Last Device

Fig. 8 shows the RF characteristics of the 210-nm gate length AlN/GaN MOSHEMTs at maximum f_T bias condition (V_{ds} = 5 V, V_{gs} = 1.25 V). Simultaneous high f_T/f_{max} of 39.6/39.8 GHz were obtained.

The peak f_T as a function of V_{ds} was measured at V_{gs} corresponding to maximum f_T. The f_T continuously increase with V_{ds} above the saturation voltage of 2 V until approaching the maximum value of 39.6 GHz at V_{ds} = 4.5 V and then decrease a little after V_{ds} higher than 6 V. The f_T does not show obvious decrease at large V_{ds} (> 5 V).

To further understand the effects of various delay components on device speed, delay time analysis was conducted [27]. The total delay time $\tau_{total} = 1/(2\pi \times f_T)$ is defined as

$$\tau_{total} = \tau_{gate} + \tau_{drain} + \tau_{channel} + \tau_{parasitic} \quad (1)$$

where all the parameters are shown in Fig. 1(b). The total delay in (1) consists of four terms. The first term is the intrinsic delay because of gate transit time, called gate delay (τ_{gate}). The second term is an additional delay associated with time spent by carriers in the depletion region, called drain delay (τ_{drain}). The third term is parasitic charging delay because of parasitic capacitance and channel resistance, called channel charging delay ($\tau_{channel}$). The channel resistance varies with the drain current. The fourth term-parasitic delay, related to access resistances of $R_s + R_d$, is given by C_{gd} ($R_s + R_d$). Fig. 9(a) shows the total delay as a function of corrected voltage across the channel. The extrapolated delay at zero voltage is equal to $\tau_{gate} + \tau_{channel} + \tau_{parasitic}$. The difference between τ_{total} and this delay is τ_{drain}. The drain delay is nearly constant with increasing V_{ds}, which implies that the drain depletion length outspreading is suppressed in such structure with only a 50-nm-thick sidewall. The negligible drain delay in this device is also confirmed in Fig. 8(b). This phenomenon has also been observed by AlN/GaN HEMTs with 40-nm gate–drain distance [25].

Similarly, extrapolated delay in τ_{total} versus W_g/I_d (gate width normalized to drain current) is $\tau_{gate} + \tau_{drain} + \tau_{parasitic}$ [Fig. 9(b)]. The $\tau_{gate} + \tau_{parasitic}$ is ~3 ps combining the intercept delay in both Fig. 9(a) and (b). The parasitic delay is then estimated to be 1 ps ($C_{gd}(R_s + R_d)$). This means the gate transit time is ~2 ps. Finally, the average channel velocity (v_e) is estimated to be 1×10^7 cm/s.

VI. Conclusion

Excellent DC performance was obtained in former AlN/GaN MOSHEMTs featuring regrown n^+-GaN as source/drain. To eliminate the large parasitic capacitances, a self-aligned gate-last process was developed, leading to greatly improved RF performance. $f_T \cdot L_g$ enhancement is observed in gate-last device by ~11%. The maximum f_T was ~39.6 GHz from a gate-last device with L_g = 210 nm. From the delay time analysis, it was found that the total delay is dominated by parasitic charging and gate transit delay, whereas

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the drain delay is negligible in this device architecture. The further improvement of RF performance still could be achieved by low-k dielectric for supporting layer and gate length scaling down.

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Authors' photographs and biographies not available at the time of publication.