Enhancement-mode AlN/GaN MOSHEMTs Fabricated by Selective Area Regrowth of AlGaN Barrier Layer

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***Abstract*—Enhancement-mode (E-mode) metal-oxide semi-conductor high electron mobility transistors (MOSHEMTs) have been fabricated by selective area regrowth technique on AlN/GaN heterostructure. A selectively regrown AlGaN barrier layer could effectively increase the 2-dimensional electron gas (2DEG) density underneath. In comparison with the conventional methods of plasma etching/treatment in the gate region, the regrowth technique can effectively avoid damage caused by the plasma process. Atomic layer deposition of Al_2O_3 was employed as the gate dielectric. It was found that the Al_2O_3 on the AlN barrier layer also could induce a higher density of 2DEG. The fabricated E-mode MOSHEMTs with a 1.4-μm gate length exhibited excellent performance of maximum drain current of 530 mA/mm and peak transconductance of 310 mS/mm. The threshold voltage of MOSHEMTs was around +0.2 V. The reverse leakage current was also observed to be around 3.6×10^{-4} mA/mm at V_{gs} = -1 V and V_{ds} = 6 V. The peak channel electron mobility was extracted to be 880 cm^2/Vs using split-CV method. These results indicate that the regrowth technique is a promising method to realize E-mode transistors.**

I. INTRODUCTION

E-mode transistors have attracted great interest due to its normally off characteristics, especially in high-power switching applications for safety and low power consumption. However, the spontaneous formation of a polarization-doped 2DEG in Al(Ga)N/GaN heterointerface makes the fabrication of E-mode GaN transistors challenging. The conventional approaches to realize E-mode transistors, including gate-recess by plasma etching [1], O_2 plasma treatment [2], and CF_4 plasma treatment [3] on the Al(Ga)N barrier layer, would inevitably cause damage to the channel underneath. Some other methods, such as adding a p-GaN cap layer [4] and introduction of an InGaN cap layer [5], also suffer from selective plasma etching to remove the cap layer in the access region. Moreover it is difficult to control the uniformity and reproducibility of plasma etching.

In this letter, we report fabrication of E-mode MOSHEMTs by a plasma damage-free process, where a selective area regrowth of AlGaN barrier layer was employed to avoid the plasma process. Moreover, the E-mode transistors were realized on a AlN/GaN heterostructure, which was different from conventional AlGaN/GaN transistors structure [6, 7]. Compared with the AlGaN, AlN offers a higher potential barrier and larger polarization effects, which are beneficial for vertical scaling to push towards high frequency performance. The AlN/GaN heterostructure in this work was grown by metal organic chemical vapor deposition (MOCVD) on a Si substrate. The AlN thickness was around 1.5 nm estimated by growth rate. Post-gate annealing was performed for E-mode transistors. The final E-mode transistors with 1.4-μm gate length exhibited a high drain current and extrinsic transconductance.

II. MATERIALS GROWTH AND DEVICE FABRICATION

The samples used in this work were grown on 2" Si (111) substrates by MOCVD. The corresponding epitaxial layer structure is shown in Fig. 1(a), which is similar to that in reference [5]. The epi-layers consist of a 40-nm AlN nucleation layer, an 800-nm GaN, an 8-pair AlN (6 nm)/AlGaN (25 nm) super-lattice interlayer with total thickness of 300 nm, a 1000-nm GaN, an AlN barrier layer around 1.5 nm, and finally a 1-nm GaN protective layer on top. Before the regrowth process, the abovementioned AlN/GaN heterostructure wafer was patterned with a 65-nm-thick SiO_2 layer as a regrowth mask deposited by plasma enhanced chemic vapor deposition (PECVD). The SiO_2 was processed by photolithography and diluted HF etching solution to form mask patterns on the gate region. Then the patterned sample was loaded back into MOCVD chamber for selective regrowth of an AlGaN barrier layer. The as-grown heterostructure shows an average sheet resistance about 4000 Ω/sq, and its surface is very smooth with step flow growth mode (Fig. 1(b)). Atomic force microscopy (AFM) measurements revealed a smooth surface with root-mean-square (RMS) roughness of 0.72 nm for a scanned area of 2μm×2μm.

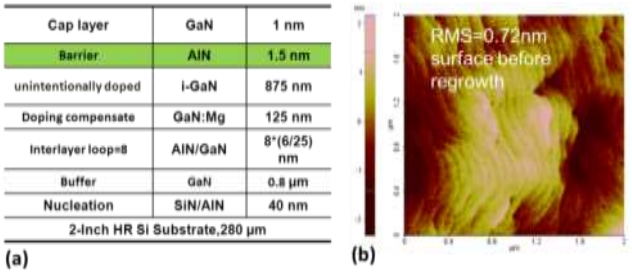

Fig. 1. (a) AlN/GaN heterostructure. (b) Surface morphology scanned by AFM.

The regrowth and fabrication procedures are shown in detail in Fig. 2. After patterning the SiO_2 mask and regrowth of the AlGaN layer, mesa isolation was performed using Cl_2/He plasma dry etching in an inductively coupled plasma reactive ion etching (ICP-RIE) system. Then, source and drain electrodes were deposited using Ti/Al/Ni/Au followed by annealing at 850°C for 30 s in a nitrogen ambient. A 7-nm Al_2O_3 deposition by atomic layer deposition (ALD) was used to block tunneling leakage current due to ultra-thin AlN barrier. Finally the gate metal (Ni/Au) was deposited. The post-gate annealing was performed at 400°C for 10 min in a nitrogen ambient. The profile of regrown AlGaN near the gate region was characterized by AFM. The regrowth profile (Fig. 3) after stripping of the SiO_2 mask showed a nearly vertical step and the AlGaN thickness was about 20 nm.

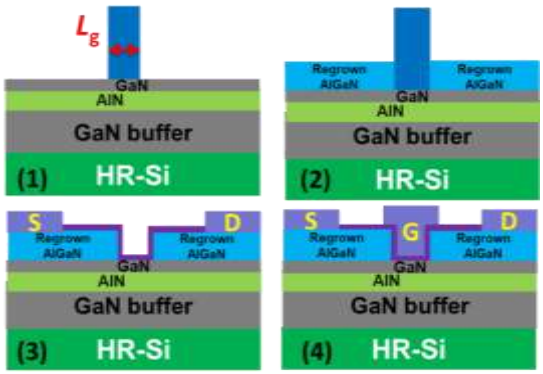

Fig. 2. Regrowth and simplified process flow of MOSHEMTs: (1) pattern with SiO_2, (2) regrowth of AlGaN barrier layer, (3) SiO_2 strip, source/drain ohmic formation and 7-nm Al_2O_3 deposition, (4) gate metal deposition.

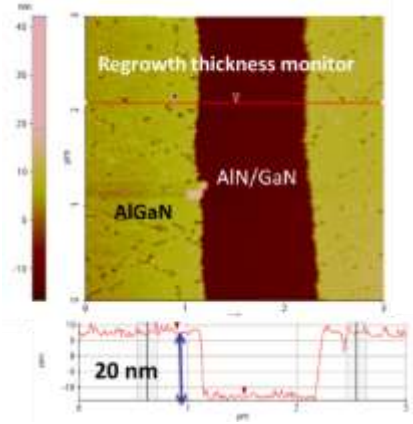

Fig. 3. AFM image of the regrowth profile in the gate region after SiO_2 is removed.

III. Results and Discussion

Prior to the regrowth of AlGaN barrier layer, the average sheet resistance (R_{sh}) of the as-grown sample was more than 4000Ω/sq from the Hall-effect measurement. The R_{sh} was reduced to 330Ω/sq after regrowth of the AlGaN barrier layer, as shown in transmission line measurement (TLM) results (Fig. 4). This R_{sh} value is almost similar to that of conventional AlGaN/GaN HEMTs. This demonstrated that the regrown AlGaN could effectively increase the 2DEG density underneath. Meanwhile, a low contact resistance of 0.39 Ω·mm was obtained.

Al_2O_3 deposited by atomic layer deposition (ALD) can effectively increase the 2DEG density, which results in enhanced drain current. Fig. 5 shows the IV curves of devices with various Al_2O_3 thicknesses prior to gate metal deposition. The drain current increased correspondingly from 39 mA/mm (0-nm Al_2O_3), 450 mA/mm (7-nm Al_2O_3), to 815 mA/mm (10-nm Al_2O_3) with the increase of Al_2O_3 thickness. This implies that the Al_2O_3 could induce a higher density of 2DEG. Previous publications had demonstrated that the SiN_x deposited by catalytic chemical vapor deposition (Cat-CVD) [8] and PECVD [9] could increase 2DEG density and reduce the sheet resistance in AlN/GaN HFETs. The increase of 2DEG density after Al_2O_3 deposition is believed to result from a decreased surface barrier height. The mechanism for this is considered to be the interface donors and incorporated stress [10].

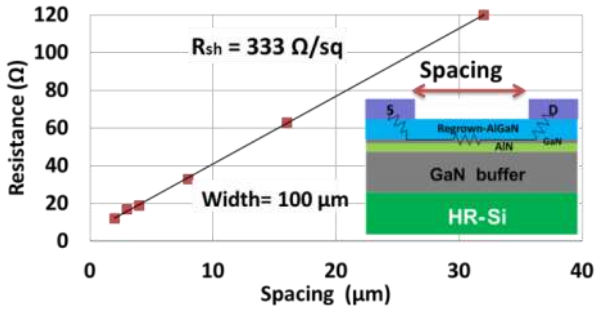

Fig. 4. TLM of the sample with regrown AlGaN cap layer. Inset: schematic view of the measured structure.

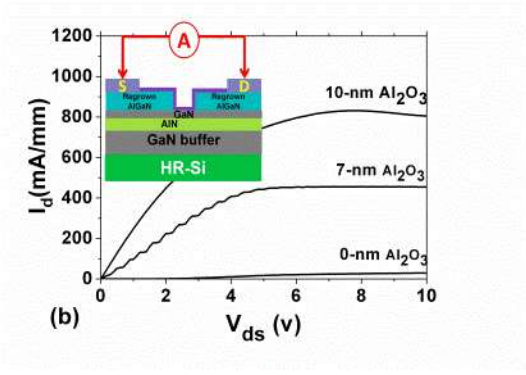

Fig. 5. DC I_d-V_{ds} characteristics of transistors before gate metal deposition with different Al_2O_3 thickness. Source-drain spacing is 4.5 μm. Inset is schematic view of the measured structure.

A scanning electron microscope (SEM) image of an E-mode device with a gate length (L_g) of 1.4 μm and 5.5 μm

source-drain spacing (L_{sd}) is shown in Fig. 6(a). The fabricated transistor shows a maximum drain current of 530 mA/mm and a peak transconductance (G_m) of 310 mS/mm (Fig. 6). The threshold voltage (V_{th}) is +0.2 V, and the V_{th} was extracted from the linear extrapolation of I_d at peak G_m. The reverse leakage was also observed to be around 3.6×10^{-4} mA/mm at V_{gs} = -1 V and V_{ds} = 6 V. The on-state resistance (R_{on}) was as low as 3.6 Ω·mm.

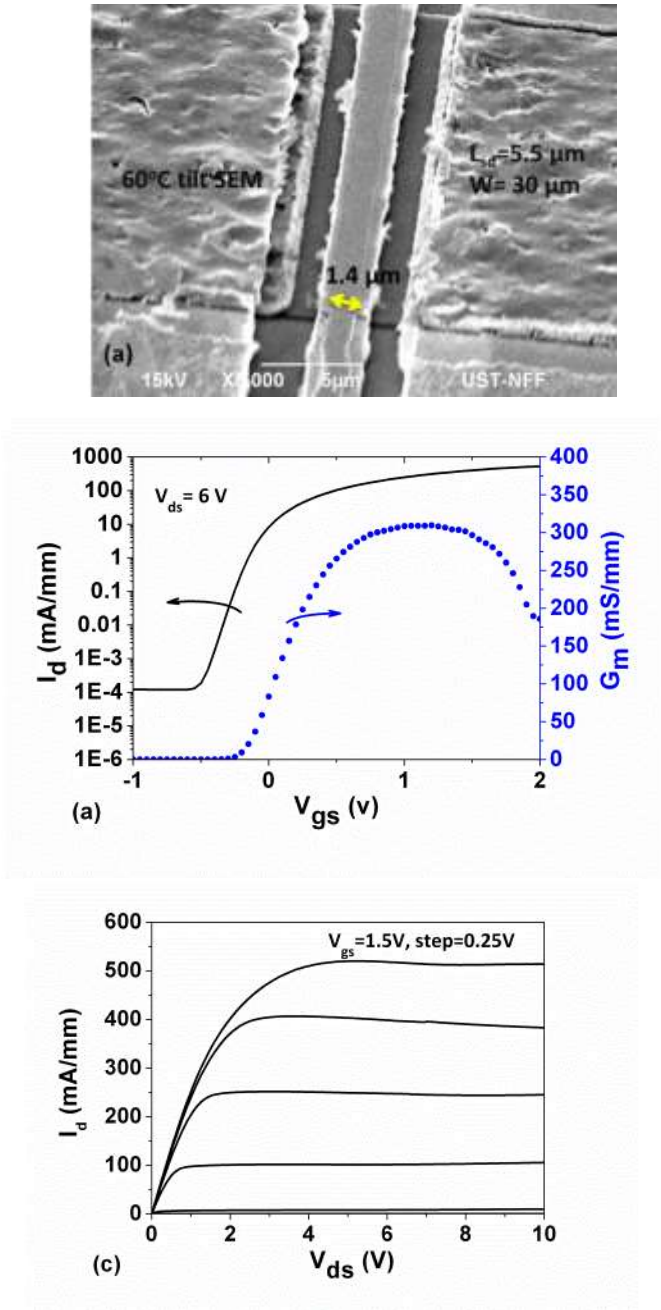

Fig. 6. (a) SEM image of the fabricated E-mode transistor with 60 °C tilt view angle. (b) Transfer and (c) DC I_d-V_{ds} characteristics for AlN/GaN MOSHEMTs carried out by annealing.

Measurement of the drift mobility was made using gated Transmission Line Method (gated TLM) [11]. Equation (1) shown below, the electron mobility could be extracted from the channel resistance in the linear region. The gate lengths and access region lengths of TLM patterns were determined by SEM. The plot of R_{on} with respect to gate length is illustrated in Fig. 7(a). R_{SD} from gated TLM is about 2.35 Ω·mm. Then the channel conductance (G_{ch}) was calculated with $G_{ch}=1/(R_{on}-R_{SD})$. The intercept with R_{on}-axis is the access resistance (R_{SD}). The 2DEG sheet charge n_s as a function of gate bias was determined from split capacitance voltage (C–V) measurements [12]. The n_s was calculated by integration of gate capacitance in (2).

$$R_m = R_{ch} + R_{SD} = \frac{L}{W \times q \times \mu_n n_s} + R_{SD} \quad (1)$$

$$n_s = \frac{1}{q}\int_{V_{th}}^{V_g} C_g dV_g \quad (2)$$

Combining (1) and (2), mobility as a function of accumulated charge concentration was obtained (Fig. 7(b)). The maximum extracted channel mobility was about 880 cm^2/Vs (Fig. 7(b)). The increase in mobility at low gate bias is due to the screening of ionized impurities and dislocation. As the gate bias increases, alloy scattering and interface roughness scattering degrade the mobility, because an increasing amount of 2DEG overcome and spill over the AlN barrier, accumulating at the dielectric/GaN interface.

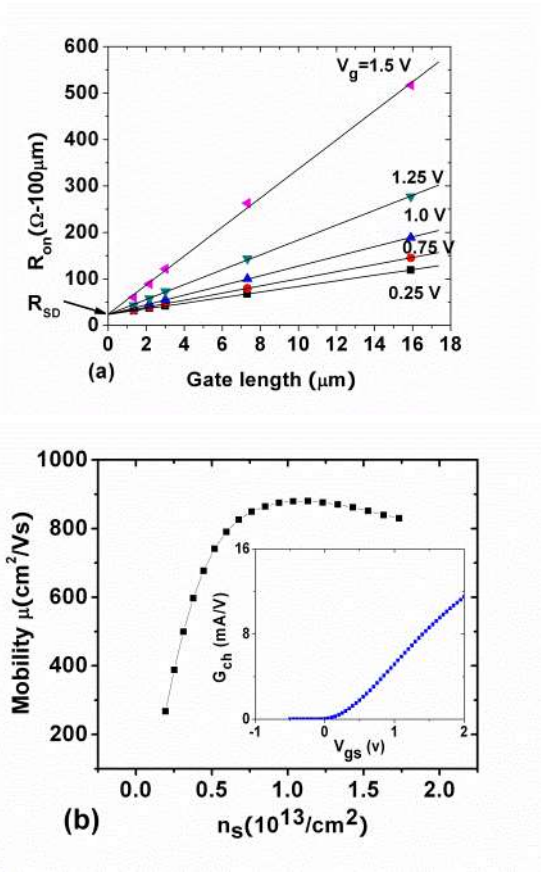

Fig. 7. (a) Plot of measured on-state resistance versus gate length (L_g) for transistors with differing L_g and varying gate voltages. The total access region length is around 4.3 µm. (b) Extracted channel mobility dependence on 2DEG concentration. Inset is the plot of channel conductance versus gate voltage.

The post-gate annealing step is critical in achieving E-mode operation. The V_{th} was unchanged even under longer annealing time (>10 min.) at 400 ^{o}C. The device fabricated without post-gate annealing exhibited D-mode properties. The transfer characteristics showed a threshold voltage around -0.8 V (Fig. 8). The peak transconductance and peak drain current were about 250 mS/mm and 0.66 A/mm, respectively. The different threshold voltage of E-mode and D-mode MOSHEMTs was a result of the post-gate annealing. Further investigation about the mechanism of V_{th} shift is in progress.

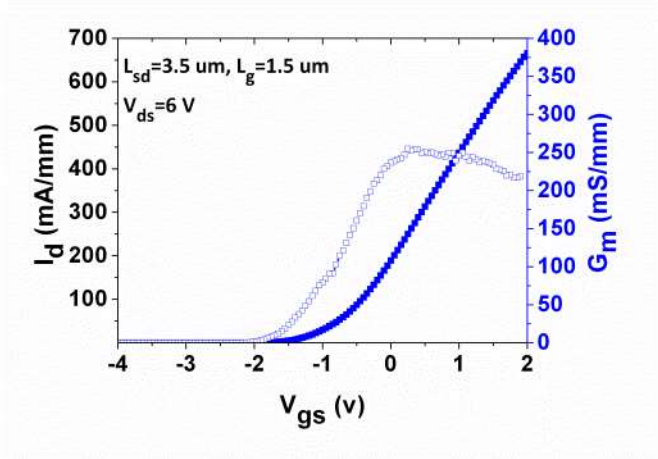

Fig. 8. DC transfer characteristics of AlN/GaN MOSHEMTs fabricated without post-gate annealing

IV. Conclusion

E-mode AlN/GaN MOSHEMTs have been fabricated by selective area regrowth of AlGaN barrier layer. The Al_2O_3 deposited by ALD could effectively increase the 2DEG density. After the post-process annealing, E-mode transistors (V_{th}= +0.2 V) were realized, exhibiting a good dc performance and extremely low I_{off}. A better performance can be expected by optimizing regrowth condition and gate length scaling. The experimental results imply that the selective area regrowth technique is a promising method for fabricating high performance E-mode AlN/GaN HFETs.

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