30-nm Inverted $In_{0.53}Ga_{0.47}As$ MOSHEMTs on Si Substrate Grown by MOCVD With Regrown Source/Drain

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***Abstract*—We report inverted-type $In_{0.51}Al_{0.49}As$/$In_{0.53}Ga_{0.47}As$ MOSHEMTs grown by MOCVD on a Si substrate. n^{++} InGaAs with an electron density of 4.5×10^{19} cm^{-3} was selectively regrown in the source/drain regions to reduce parasitic resistance while eliminating the conventional gate recess etching. A 30-nm-channel-length device was successfully demonstrated with a maximum drain current of 1698 mA/mm, a peak transconductance of 1074 mS/mm at $V_{ds} = 0.5$ V, a subthreshold slope of 172 mV/dec at $V_{ds} = 0.05$ V, and a record-low on-resistance of 133 $\Omega \cdot \mu$m. An effective mobility of 4805 $cm^2/V \cdot s$ was also extracted, indicating the high-quality metamorphic growth by MOCVD. In addition, the scalability of the inverted MOSHEMT on a Si substrate from 1 μm down to 30 nm was investigated.**

***Index Terms*—Effective mobility, InAlAs/InGaAs MOSHEMT, selective regrowth, 30-nm channel length.**

I. Introduction

As SILICON CMOS scaling has entered the "power-constrained era," high on-current at low operation voltage is required for future transistors [1]. Aiming at this target, high-mobility III–V FETs are being extensively investigated, and significant progress has been achieved [2]–[7]. However, most of these devices were built on InP substrates. In addition to the high cost and brittleness, the supply of large-area InP substrates is limited. Meanwhile, Si remains the workhorse in the IC industry and will continue to progress in its manufacturing technologies in the foreseeable future. To combine the superior carrier transport properties of III–V compounds with Si technologies, one straightforward wafer-level solution is III–V heteroepitaxy on a Si substrate [7]–[11]. By carefully managing the lattice mismatch and thermal expansion coefficient mismatch, we have previously demonstrated InGaAs HEMT on a Si substrate with promising dc and RF performance [9], [11]. A typical HEMT structure with large gate leakage and traditional topology is not suitable for future logic applications. A high-k dielectric is required ultimately. On the other hand, although 30-nm HEMT has been demonstrated with impressive logic figures of merit [12], there have been few reports on high-performance MOSFETs with scaled gate length down to sub 50 nm [13].

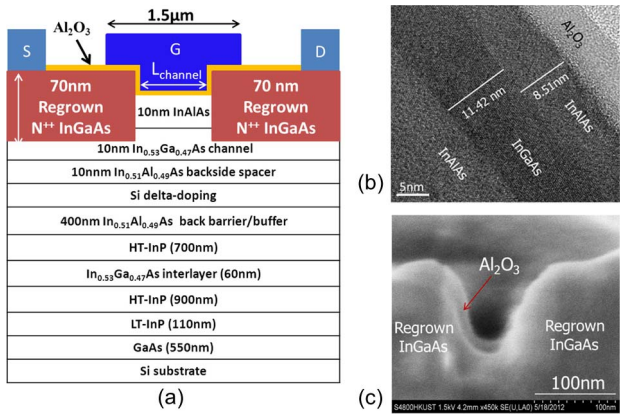

Fig. 1. (a) Schematic cross section of the finished device [(LT) low temperature and (HT) high temperature; note that the figure is not drawn to scale]. (b) TEM image of oxide/InAlAs/InGaAs active layers. (c) SEM cross-sectional image of a 30-nm-channel-length device.

Access resistance is another big concern for device scaling. Future generations of transistors will require a source resistance below 50 $\Omega \cdot \mu$m [14]. Conventional implantation in the source/drain (S/D) is difficult to meet the requirement, due to the limited activation efficiency. One emerging alternative device design is to incorporate regrown S/D with high doping concentrations for ohmic contacts [3]–[5], and a low parasitic resistance can be achieved. In this work, a 30-nm InGaAs MOSHEMT on a Si substrate with regrown S/D and a record-low on-resistance of 133 $\Omega \cdot \mu$m was demonstrated. The scalability of the drive current and extrinsic transconductance was also investigated.

II. Experiment

Four-inch exact-(001)-oriented Si substrates were used for metamorphic growth. Si wafers were cleaned in a boiling $NH_4OH : H_2O_2 : H_2O$ (1 : 1 : 5) solution, followed by a $HF : H_2O$ (1 : 40) dip. Epitaxial growth was carried out in an Aixtron 200/4 MOCVD system. The substrate was annealed at 810 °C in H_2 for 30 min, and AsH_3 was introduced at the end of the annealing. Fig. 1(a) shows the cross-sectional schematic of the nominal structure grown. The composite buffer stack consists of a 10-nm GaAs nucleation layer deposited at 400 °C, 540-nm GaAs grown at graded temperatures of 550 °C, 590 °C, and 630 °C, a 110-nm InP nucleation layer deposited at 450 °C,

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1.6-μm InP grown at 600 °C (with a 60-nm $In_{0.6}Ga_{0.4}As$ interlayer inserted in the middle), and a 400-nm $In_{0.51}Al_{0.49}As$ buffer layer. The inverted-type InAlAs/InGaAs HEMT structure includes a 10-nm $In_{0.51}Al_{0.49}As$ top barrier, a 10-nm $In_{0.53}Ga_{0.47}As$ channel, and a 10-nm $In_{0.51}Al_{0.49}As$ backside spacer. Si delta doping was inserted under the $In_{0.51}Al_{0.49}As$ spacer. From van der Pauw–Hall measurements, 2-D electron gas mobilities of 6700 and 26 800 $cm^2/V \cdot s$ were obtained at 300 K and 77 K, respectively, with a corresponding sheet carrier density of $2 \times 10^{12}/cm^2$. Compared with those of identical HEMTs grown on GaAs substrates, the mobility values are about 20% less, relating to a rougher surface (the root mean squares of AFM for an InP buffer on GaAs and Si were 1.8 and 2.5 nm, respectively).

A gate-last process was developed to fabricate MOSHEMTs with regrown S/D. The as-grown HEMT wafer was first passivated by SiO_2 (1000 Å) as regrowth mask. Then, the SiO_2 was patterned by BOE wet etching, followed by S/D recess etching down to the InGaAs channel using a $H_3PO_4 : H_2O_2 : H_2O$ (3:1:50) solution. The recess etch is not critical as long as it terminates somewhere within the channel. Then, 70 nm of Si-doped n^{++} InGaAs with an electron concentration of 4.5×10^{19} cm^{-3} was regrown in the exposed S/D regions by MOCVD at 600 °C, using TEGa, TMIn, TBA, and SiH_4 as precursors. The growth rate was around 15 nm/min. Due to loading effects in the selective growth, InGaAs close to the SiO_2 mask grows a little bit faster. Mesa isolation was formed by wet etching down to the InAlAs buffer, and the SiO_2 regrowth mask was removed by BOE. The gate width was defined by the mesa width, which was designed to be 10 μm but shrunk to 9.57 μm due to the lateral etch undercut. After surface cleaning using $HCl : H_2O$ (1:10) for 2 min followed by $(NH_4)_2S$ passivation for 20 min, the sample was immediately loaded into an Oxford OpAL atomic layer deposition (ALD) system. *In situ* TMA pretreatment was performed in the ALD chamber using ten cycles of TMA/Ar. Six nanometers of Al_2O_3 was deposited on the sample at 300 °C using TMA and water as precursors, followed by post deposition annealing at 380 °C for 30 min using N_2 in the ALD chamber. S/D contact holes were subsequently opened, and nonalloyed ohmic contacts were achieved by electron-beam evaporation of Ni/Ge/Au/Ge/Ni/Au and lift-off process. Finally, Ti/Pt/Au gate metallization was realized. The schematic of the finished device with nominal layer thicknesses is shown in Fig. 1(a). Fig. 1(b) shows a cross-sectional TEM image of the oxide and active layers. Fig. 1(c) shows a SEM cross-sectional image of a 30-nm-channel-length device.

III. Results and Discussion

Fig. 2 shows the output characteristics and transfer characteristics of a 30-nm device. A maximum drain current $(I_{ds,max})$ of 1698 mA/mm was obtained at $V_{gs} = 1.5$ V and $V_{ds} = 0.5$ V, and a peak extrinsic transconductance $(G_{m,max})$ of 1074 mS/mm was achieved at $V_{ds} = 0.5$ V. The threshold voltage (V_{th}) is determined to be -1.32 V by a linear extrapolation method from the I_{ds}–V_{gs} curve at $V_{ds} = 50$ mV. The gate leakage current was 8.3×10^{-4} mA/mm at $V_{gs} = 1.5$ V and $V_{ds} = 0.5$ V, which was over six orders lower than the $I_{ds,max}$ of 1698 mA/mm obtained at the same drain bias. An ultralow R_{on} of 133 $\Omega \cdot \mu$m was extracted from the I_{ds}–V_{ds} curve, which could be attributed to the raised S/D with high doping level

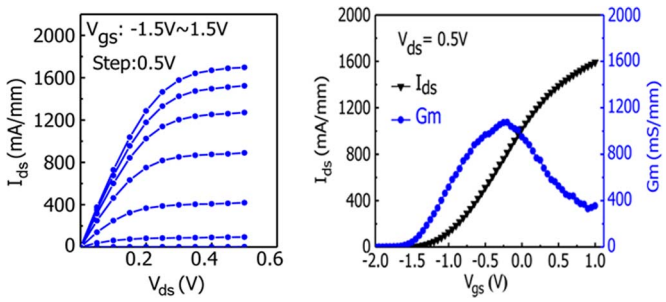

Fig. 2. (Left) Output characteristics of a device with an L_{ch} of 30 nm. (Right) Transfer characteristics of a device with an Lch of 30 nm.

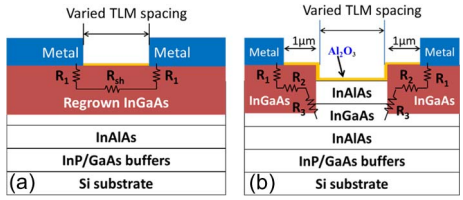

Fig. 3. Extraction of access resistance using (a) TLM-1 and (b) TLM-2.

by regrowth. To evaluate the access resistance components, including the contact resistance (R_1) between the S/D metal and regrown InGaAs, the series resistance (R_2) of the regrown InGaAs, and the regrowth interface resistance (R_3) caused by interfacial defects, two transmission line matrix (TLM) patterns were designed as shown in Fig. 3. The average sheet resistance of the regrown $In_{0.53}Ga_{0.47}As$ $(R_{sh} = 22.4\ \Omega/\square)$ and $R_1 = 8.3\ \Omega \cdot \mu$m were determined from TLM-1, while the average values of $R_2 = 22.4\ \Omega \cdot \mu$m and $R_3 = 31.9\ \Omega \cdot \mu$m were deduced from TLM-2. The total access resistance of $2(R_1 + R_2 + R_3)$ ranged from 116.6 to 136.2 $\Omega \cdot \mu$m across the sample with an average value of 125 $\Omega \cdot \mu$m, which agreed well with the R_{on} of 133 $\Omega \cdot \mu$m.

Fig. 4 (left) shows the subthreshold characteristics of the 30-nm-channel-length device. The subthreshold slope (SS) was 172 mV/dec at $V_{ds} = 50$ mV. Another device with an L_{ch} of 340 nm exhibited a lower SS of 127 mV/dec at $V_{ds} = 50$ mV. In addition, the devices exhibited a somewhat large OFF-state current (I_{off}). The current SS and I_{off} are believed to be limited by the capacitance equivalent thickness arising from the thick Al_2O_3 and InAlAs, as well as the backside δ-doping structure, resulting in a small I_{on}/I_{off}. More efforts are being made to improve gate electrostatic control over the channel. Effective mobility (μ_{eff}) was extracted as a function of carrier density using a combination of 1-MHz capacitance–voltage (CV) and I_{ds}–V_{ds} measurements [15]. As shown in the right side of Fig. 4, a high peak μ_{eff} of 4805 $cm^2/V \cdot s$ was obtained for our buried-channel MOSHEMT on a Si substrate with an L_{ch} of 1 μm. Although our device was metamorphically grown on a Si substrate, it exhibited a competitive μ_{eff} compared to lattice-matched devices on InP, indicating the high-quality epitaxial growth by MOCVD.

Transistor scalability is also a major issue. It is still uncertain whether future III–V transistors will be able to scale to the required dimensions while preventing excessive short-channel effects and attaining the demanding parasitic resistance objective [1]. The scalability of the MOSHEMT on a Si substrate was investigated in this work. Fig. 5 (left) shows the $I_{ds,max}$ and $G_{m,max}$ as functions of the channel length ranging from

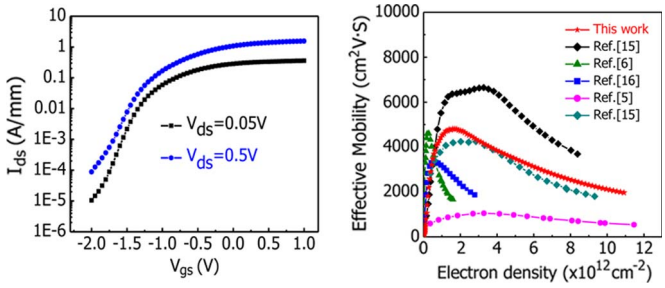

Fig. 4. (Left) Subthreshold characteristics of a device with an $L_{\rm ch}$ of 30 nm. (Right) Comparison of effective mobilities with other works.

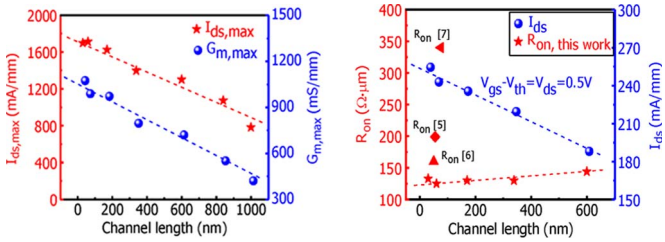

Fig. 5. (Left) $I_{\rm ds,max}$ and $G_{m,\rm max}$ of MOSHEMT as functions of the channel length. (Right) $I_{\rm ds}$ at $V_{\rm gs}-V_{\rm th}=V_{\rm ds}=0.5$ V and $R_{\rm on}$ versus channel length.

1 μm to 30 nm. $I_{\rm ds,max}$ was measured at $V_{\rm gs}=1.5$ V and $V_{\rm ds}=0.5$ V, while $G_{m,\rm max}$ was measured at $V_{\rm ds}=0.5$ V. The device performance scaled well with channel length. In addition, as shown in Fig. 2, the 30-nm device still exhibits excellent saturation characteristics and ultralow $R_{\rm on}$, and no obvious short-channel effect was observed. Fig. 5 (right) shows the $R_{\rm on}$ and drain current $(I_{\rm ds})$ at $V_{\rm gs}-V_{\rm th}=V_{\rm ds}=0.5$ V as functions of the channel length. The $R_{\rm on}$ of state-of-the-art InGaAs MOSFETs in the literature is included for comparison. A record-low $R_{\rm on}$ of 125 $\Omega\cdot\mu$m has been achieved for our 60-nm device.

IV. Conclusion

Thirty-nanometer inverted $In_{0.53}Ga_{0.47}As$ MOSHEMTs on a Si substrate grown by MOCVD with an $I_{\rm ds,max}$ of 1.698 A/mm and a record-low $R_{\rm on}$ of 133 $\Omega\cdot\mu$m have been reported. A peak effective mobility up to 4805 cm^2/V $\cdot$ s was obtained. The devices showed good scalability with the channel length from 1 μm to 30 nm. Our results indicate that combining an InAlAs/InGaAs HEMT structure with S/D regrowth is promising for future high-speed and low-power logic applications.

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