30nm Enhancement-mode $In_{0.53}Ga_{0.47}As$ MOSFETs on Si Substrates Grown by MOCVD Exhibiting High Transconductance and Low On-resistance

Xiuju Zhou, Qiang Li, Chak Wah Tang and Kei May Lau
Department of Electronic & Computer Engineering, Hong Kong University of Science and Technology,
Clear Water Bay, Kowloon, Hong Kong
Tel: (852) 23587049, Fax: (852) 23581485, Email: eekmlau@ust.hk

Abstract

This paper describes the development of 30nm enhancement-mode $In_{0.53}Ga_{0.47}As$ MOSFETs grown on Si substrates featuring Al_2O_3/InAlAs composite gate stack with extrinsic transconductance of 1700mS/mm at V_{ds}=0.5V and on-resistance of 157 Ω·μm. A low-temperature process of post metallization annealing has been developed to achieve enhancement-mode operation. Capacitance-Voltage measurements and TEM observation were carried out to investigate the mechanisms of threshold voltage shift. Furthermore, device scalability down to 30nm is reported.

Introduction

Because of the low electron effective mass and associated high mobility/carrier velocity, InGaAs related III-V compounds are gaining increasing attention as alternative n-channel materials for Post-Si CMOS [1]. Although surface-channel design is desirable from the scaling point of view, the effective channel mobility is jeopardized by the problematic high-k/III-V interface [2]. One strategy to resolve this issue is burying the channel beneath a thin wide-bandgap material, such as InAlAs or InP upper barrier. Compared with InP, $In_{0.52}Al_{0.48}As$ offers much larger band offset with InGaAs quantum well, thus better carrier confinement. In growth, it is more challenging to achieve high interfacial quality at InGaAs/InP, which requires switching of two different group V elements. Reported research indicated that the inverted InGaAs/InP interface tends to be compositionally graded and shows surface undulations [3], whereas the InGaAs/InAlAs one is flat and abrupt. Therefore, the use of high-*k*/InAlAs composite as gate stack in III-V MOSFETs is a good option to explore. Using scaled Si MOSFETs for baseline comparison, III-V MOSFETs with deeply scaled physical gate length are being investigated and significant progress has been made in InGaAs MOSFET with gate lengths in the 50-100nm range [4-6]. However, there are few reports on high performance sub-50nm devices [2]. Recently, we have demonstrated 30nm depletion-mode $In_{0.53}Ga_{0.47}As$ MOSFETs with $In_{0.51}Al_{0.49}As$ upper barrier [7]. But the weakened gate electrostatic control is also a well-known drawback of the buried channel design. In this paper, we report a low-temperature process of post-metallization-annealing (PMA) to achieve enhancement-mode (E-mode) operation. Significantly improved on-state and off-state performance are demonstrated compared to our previously reported work. Meanwhile, a high effective mobility (μ_{eff}) up to 5068 $cm^2/V{\cdot}s$ was obtained due to the buried channel.

Material Growth and Device Fabrication

The $In_{0.51}Al_{0.49}As/In_{0.53}Ga_{0.47}As$ buried quantum-well (QW) structure was grown on exact-(001)-orientated Si substrates using an Aixtron 200/4 MOCVD system. Fig.1a depicts the cross-sectional schematic of the nominal layered device structure. A simulated band diagram with corresponding electron distribution is illustrated in Fig.1b. Fig.1c and Fig.1d show the cross-sectional TEM images of the complete epi-structure including buffer layers and InAlAs/InGaAs active layers with the Al_2O_3, respectively. The buffer layers effectively block the propagation of most dislocations into the active layers. The detailed growth scheme has been described elsewhere [7].

The fabrication process starts with the deposition of 1000Å SiO_2 as regrowth mask. Source/drain (S/D) region was opened by selectively removing SiO_2 using buffered oxide etch (BOE). Exposed S/D area was further etched down to the InGaAs channel and refilled by 70nm n^{++} $In_{0.53}Ga_{0.47}As$ with an electron density of $4.5x10^{19}cm^{-3}$. Then mesa isolation was formed and the SiO_2 regrowth mask was removed. After surface treatment using HCl for 2min and $(NH_4)_2S$ for 20min, a 6nm-thick Al_2O_3 gate dielectric was deposited by ALD at 300˚C, followed by in-situ post deposition annealing (PDA) at 380 ˚C for 30min in N_2 ambient. S/D ohmic contacts were formed by e-beam evaporation of Ni/Ge/Au/Ge/Ni/Au and lift off process, followed by Ti/Pt/Au gate metallization. Finally, the key step for E-mode device, PMA, was performed in the ALD chamber at 300˚C for 5min in a N_2 ambient at a pressure of 170 mTorr. A schematic of the finished device with nominal layer thicknesses is depicted in Fig.1a. Fig.2a-c presents the AFM and SEM images of a 30nm channel-length (L_{ch}) device.

X-ray photoelectron spectroscopy (XPS) was carried out to probe the chemical components at the oxide/InAlAs interface. Fig.3 illustrates the As-*3d*, As-*2p* and In-*3d* XPS spectra for the InAlAs surface after gate dielectric deposition and PDA. No peaks from As- or In-related oxide were detected, suggesting the surface passivation is effective in removing native oxide on the as-grown InAlAs.

Device Characterizations and Discussion

Fig.4 shows the transfer characteristics of the 30nm channel-length device at V_{ds} = 0.5V before and after PMA. Threshold voltage (V_{th}) is extracted by liner extrapolation at V_{ds} = 50mV from the I_{ds} -V_{ds} curve. V_{th} is shifted from -1.4V to +0.08V after PMA, resulting in E-mode operation. Due to the enhanced gate electrostatic control, the peak

transconductance (Gm_{max}) was greatly improved from 1074mS/mm to 1700mS/mm. The PMA was also beneficial to the off-state performance. As illustrated in Fig.5, the subthreshold slope (SS) at V_{ds} = 50mV was reduced from 172 to 142mV/dec, and the SS at V_{ds} = 0.5V decreased from 205 to 186mV/dec after PMA. An I_{on}/I_{off} ratio of 1.7 x 10^4 has been achieved, where I_{on} and I_{off} are measured at $V_{gs}=V_{th}+0.5V$ and $V_{gs}=V_{th}-0.5V$, respectively. A device with a longer channel length of 60nm exhibits a lower SS of 101mV/dec at V_{ds}=0.05V, SS of 120mV/dec at V_{ds}=0.5V, and drain induced barrier lowering (DIBL) of 138mV/V, as shown in Fig.6. Fig.7 gives the output characteristic of the E-mode device with L_{ch} of 30nm. A maximum drain current ($I_{ds,max}$) of 1327 mA/mm was obtained at V_{ds}=0.5V and V_{gs} = 1.6V. An on-resistance (R_{on}) of 157 Ω·μm was extracted from the I_{ds} -V_{ds} curve, which agrees well with the low contact resistance of 8 Ω·μm and access resistance of 125 Ω·μm from TLM measurement as described in [7].

Fig.8-10 illustrate the $I_{ds,max}$ and R_{on}, Gm_{max}, SS and DIBL as a function of channel length, respectively. Significant improvement of device performance including Gm_{max}, SS and DIBL is achieved by PMA, with the exception of maximum drain current due to the reduced overdrive voltage. The device performance scales well with channel length. The smallest, 30nm device shows some performance degradation due to short-channel effect. Fig.11-13 compare the Gm_{max}, R_{on} and SS of our devices with state-of-the-art InGaAs MOSFETs in literature, respectively. Our devices exhibit high Gm_{max} at low supply voltage and the lowest R_{on}. We attribute the impressive R_{on} to the high-quality S/D regrowth with high doping level. Effective mobility was extracted using a combination of 1MHz Capacitance-Voltage (C-V) and I_{ds}-V_{ds} measurement [8]. A high peak μ_{eff} of 5068 $cm^2/V{\cdot}s$ was obtained for our buried channel MOSFET on Si substrate with a channel length (L_{ch}) of 0.85μm.

Post Metallization Annealing

To investigate the effects of PMA, ring capacitors with diameter of 160μm were fabricated using the same gate process. Fig.14 compares the 1MHz C-V response of a Al_2O_3/InAlAs/ InGaAs capacitor before and after PMA. The positively shifted C-V curve agrees well with the change of V_{th} in Fig.4. The sample without PMA shows a hysteresis of 105 mV, whereas the PMA treated sample exhibits almost "zero" hysteresis with a maximum shift less than 30 mV, indicating an improved gate stack quality. The capacitance equivalent thickness (CET) of the composite gate stack decreases from 6.1nm to 4.8nm after PMA. Fig.15 illustrates high-resolution TEM images of the gate metal-Ti/Al_2O_3/InAlAs gate stacks. Physical thickness of the Al_2O_3 shrunk from 5.8 to 4.6nm, correspondingly, equivalent oxide thickness (EOT) reduced from 2.8nm to 2.2nm after PMA, which agree well with the CET reduction extracted from the C-V curve in Fig.14. The vertical scaling of InAlAs upper barrier would further enhance dc characteristics, especially the off-state performance. In addition to the increased gate capacitance, we speculate there are other effects from the PMA, contributing to the aggressive V_{th} shift in Fig.4. Recently, Lin et al. reported that reactive ion etching (RIE) induced damage to III-V MOSFET can be annealed out through a low-temperature annealing process. Positively shifted threshold voltage and increased accumulation capacitance were also observed in the annealed devices [9]. Although no RIE was involved in our MOSFET fabrication, damage in the gate metal layer caused by E-beam metallization was observed (Fig.15a). After the PMA process, these damages were recovered as shown in Fig.15b, leading to a smooth and densified Ti layer, which might increase the effective work function of gate metal and reduce the charges in gate stacks. From the analysis of energy dispersive x-ray spectroscopic (EDS) equipped in TEM system, some oxygen was detected in this "damaged" metal layer, whereas no oxygen was detectable after PMA. Moreover, abrupt and flat gate metal/oxide/InAlAs interfaces could also be observed from Fig.15.

Conclusion

We have developed a PMA process to achieve E-mode $In_{0.53}Ga_{0.47}As$ buried channel MOSFETs. 30nm E-mode $In_{0.53}Ga_{0.47}As$ MOSFETs on Si substrates featuring Al_2O_3/ InAlAs gate stack exhibit high transconductance and low on-resistance. Our results indicate that application of source/drain regrowth and PMA on the InAlAs/InGaAs quantum-well device structure without e-beam lithography can lead to high speed and low power sub-50nm E-mode devices.

Reference

[1] J. A. del Alamo, "Nanometer-scale electronics with III-V compound semiconductors," *Nature*, vol. 479, no.7373, pp. 317-323, Nov. 2011.

[2] F. Xue et al., "Sub-50-nm $In_{0.7}Ga_{0.3}As$ MOSFETs with various barrier layer materials," *IEEE Electron Device Lett.*, vol.33, no.1, pp. 32-34, Jan. 2012.

[3] J. Decobert and G. Patriarche, "Transmission electron microscopy study of the InP/InGaAs and InGaAs/InP heterointerfaces grown by metalorganic vapor-phase epitaxy," *Journal of Applied Physics*, vol.92, no.10, pp. 5749-5755, Nov. 2002.

[4] M. Egard et al., "High transconductance self-aligned gate-last surface channel $In_{0.53}Ga_{0.47}As$ MOSFET," in *IEDM Tech. Dig.*, 2011, pp.303-306.

[5] M.Radosavljevic et al., "Advanced High-K gate dielectric for high-performance short-channel $In_{0.7}Ga_{0.3}As$ quantum well field effect transistors on silicon substrate for low power logic applications," in *IEDM Tech. Dig.*,2009, pp.319-321.

[6] Y. Yonai, T. Kanazawa, D. Ikeda, and Y. Miyamoto*," "* High drain current (>2A/mm) InGaAs channel MOSFET at V_D=0.5V with shrinkage of channel length by InP anisotropic etching," in *IEDM Tech. Dig.*,2011, pp.307-310.

[7] X. Zhou, Q. Li, C. W. Tang and K. M. Lau *"*30nm inverted $In_{0.53}Ga_{0.47}As$ MOSHEMTs on Si substrate grown by MOCVD with regrown source/drain," *IEEE Electron Device Lett.,* In press.

[8] S. J. Bentley et al., "Electron mobility in surface- and buried-channel flatband $In_{0.53}Ga_{0.47}As$ MOSFETs with ALD Al_2O_3 gate dielectric," *IEEE Electron Device Lett.,* vol.32, no. 4, pp. 494-496, Apr.2011.

[9] J. Lin, T-W. Kim, D. A. Antoniadis, and J. A. del Alamo, "A self-aligned InGaAs quantum-well metal–oxide–semiconductor field-effect transistor fabricated through a lift-off-free front-end process," *Appl. Phys. Express*, vol.5, no.6, pp. 064002-1-064002-3, May. 2011.

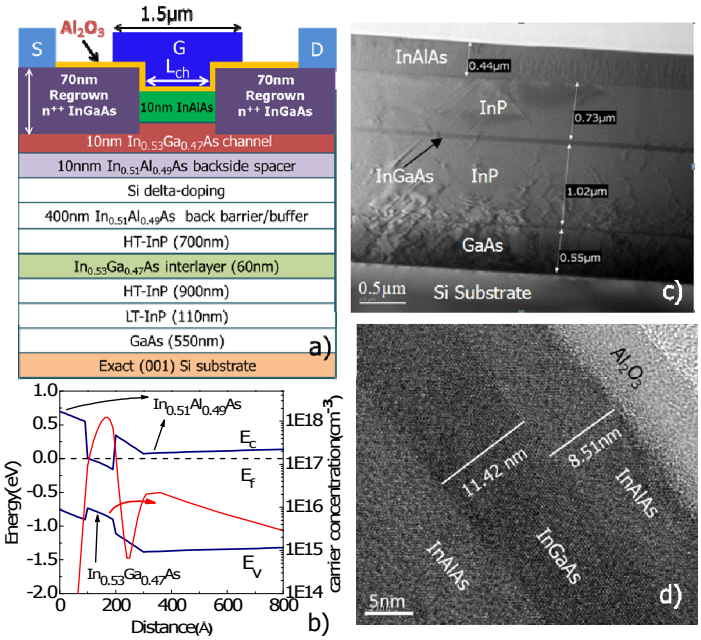

Fig.1: (a) Schematic of device with nominal layer thicknesses (LT-low temperature, HT-high temperature, note: figure is not drawn to scale), (b) Simulated band diagram and carrier distribution of the quantum well structure corresponding to Fig.1a, (c) Cross-sectional TEM image of the composite buffer layers grown on Si substrate, (d) Cross-sectional TEM image of oxide and InAlAs/InGaAs active layers with gate oxide.

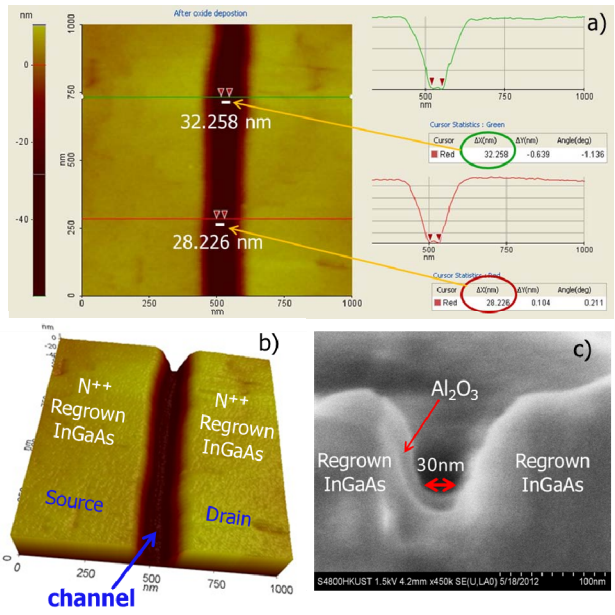

Fig.2: (a) AFM line profile of a L_{ch}=30nm device scanned after gate dielectric deposition. The channel length is defined by the regrown source/drain separation. Several positions have been measured across the channel with an average L_{ch} of 30nm. Two representative positions (red line and green line) were shown, (b) 3-dimentional AFM image corresponding to Fig.2a, (c) Cross-sectional SEM image of a L_{ch}=30nm device after whole process.

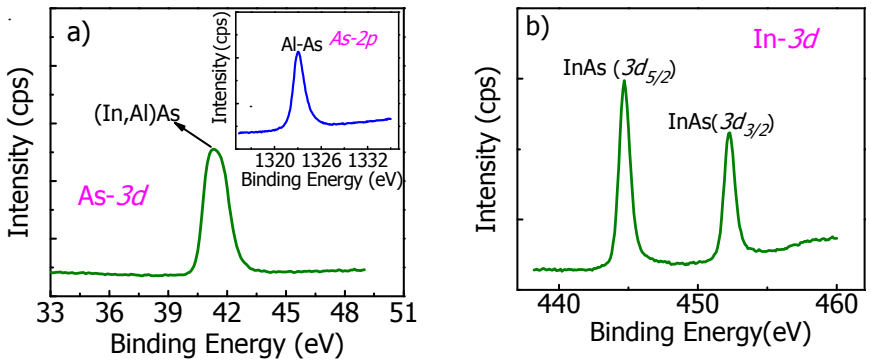

Fig.3: (a) As-*3d* and As-*2p* *(b)*In-*3d* XPS spectrum at Al_2O_3/InAlAs interface after ALD and PDA. No peaks from As- or In-related oxide were detected, indicating that the surface passivation could effectively remove native oxide on the as-grown InAlAs.

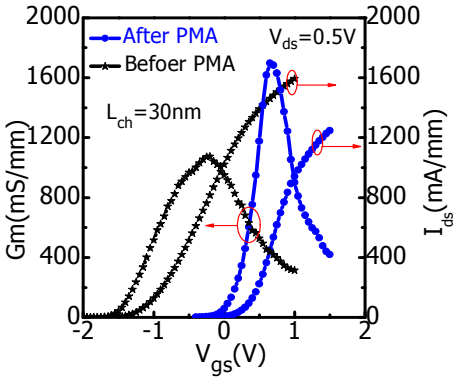

Fig.4: Transfer characteristics of a 30nm device measured with the device in Fig.2 before/after PMA.

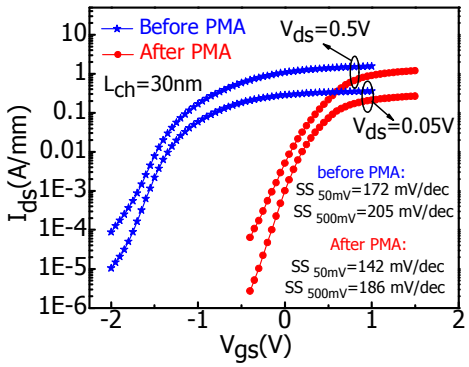

Fig.5: Subthreshold characteristics of a 30nm channel -length device before and after PMA.

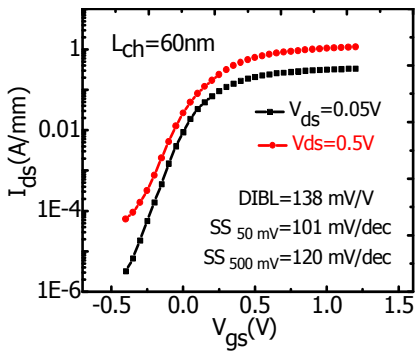

Fig.6: Transfer characteristics of a device with a L_{ch} of 60nm after PMA

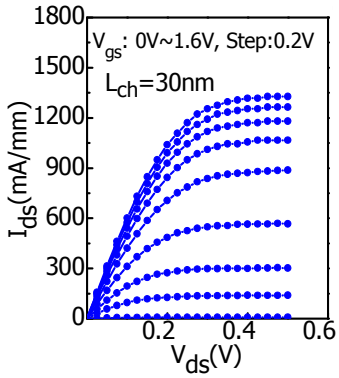

Fig.7: Output characteristics of a 30nm channel -length E-mode device after PMA

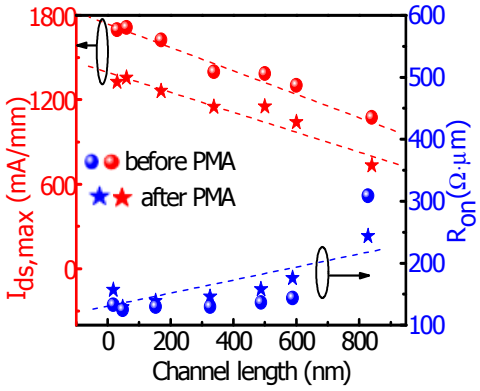

Fig.8: Maximum drain current ($I_{ds,max}$) at V_{ds}=0.5V and on-resistance (R_{on}) as a function of channel length.

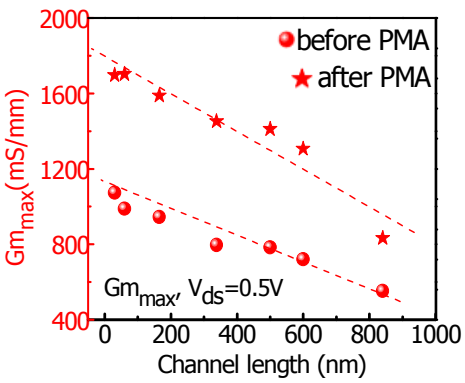

Fig.9: Peak transconductance (Gm_{max}) measured at V_{ds}=0.5V as a function of channel length.

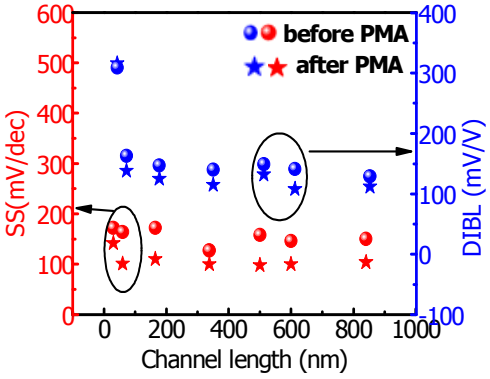

Fig.10: Subthreshold slope (SS) at V_{ds}=0.5V and drain induced barrier lowering (DIBL) as a function of channel length

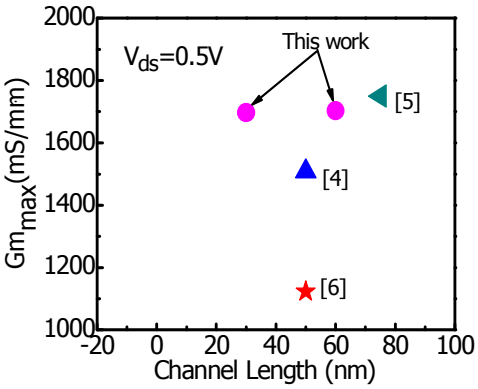

Fig.11: Comparison of Gm_{max} measured at V_{ds}=0.5V with state-of-the-art InGaAs MOSFETs

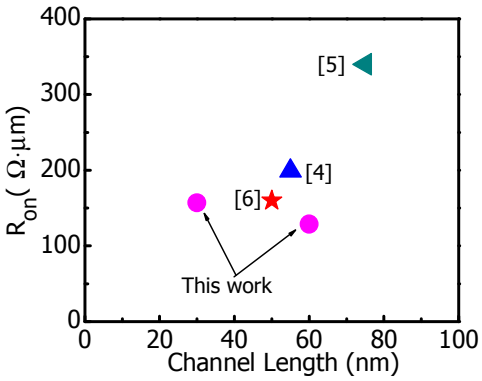

Fig.12: Comparison of R_{on} with state-of-the-art InGaAs MOSFETs

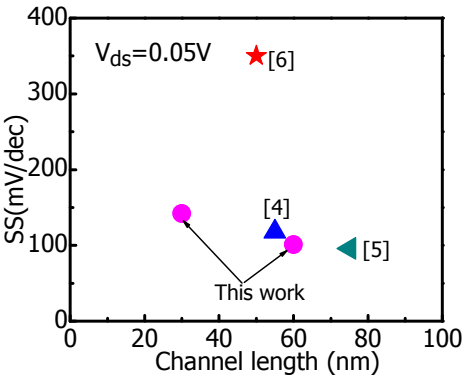

Fig.13: Comparison of SS measured at V_{ds}=0.05V with state-of-the-art InGaAs MOSFETs

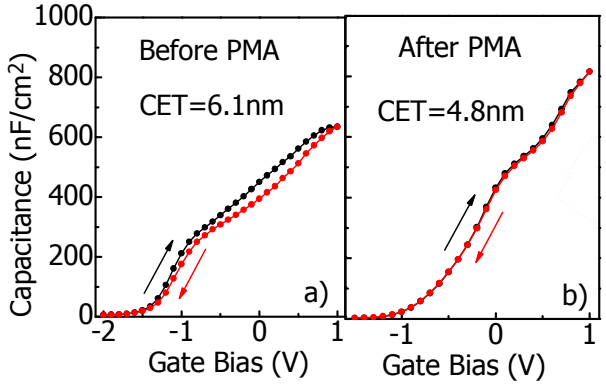

Fig.14: 1MHz C-V measurement of Al_2O_3/InAlAs/ InGaAs capacitor before and after PMA, where the gate bias was swept bi-directionally. Increased gate capacitance and greatly reduced hysteresis are obtained after PMA.

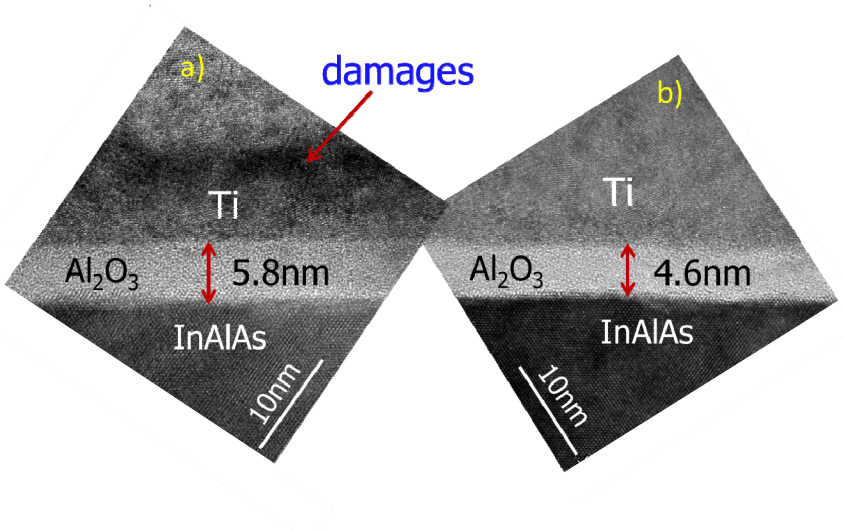

Fig15: High-resolution cross-sectional TEM images of gate metal/oxide/InAlAs gate stacks before (a) and after (b) PMA, showing reduced oxide thickness and recovered damages from E-beam metallization, leading to abrupt and flat Ti/oxide/InAlAs interfaces.