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$In_{0.53}Ga_{0.47}As$ MOS-HEMTs on GaAs and Si substrates grown by MOCVD

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High-performance $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor high-electron-mobility-transistors (MOS-HEMTs) on GaAs substrates grown by metal organic chemical vapor deposition (MOCVD) are demonstrated. A low-temperature process has been developed to achieve low contact resistances while maintaining the quality of the dielectric/III–V interface. Atomic-layer-deposited Al_2O_3 was used as the gate dielectric on top of a δ-doped $In_{0.51}Al_{0.49}As/In_{0.53}Ga_{0.47}As$ metamorphic heterostructure. A 1-μm gate-length device exhibits a maximum drain current of 646 mA/mm and an extrinsic peak transconductance of 575 mS/mm, respectable values for III–V metal-oxide-semiconductor field-effect transistors (MOSFETs) on GaAs substrates. In addition, preliminary results of $In_{0.53}Ga_{0.47}As$ MOS-HEMTs on Si substrates, also grown by MOCVD, are presented for comparison.

1 Introduction In anticipation of reaching the physical limits of Si-based CMOS scaling, III–V compound semiconductors have been considered as promising channel materials due to their superior electron transport properties. Without a definitive good dielectric like those for Si, practical III–V MOSFETs are still under intensive research. Currently, various device configurations [1], including MOS-HEMT, are being actively explored and significant progress has been achieved [2–10]. Specifically, most of these devices are built on InP substrates with materials deposited by molecular-beam-epitaxial (MBE). Reports of devices grown on GaAs or Si substrates using metal organic chemical vapor deposition (MOCVD) growth technology are rare. In addition to the high cost and brittleness, the supply of large area InP substrate is limited. It is desirable to use commercially available large area GaAs or Si substrates, even during the technology development stage, making them one step closer to the eventual goal of large-scale integration of devices and circuits. Compared to MBE, MOCVD is preferred for high volume manufacturing.

MOS-HEMT is a promising candidate for high-speed low-power logic applications. It offers higher channel mobility in the two-dimensional electron gas (2DEG) than conventional III–V MOSFETs, as well as lower gate leakage compared to conventional HEMTs. It is well known that III–V MOSFETs usually have low thermal tolerance in the device fabrication process. Degradation of the interface between the gate oxide and III–V materials after high-temperature process, such as ion-implantation activation used in inversion-mode MOSFETs is commonly observed [1, 11]. For III–V integration on Si substrates, the large mismatch in the thermal expansion coefficient also requires a low thermal budget processing.

In this work, we report $In_{0.53}Ga_{0.47}$ As metamorphic MOS-HEMTs on both GaAs and Si substrates grown by MOCVD. 1-μm gate-length devices on GaAs substrates exhibited a maximum drain current I_{dss} of 646 mA/mm and an extrinsic peak transconductance G_m of 575 mS/mm, which are significant improvement over recently reported III–V MOS-HEMTs on GaAs substrates [12–15]. The preliminary results of InGaAs MOS-HEMT on Si substrate, also grown by MOCVD, is presented for comparison.

2 Experimental The InAlAs/InGaAs metamorphic HEMT (mHEMT) structures were grown on 4-inch GaAs and Si substrates using an Aixtron AIX-200/4 MOCVD system. The detailed epitaxial layer structures on different substrates are shown in Figs. 1 and 2. All the layers were compositionally lattice-matched to InP. From room-temperature Hall measurements, 2DEG carrier concentrations of 4.9×10^{12} and $3.0 \times 10^{12}\,cm^{-2}$, with electron

$In_{0.53}Ga_{0.47}As$: Si, 5 × $10^{18}cm^3$, 15nm,	Cap layer
Undoped $In_{0.51}Al_{0.49}As$, 25nm,	Barrier
Si δ-doping, $4x10^{12}/cm^2$	Delta doping
Undoped $In_{0.51}Al_{0.49}As$, 5nm,	Spacer
Undoped $In_{0.53}Ga_{0.47}As$, 18nm,	Channel
Undoped HT- $In_{0.51}Al_{0.49}As$, 100nm	Buffer 5
Undoped LT- $In_{0.51}Al_{0.49}As$, 200nm	Buffer 4
Undoped HT-InP, 650nm	Buffer 3
Undoped LT-InP, 110nm	Buffer 2
Undoped GaAs, 100nm	Buffer 1
Semi-insulating GaAs substrate	

Figure 1 mHEMT layer structure grown on GaAs substrate (LT – low temperature, HT – high temperature).

$In_{0.53}Ga_{0.47}As$: Si, 5 × $10^{18}cm^3$, 15nm,	Cap layer
Undoped $In_{0.51}Al_{0.49}As$, 25nm,	Barrier
Si δ-doping, $4x10^{12}/cm^2$	Delta doping
Undoped $In_{0.51}Al_{0.49}As$, 5nm,	Spacer
Undoped $In_{0.53}Ga_{0.47}As$, 30nm,	Channel
Undoped HT- $In_{0.51}Al_{0.49}As$, 100nm	Buffer 5
Undoped LT- $In_{0.51}Al_{0.49}As$, 200nm	Buffer 4
Undoped HT-InP, 650nm	Buffer 3
Undoped LT-InP, 110nm	Buffer 2
Undoped HT-GaAs, 100nm	Buffer 1
Undoped LT-GaAs, 10nm	Nucleation
P-type Si substrate	

Figure 2 mHEMT layer structure grown on Si substrate.

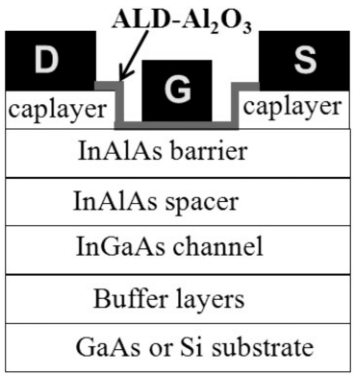

Figure 3 Schematic of MOS-HEMT on GaAs and Si substrate.

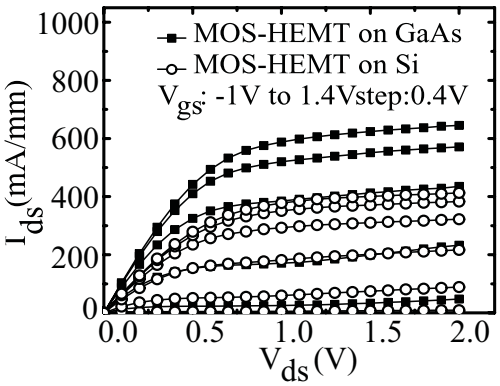

Figure 4 I_{ds}–V_{ds} characteristics of InGaAs MOS-HEMTs on GaAs and Si substrates.

mobilities of 7600 and 4020 cm^2/V s were obtained for the HEMT on GaAs and Si substrate, respectively.

The same MOS-HEMT fabrication process was used for devices on GaAs and Si substrates. The device fabrication process started with mesa isolation by wet etching down to the low-temperature grown InAlAs (buffer 4). Then, a succinic acid-based etchant was used to perform the gate recess. After surface pretreatment using dilute HCl (HCl/H_2O = 1:10) for 3 min to remove the native oxide, the sample was immediately loaded into an Oxford OpAL atomic layer deposition (ALD) system for gate oxide growth. 15 nm of Al_2O_3 was deposited at 300 °C using alternating pulses of trimethylaluminum (TMA) and water precursors with Ar as carrier gas. After removal of the Al_2O_3 in the source/drain regions, Ohmic contacts were formed by electron beam evaporation of a six-layer metal system of Ni/Ge/Au/Ge/Ni/Au and lift off, followed by annealing at 280 °C for 10 min using rapid thermal annealing (RTA) in a N_2 ambient. Finally, the gate was realized with Ti/Au metallization and lift off. The cross-section view of a finished InGaAs MOS-HEMT on GaAs and Si substrates is depicted in Fig. 3.

3 Results and discussion Figure 4 shows the I_{ds}–V_{ds} characteristics of 1-μm gate-length $In_{0.53}Ga_{0.47}As$ MOS-HEMTs on GaAs and Si substrates. For the device on GaAs substrate, the maximum drain current I_{dss} is 646 mA/mm at V_{gs} = 1.4 V and V_{ds} = 2 V. The on resistance is calculated as 1026 Ω μm from the I_{ds}–V_{ds} curve. Figure 5 shows the transfer characteristics of MOS-HEMTs on GaAs and Si substrates at a drain bias of 1.5 V. For the device on GaAs substrate, an extrinsic transconductance G_m of 575 mS/mm is achieved at V_{gs} = 0.25 V and the threshold voltage V_{th} is extracted to be −0.31 V using "extrapolation in the linear region method" from the I_{ds}–V_{gs} curve. A low contact resistance of 0.13 Ω mm was achieved from the

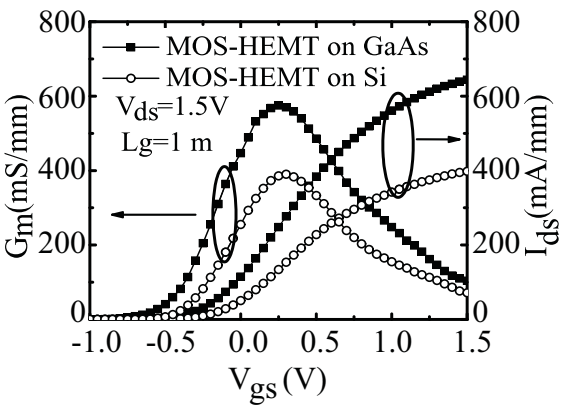

Figure 5 Transfer characteristics of InGaAs MOS-HEMTs on GaAs and Si substrates.

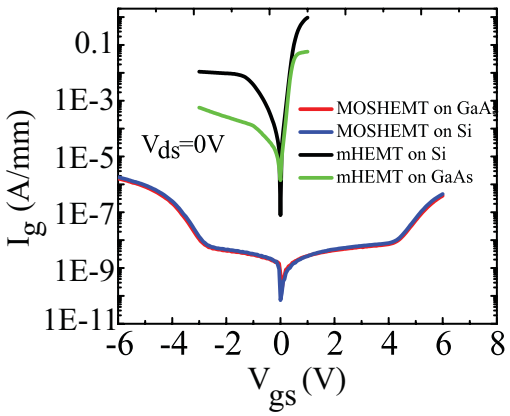

Figure 6 (online color at: www.pss-a.com) Gate current characteristics of MOS-HEMT and mHEMT on GaAs substrates.

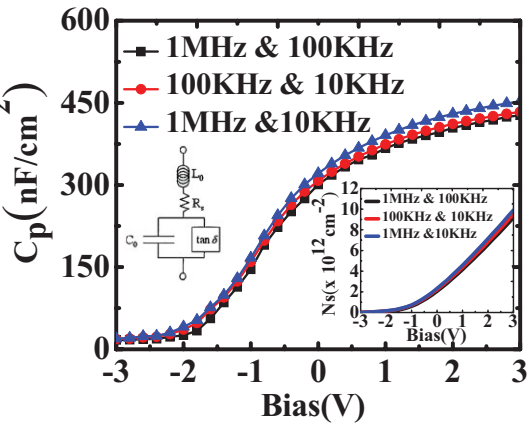

Figure 8 (online color at: www.pss-a.com) *C–V* curves after two-frequency correction measured at different pairs of frequency. The insets: four-element circuit model for the MOS capacitor and carrier density profile.

transmission line measurement (TLM). For the 1-μm gate-length MOS-HEMT on Si substrate, the device figures of merit are given as follows: $I_{dss} = 406$ mA/mm, $R_{on} = 1241\ \Omega\ \mu$m, $G_m = 390$ mS/mm, and $V_{th} = -0.17$ V. Figure 6 shows the gate current characteristics of the MOS-HEMTs and mHEMTs on GaAs and Si substrates. The MOS-HEMT on GaAs showed almost the same gate current profile as that on Si. For devices on Si substrate, the gate leakage of MOS-HEMT is six orders of magnitude lower than that of mHEMT using the same heterostructure and fabrication process, which indicates that the oxide could effectively block the gate leakage current.

To investigate the interface quality of Al_2O_3/InAlAs, ring capacitors with diameter of 200 μm were fabricated using the same gate process. Figure 7 illustrates the measured capacitance–voltage (*C–V*) response of the Al_2O_3/InAlAs capacitor. It was observed that a large frequency dispersion occurred at both bias directions, which may arise from the interface states at the oxide/InAlAs interface and parasitic components such as series resistances. Several improved two-frequency correction methods have been proposed to exclude the effect of parasitic components on the *C–V* measurement, and the four-element circuit model is commonly used for the *C–V* correction of high-κ gate dielectric [16–18]. It has been demonstrated that the frequency dispersion of *C–V* curves at high frequencies can be effectively eliminated when considering the influences of the parasitic components. Figure 8 shows the *C–V* curve after two-frequency correction with an inset of the four-element equivalent circuit model. Three pairs of frequencies were used to extract the intrinsic capacitance. It was found that the frequency dispersion at both accumulation and depletion region reduced a lot after the correction, which suggested that the original measured dispersion partly arised from the parasitic components. Another inset of Fig. 8 is the carrier concentration density profile as a function of bias voltage and frequency pairs after the two-frequency correction.

Figure 9 shows the subthreshold characteristics at drain biases of 1.5 and 0.1 V. The device on GaAs exhibits a subthreshold slope (SS) of 101 mV/dec at $V_{ds} = 1.5$ V and a

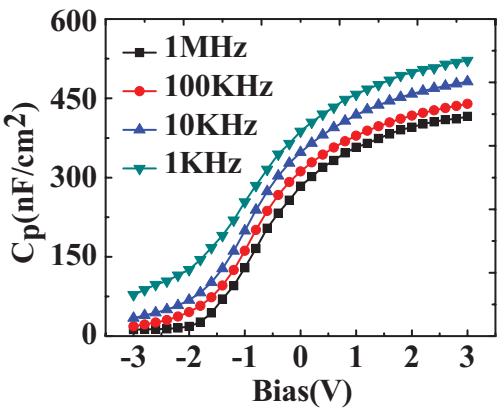

Figure 7 (online color at: www.pss-a.com) Measured multi-frequency *C–V* curve of oxide/InAlAs capacitor.

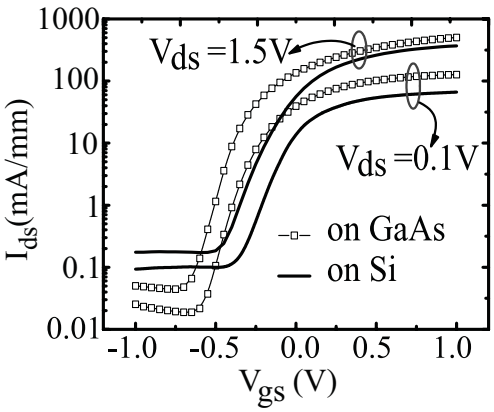

Figure 9 Subthreshold characteristics of 1-μm gate-length MOS-HEMT on GaAs and Si substrate.

drain induced barrier lowering (DIBL) of 142 mV/V. I_{on}/I_{off} ratio is around 1.0×10^4. The device on Si shows SS = 130 mV/dec, DIBL = 138 mV/V, and $I_{on}/I_{off} = 2.0 \times 10^3$. The I_{on} and I_{off} were measured at $V_{gs} = -0.9$ V and $V_{gs} = 0.9$ V for both devices. The current subthreshold characteristics are mostly limited by the thick Al_2O_3/InAlAs stack and large D_{it}. Compared to the MOS-HEMT on GaAs substrate, the device on Si shows a performance degradation due to the large lattice mismatch (8%) and thermal expansion coefficient mismatch (43%) between InP and Si, which are almost two times larger than the mismatches between InP and GaAs.

The on-state characteristics including I_{dss} and G_m of the MOS-HEMT on GaAs substrate is obviously improved [12–15]. We ascribe this to the high-quality metamorphic heterostructure grown by MOCVD and the low-temperature process. The highest temperature during the fabrication was 300 °C used in ALD process. To examine the effect of this thermal processing on the epitaxial material, hall measurements before and after oxide deposition was performed, and no degradation was found.

To further improve the device performance, the following two major aspects should be optimized. First, the oxide/InAlAs stack will be thinned to strengthen the gate modulation. The reason for choosing 15 nm for oxide thickness in this work was just to ensure a small and uniform gate leakage at this initial stage, so that we could optimize other parameters including III–V hetero-epitaxy on GaAs/Si and fabrication processes. Secondly, there is high D_{it} located in InAlAs/oxide interface, which needs to be optimized further.

4 Conclusions High-performance $In_{0.53}Ga_{0.47}As$ MOS-HEMTs on GaAs and Si substrates grown by MOCVD are reported. A low-temperature process was developed to facilitate the low thermal budget for III–V materials. Remarkable enhancement in on-state I_{dss} and G_m has been achieved for MOS-HEMT on GaAs substrates. Current device performance was analyzed and further optimization was also proposed.

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