High-Performance AlN/GaN MOSHEMTs with Regrown Ohmic Contacts by MOCVD

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Abstract

High-performance AlN/GaN metal–oxide-semiconductor heterojunction field-effect transistors (MOSHEMTs) have been fabricated with source/drain (S/D) regrowth technology by metal-organic chemical vapor deposition (MOCVD). The gate and S/D metallization were produced simultaneously employing Ti/Al/Ni/Au. Low S/D contact resistance of 0.33 Ω·mm and interface resistance less than 0.07 Ω·mm were extracted. The fabricated 550-nm gate-length device exhibits a maximum transcondutance (G_m) of 542 mS/mm and maximum drain current (I_d) of 1120 mA/mm with an on/off state current ratio up to 10^6.

1. Introduction

Excellent RF performance have already been demonstrated on both Ga-polar and N-polar GaN HEMTs, including record power-gain cut-off frequency/current-gain cut-off frequency (f_{max}/f_T) of 400/370 GHz for Ga-polar [1, 2] and f_{max}/f_T of 351/275 GHz for N-polar [3, 4]. The unceasing gate length down scaling certainly has has been the key to these rapid improvements. Nevertheless, such outstanding performances are also the results of strengthened gate electrostatic control over channel carriers as well as reduced S/D access resistance. Back barrier [5] and non-planar structures [6] have been employed to carefully increase the gate-channel capacitance, while S/D regrowth [7] has been employed to minimize the access resistance instead of using traditional high-temperature alloying process only. AlN/GaN heterostructures allows for the thinnest barrier thickness associated with high 2-dimentional electron gas (2DEG) density and reasonable mobility in HEMTs. These merits make AlN/GaN HEMTs one of the most promising candidates for ultra-scaled high-speed GaN transistors. A majority of the AlN/GaN HEMTs on Si reported were grown by molecular beam epitaxy (MBE) at low temperatures around 800°C, which helped manage stain built up due to large lattice/thermal-expansion mismatch between GaN and Si substrate. Recently, MOCVD grown AlN/GaN HEMTs on Si were reported with good DC and RF performances [8] [9] [10]. Moreover, intriguing achievements, in terms of low leakage current [11], low noise figure [12], and power amplifier extending into Ka band [13], were also demonstrated.

In this work, we present a high-performance ultra-thin barrier AlN/GaN MOSHEMTs on Si substrate with regrown n^+-GaN as the S/D contacts. Moreover, the S/D and gate metals were deposited simultaneously with Ti/Al/Ni/Au, which reduced the number of necessary process procedures. A single patterned SiO_2 step defines not only the S/D regrowth mask but also the gate region. The measured G_m is as high as 543 mS/mm despite of a relatively long channel length (L_g) of 550 nm. Using an atomic-layer-deposited (ALD) Al_2O_3 as the gate dielectric, gate leakage current was effectively limited to as low as 0.02 mA/mm.

2. Experiment

The AlN (1.5 nm)/GaN heterostructures were grown by MOCVD on a highly resistive (HR) 2-inch Si (111) substrate. The growth conditions were almost identical to that reported in Ref. [9]. The device fabrication process started with an 80-nm SiO_2 deposition by plasma enhanced chemic vapor deposition (PECVD), and then SiO_2 was patterned and wet-etch using BOE. With the,

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SiO_2 mask, the S/D region was recessed down to a depth about 70 nm by plasma dry etching. Then the patterned sample was loaded back into MOCVD chamber for a regrowth of around 54 nm n^+-GaN. The n^+-GaN consists of two layers with different Si doping concentration (Si: $2.5\times10^{19}/cm^3$ and then a highly-doped layer up to $6\times10^{19}/cm^3$). The lighter-doped GaN was used to provide a better transition to the highly-doped layer with good surface morphology. After the regrowth, the SiO_2 is stripped using BOE. A 6-nm Al_2O_3 as the gate dielectric was deposited at 300°C using TMA and H_2O as precursors in an Oxford Instrument OpAL ALD system. After the Al_2O_3 over the S/D region was locally removed, both the gate and S/D metallization were realized simultaneously with Ti/Al/Ni/Au. A cross-sectional schematic of the as-fabricated AlN/GaN MOSHEMTs is shown in Fig. 1(a). A typical scanning atomic force microscopy (AFM) image of the regrowth profile clearly shows the total regrown n^+-GaN thickness (54+70 nm) and gate length (550 nm).

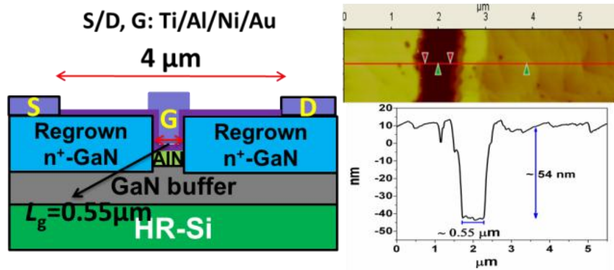

Fig. 1. Cross-sectional schematic of as-fabricated AlN/GaN MOSHEMTs, and AFM image of the gate region profile with regrown n+-GaN approximately 54 nm above the mesa.

3. Results and Discussion

The thermal stability of the non-alloyed ohmic contact was evaluated separately in another control sample with 200-nm regrown n+-GaN. Shown in Fig. 2(a) is the DC current between two metal/n^+-GaN contact pads before and after thermal annealing at 300 °C for 10 min. It was found that, in this control sample, the contact became rectifying, caused by the formation of TiN during the annealing process [14].

Therefore, in our device fabrication process, the S/D and gate metallization was arranged to be the last step to avoid any additional thermal budget. From the transmission-line method (TLM) patterns with regrown n^+-GaN channel and contacts, extracted contact resistance of 0.33 Ω·mm and sheet resistance of 165 Ω/sq were obtained.

The output characteristics of the MOSHEMTs with 550-nm channel length is shown in Fig. 2(b). Gate-source voltage (V_{gs}) was swept up from (or down toward) below threshold voltage. There is no severe current hysteresis between these two V_{gs} sweeping directions. A maximum I_d of 1120 mA/mm is obtained under V_{gs} = 1.5 V and V_{ds} = 2.5 V.

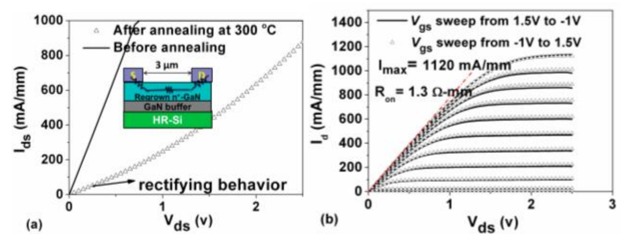

Fig. 2. (a) The monitored currents between two adjacent contact pads with 3-µm spacing on estimated 200-nm thick regrown n^+-GaN. This test was conducted on a control sample. (b) I_d-V_{ds} characteristics. The V_{gs} is swept up or down separately with the same sweeping rate, step= 0.5 V.

The device on-state resistance R_{on} is about 1.3 Ω·mm, which is extracted at V_{gs} =1.5 V in the linear operation region. The R_{on} consists of four components, including ohmic contact resistance (R_c), series resistance (R_{ac}) induced by the access n^+-GaN region, the interface resistance between n+-GaN and 2DEG channel, and the channel resistance. As the R_c and R_{ac} contribute 1.23 Ω·mm to the R_{on} based on calculation, the interface resistance should be less than 0.07 Ω·mm, which suggests high crystal quality of the regrown n+-GaN and low barrier for electron flowing across the interfaces.

Fig. 3 shows the transfer characteristics in linear and semilog scales, with V_{ds} biased at 2.5 and 0.5 V. No apparent drain induced barrier lowering (DIBL) is found by comparing the threshold voltage at different V_{ds} in Fig. 3(b). The subthreshold slope (*SS*) is estimated to be

96 mV/dec, with an observed on/off-state current ratio up to 10^6. Those ascribes to the high gate-length-to-barrier-thickness ratios (L_g/t_{bar}) as well as vertical ultra-thin barrier thickness (t_{bar}= 7.5 nm), which gives rise to a maximum G_m as large as 543 mS/mm at V_{ds} = 0.5 V. For GaN transistors on Si, such high G_m is even comparable with the record 606 mS/mm in Ref. [10] with a smaller gate length of only 130 nm. The deposited Al_2O_3 effectively suppress the gate leakage current under both reverse and forward bias. Off-state drain leakage current at V_{gs} = -1.5V was as low as 0.02 mA/mm.

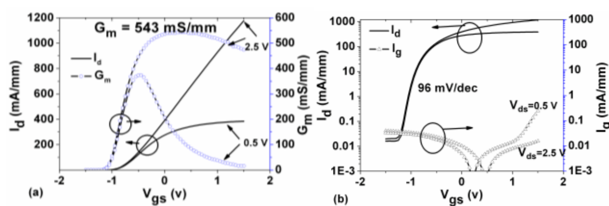

Fig. 3. Transfer characteristics of the AlN/GaN MOSHEMTs at V_{ds} = 2.5 and 0.5 V: (a) Linear scale and (b) Semilog scale along with gate diode leakage.

4. Summary

We have reported ultra-thin barrier AlN/GaN MOSHEMTs with the gate and S/D metallization produced simultaneously. The highly-doped regrown S/D facilitates the formation of low ohmic contact resistance. The unique combination of ultra-thin barrier and S/D regrowth result in I_d of 1120 mA/mm and G_m of 542 mS/mm for 550-nm gate length device. These results reflect the great promise for future performance improvement through optimization of device configuration in such heterostructures.

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