Enhancement-Mode AlN/GaN MOSHFETs on Si Substrate With Regrown Source/Drain by MOCVD

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***Abstract*—High-performance enhancement-mode (E-mode) AlN/GaN metal–oxide–semiconductor heterojunction field-effect transistors (MOSHFETs) on Si substrates have been demonstrated. Record high peak transconductance G_m of 509 mS/mm and maximum drain current I_d of 860 mA/mm were achieved for E-mode MOSHFETs with a source/drain spacing value L_{sd} of 0.7 μm. Low gate leakage current ($< 10^{-3}$ mA/mm) and improved ohmic contact resistance (0.153 $\Omega \cdot$ mm) were enabled by a combination of Al_2O_3 gate dielectric and regrown source/drain contacts. Al_2O_3 also significantly increases the 2DEG density under the channel, which is beneficial for device performance by reducing the access resistance. The on-resistance is as low as 1.63 $\Omega \cdot$ mm. The average regrowth interface resistance across the sample was estimated to be 0.056 $\Omega \cdot$ mm. The E-mode MOSHFETs exhibit a high I_{on}/I_{off} ratio up to 10^6.**

***Index Terms*—Atomic-layer-deposited (ALD) Al_2O_3, AlN/GaN, enhancement-mode (E-mode), metal–oxide–semiconductor high-electron mobility transistor (MOS HEMT).**

I. Introduction

REMARKABLE progress in GaN-based HFETs has been enabled by a combination of novel technologies such as thin AlN/InAlN barrier layers [1], [2], InGaN/AlGaN back barriers [3]–[5], lateral scaling, and ohmic contact regrowth [6], [7]. AlN, having the highest spontaneous polarization and largest band gap among all the III-nitride semiconductor materials, has been utilized as a barrier material allowing sufficiently high aspect ratio (gate length to barrier thickness) to mitigate short-channel effects associated with lateral and gate length scaling. Excellent dc and RF performance have been demonstrated for AlN/GaN HFETs on SiC substrates, including $I_d = 2.9$ A/mm [8], peak G_m of 1.63 S/mm, cutoff frequency f_T over 300 GHz [7], and unit power-gain frequency $f_{\max}$ of 400 GHz [9]. On the other hand, there still remains much to be desired for AlN/GaN HFETs on Si substrates, particularly for the enhancement mode (E-mode), in terms of achieving low-cost, high-efficiency, and simple circuit topologies. However, large tensile lattice strain in AlN makes the growth of high-performance III-nitride devices on silicon challenging.

Recently, normally off AlN/GaN HFETs on Si substrates have been fabricated by recessing the gate and source/drain metals into an *in situ* grown SiN_x cap layer [10]. However, the high potential barrier of AlN makes it difficult to form low contact resistance to the channel. In this letter, we present E-mode AlN/GaN MOSHFETs with regrown n^+ GaN source/drain regions and Al_2O_3 as gate dielectric and surface passivation layer. Atomic-layer-deposited (ALD) Al_2O_3 is of great benefit to suppress gate leakage current as a gate dielectric and increase the 2DEG density in the access region as a passivation layer [10]. No additional dry-etching process was employed at the gate or source/drain region. Due to the inferior thermal stability of the Ti/Al/Ni/Au metal contact [11], the source/drain metal deposition was the last step in our process. To characterize the dc performance of the AlN/GaN MOSHFETs and the effects of Al_2O_3 passivation, two kinds of device configuration with different L_{sd} values were fabricated. The gate length L_g and the L_{sd} value of MOS1 [see Fig. 1(a)] were set to be 1.3 and 3 μm, respectively, whereas in MOS2 [see Fig. 1(b)], both are 0.7 μm. The gate metal overlaps a part of the regrown source/drain region in MOS2. The aforementioned dimensions were confirmed by scanning electronic microscope and atomic force microscope.

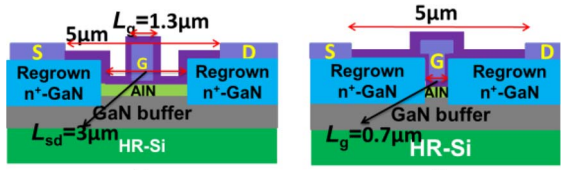

Fig. 1. Device schematic of (a) MOS1 with $L_g = 1.3$ μm and $L_{sd} = 3$ μm, and (b) MOS2 with $L_g = 0.7$ μm.

II. Materials Growth and Device Fabrication

The AlN (1.5 nm)/GaN heterostructure was grown by metal–organic chemical vapor deposition (MOCVD) on a 2-in high-resistivity ($\rho > 5000$ $\Omega \cdot$ cm) Si (111) substrate. The epitaxial structure consisted of, from bottom to top, a 40-nm AlN nucleation layer, eight periods of AlN (11 nm)/Mg:GaN (23 nm) superlattice strain relaxation interlayer, 2 cycles of GaN layer (600 nm)/low-temperature AlN (20 nm) interlayer, a 125-nm Mg-doped GaN layer, an 875-nm GaN buffer layer, and a 1.5-nm AlN barrier layer. Finally, a 1-nm GaN protective cap layer was grown. Before any surface passivation, the sheet resistance of the as-grown sample was in the order of 10^4 Ω/sq from Hall measurement results.

Before the regrowth process, a 84-nm-thick SiO_2 layer was deposited on the AlN/GaN heterostructure wafer as a regrowth mask by plasma-enhanced chemical vapor deposition (PECVD). SiO_2 was patterned using diluted HF etching solution. The source and drain regions were created using Cl_2-based dry etching to a depth around 120 nm from the sample surface. After that, the patterned sample was loaded into the MOCVD

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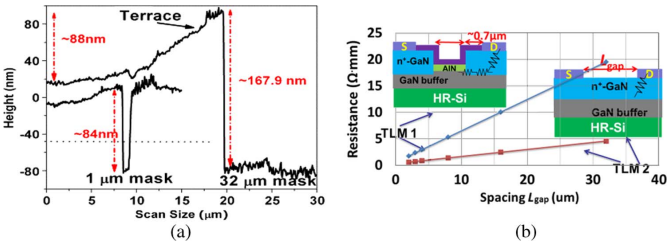

Fig. 2. (a) Regrowth profile after the removal of SiO_2 mask (mask length $=$ 1 μm and mask length $=$ 32 μm). (b) TLM results of regrown contacts on two types of TLM patterns after Al_2O_3 passivation. TLM1 (regrown n^+-GaN and n^+-GaN/AlN channel) and TLM2 (regrown n^+-GaN).

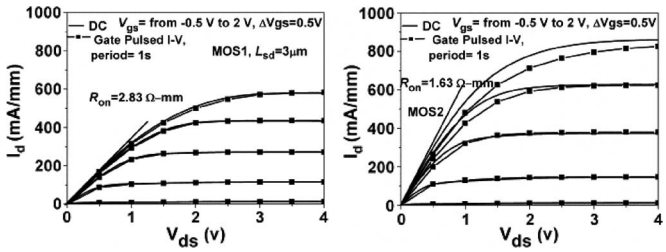

Fig. 3. DC and pulsed I_d–V_{ds} characteristics of MOS1 and MOS2. Record high $I_d = 860$ mA/mm at $V_{gs} = 2$ V for MOS2.

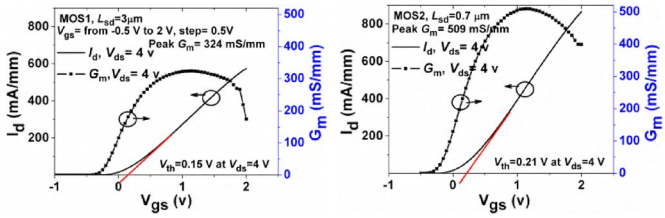

Fig. 4. I_d–V_{ds} transfer curves of MOS1 and MOS2. Record high $G_m =$ 509 mS/mm at $V_{gs} = 2$ V for MOS2.

chamber for the selective regrowth of n^+-GaN drain/source for the ohmic contact. n^+-GaN consists of two-level doped layers (Si : $2.5 \times 10^{19}/\text{cm}^3$ and a highly doped layer up to $6 \times 10^{19}/\text{cm}^3$). The lighter doped GaN was used to provide better transition to the highly doped layer with good surface morphology. The regrowth temperature was 1090 °C, and the growth rate was about 43 nm/min in the planar region. Growth occurred on both the bottom surface and the etched sidewalls. The edge effect led to a somewhat thicker regrown layer near the mask edge. The total regrown n^+-GaN thickness in the planar region is about 200 nm, which is about 80 nm higher than the mesa height. The growth rate near the side wall and mask is greatly enhanced due to the nonplanar regrowth and diffusion of species from the SiO_2 mask. This phenomenon is well known and has been also observed by other groups [12], [13]. The regrowth profiles after the removal of the SiO_2 mask are shown in Fig. 2(a). It was found that, for a small mask size of 1 μm (length) $\times$ 100 μm (width), the regrown n^+-GaN thickness near the mask edge is nearly the same as that in the planar region far away from the mask [see Fig. 2(a)]. However, in the case of a large mask size of 32 μm (length) $\times$ 100 μm (width), the terrace near the mask edge is about 88 nm higher than the area of the planar region, with a graded slope [see Fig. 2(a)]. The terrace height increases with enlarging mask area.

After the regrowth of the n^+-GaN and the removal of the SiO_2 mask, a 6-nm-thick Al_2O_3 serving as the gate dielectric was deposited at 300 °C in an ALD chamber with trimethylaluminum and H_2O precursors. The Ni/Au gate metal was defined, followed by the deposition of another 20-nm Al_2O_3 as a passivation layer. Subsequently, the sample was annealed at 400 °C for 10 min to enable gate sinking. Finally, a nonalloyed Ti/Al/Ni/Au source/drain ohmic stack was formed after the removal of Al_2O_3 in the ohmic contact regions by the HF solution. The gate length of MOS1 was defined by the gate metal length, whereas the channel length in MOS2 was defined by the distance between the n^+-GaN regrowth regions.

III. Results and Discussion

Transmission-line modeling (TLM) measurements were used to investigate the regrown GaN electrical characteristics on the samples. Fig. 2(b) shows results of the two TLM patterns in the insets (TLM1 and TLM2). After the $(6 + 20)$-nm Al_2O_3 passivation, the sheet resistance R_{sh} of TLM1 was reduced from around 10^4 to as low as 592 Ω/sq, indicating a significant increase in the channel electron density after the Al_2O_3 passivation [7], [10], [14]–[18]. The measured contact resistance R_{ct} of TLM1 was estimated to be 0.27 $\Omega \cdot$ mm by the four-probe technique. R_{ct} consists of three components, i.e., metal/n^+-GaN contact resistance, n^+-GaN access resistance (between the ohmic metal and the regrown edge), and the n^+-GaN/2DEG interface resistance. In order to extract the regrowth interface resistance between the regrown n^+-GaN and the 2DEG channel, the TLM measurement was also performed on TLM2. Results show that the metal/n^+-GaN contact resistance is around 0.153 $\Omega \cdot$ mm and the R_{sh} value of n^+-GaN is around 132 Ω/sq. The spacing between source/drain metal contacts and the regrown edge was around 0.7 μm in TLM1, the contribution of this region to R_{ct} is about 0.092 $\Omega \cdot$ mm. Based on the aforementioned analyses, it was found that the regrowth interface resistance is around 0.025 $\Omega \cdot$ mm. More TLM measurements across the sample resulted in interface resistances ranging from 0.02 to 0.1 $\Omega \cdot$ mm, with an average value of 0.056 $\Omega \cdot$ mm. This indicates a minimal barrier for the electron flow through the channel at the regrown interfaces. The aforementioned calculation ignores the influence of different terrace heights near the mask edge. Because the sheet resistance of n^+-GaN is as low as 132 Ω/sq, the error contribution by the raised terrace is very small.

Fig. 3 shows typical I_d–V_{ds} characteristics of MOS1 and MOS2. At $V_{gs} = 2$ V, the I_d value of MOS1 and MOS2 are 580 and 860 mA/mm, respectively. In order to characterize the pulse I_d–V_{ds} performance, a 500-μs pulse voltage was applied to the gate with a base voltage of -0.5 V (quiescent bias at pinchoff condition). The pulsed current shows negligible degradation in MOS1. The more severe current degradation in MOS2 is due to the higher electric field at the drain edge when compared with the case of MOS1. Fig. 4 shows the transfer characteristics of MOS1 and MOS2, exhibiting peak G_m values of 324 and 509 mS/mm at $V_{ds} = 4$ V, respectively. To our knowledge, the G_m and I_d values of MOS2 are the highest demonstrated for E-mode GaN MOSHFETs/HFETs on Si substrates.

Fig. 5 shows a comparison of recently reported G_m as a function of I_d for E-mode GaN HFETs on Si and SiC substrates [7], [10], [14]–[20]. Our work represents a new benchmark for E-mode GaN HFETs on Si substrates. By scaling down the gate length, the performance could be further improved to be comparable with that of GaN HFETs on SiC substrates. The threshold voltage V_{th} obtained by the linear extrapolation of the transfer curves are $+0.15$ V for MOS1 and $+0.21$ V for MOS2. Low on-resistance R_{on} values of 2.83 and 1.63 $\Omega \cdot$ mm

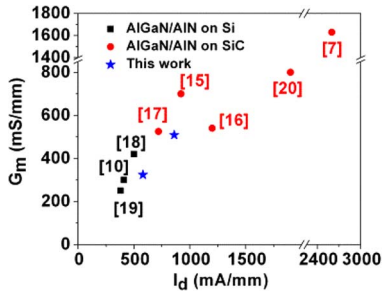

Fig. 5. Comparison of transconductance as a function of the I_d value of GaN HEMTs on Si and GaN HEMTs on SiC, including references.

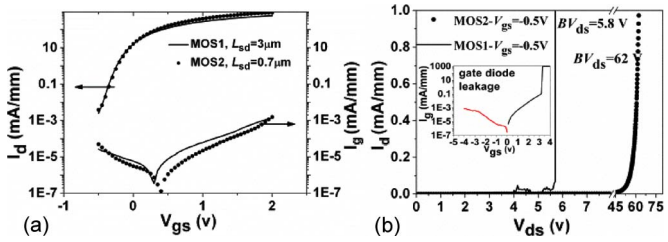

Fig. 6. (a) Log I_d–V_{ds} and log I_d–V_{ds} of both MOS1 and MOS2 for the drain bias at 4 V. (b) Breakdown voltage characteristics of MOS1 and MOS2 at $V_{gs} = -0.5$ V. (Inset) Gate diode leakage current of the controlled device with the same dimensions.

are extracted at $V_{gs} = 2$ V for MOS1 and MOS2, respectively. The difference in G_m for MOS1 and MOS2 can be explained by their different source access resistances.

Both MOS1 and MOS2 show a high ratio of $I_{\rm on}(V_{gs} = 2\ {\rm V};\ V_{ds} = 4\ {\rm V})/I_{\rm off}(V_{gs} = -0.5\ {\rm V};\ V_{ds} = 4\ {\rm V})$, around 10^6, with a low gate leakage current I_g smaller than 10^{-3} mA/mm [see Fig. 6(a)]. The three-terminal breakdown voltage of MOS1 is around 62 V under $V_{gs} = -0.5$ V [see Fig. 6(b)], which is mainly limited by the buffer leakage current. Therefore, the breakdown voltage could be significantly increased by enhancing the buffer resistivity. In the case of MOS2, the breakdown voltage is around 5.8 V due to the breakdown of the Al_2O_3 dielectric in the overlapping region between the gate and drain-regrowth n^+-GaN. The inset shows the gate diode leakage current of another controlled device with the same dimensions as MOS2, confirming that the breakdown was limited by Al_2O_3 in the overlapping region. The breakdown voltage of MOS2 could be increased by asymmetric regrowth technology with a large gate/drain spacing.

IV. Conclusion

E-mode AlN/GaN MOSHFETs on Si substrates with excellent dc performance have been demonstrated. The intriguing performance has been attributed to a combined effect of the high-quality ultrathin AlN barrier, Al_2O_3 as gate dielectric and passivation layer, and regrown source/drain contacts. Record I_d of 860 mA/mm and peak G_m of 509 mS/mm have been obtained for the E-mode device grown on the Si substrate. Further performance enhancement could be realized by the scaling down of the channel length and the increase in gate/drain spacing.

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