ETB-QW InAs MOSFET with scaled body for Improved Electrostatics

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Abstract:

This paper reports Extremely-Thin-Body (ETB) InAs quantum-well (QW) MOSFETs with improved electrostatics down to L_g = 50 nm (S =103 mV/dec, DIBL = 73 mV/V). These excellent metrics are achieved by using extremely thin body (1/3/1 nm InGaAs/InAs/InGaAs) quantum well structure with optimized layer design and a high mobility InAs channel. The ETB channel does not significantly degrade transport properties as evidenced by g_m >1.5 mS/µm and v_{inj} = 2.4 x 10^7 cm/s.

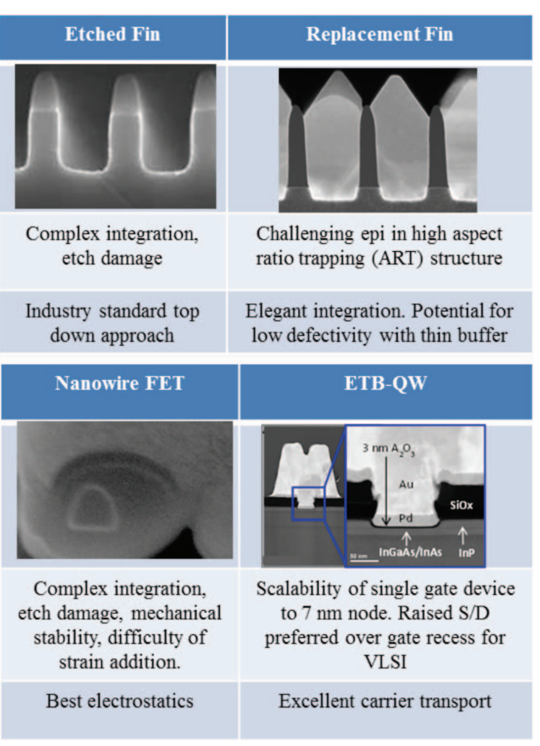
Introduction: The superior electron transport properties of III-V materials enable an attractive route to V_{dd} scaling at sub 10 nm nodes. Extremely thin (ET) architectures (finFET or planar ETB) are a choice of technology at these geometries to maintain electrostatic integrity and control short channel effects (SCE) [1-3]. However, thinning down a channel degrades carrier transport properties. For the first time, we report ETB-QW L_g = 50 nm InAs MOSFETs that exhibits excellent SCE control and favorably benchmarks an injection velocity (v_{inj}) against other III-V and Si devices. This comparison demonstrates that channel thickness can be scaled to at least 5 nm and the v_{inj} advantage over Si maintained, demonstrating a potential scaling pathway to sub 10-nm technology node.

Experimental: Table 1 as a motivation of this work compares different device architectures that can be considered for aggressively scaled III-V devices for future logic applications. The electrostatic control provided by ET-QW single gate devices may not be sufficient for sub-10nm nodes, but this architecture provides an excellent test structure to investigate the potential electron transport of multi-gate device with similar body/fin/nanowire width.

Figs. 1 sand **2** show a cross-section of the device structure and corresponding TEM images of an L_g = 50 nm device. MBE-grown 2-nm InP insulator was used to reduce access resistance and improve charge control, EOT and immunity to short channel effects as well as to improve D_{it} [3]. Extremely-Thin-Body of $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ (1/3/1nm) composite channel with inverted Si δ-doping and 5 nm $In_{0.52}Al_{0.48}As$ spacer was chosen to improve carrier transport, electron confinement in the channel and electrostatic integrity. In a calibration structure, the Hall mobility was 8,400 cm^2/V-s with $n_{s,ch}$ = 9.4 x $10^{11}/cm^2$ at 300 K. This is only about 24 % lower than the value obtained in a 10 nm thick $In_{0.7}Ga_{0.3}As$ HEMT heterostructure [4], revealing that the use of 3-nm thin InAs sub-channel was effective in mitigating a degradation of carrier transport property.

In 1D self-consistent Schrodinger-Poisson calculation for T_{QW} = 5 nm epi structure, as the channel is thinned down, the carrier concentration in the channel at the access region decreases. This causes a possible increase of R_S and R_D, as in [4]. In this work, devices with L_g from 50 nm to 250 nm are fabricated for ETB InAs QW MOSFETs. In addition, we fabricated 'FAT-FET' devices to extract long channel mobility.

Results and Discussion: Fig. 3 shows the output characteristics of ETB InAs QW MOSFET with L_g = 50



Etched Fin	Replacement Fin
Complex integration, etch damage	Challenging epi in high aspect ratio trapping (ART) structure
Industry standard top down approach	Elegant integration. Potential for low defectivity with thin buffer
Nanowire FET	**ETB-QW**
Complex integration, etch damage, mechanical stability, difficulty of strain addition.	Scalability of single gate device to 7 nm node. Raised S/D preferred over gate recess for VLSI
Best electrostatics	Excellent carrier transport

Table 1 Comparison of potential sub-10 nm III-V device architectures

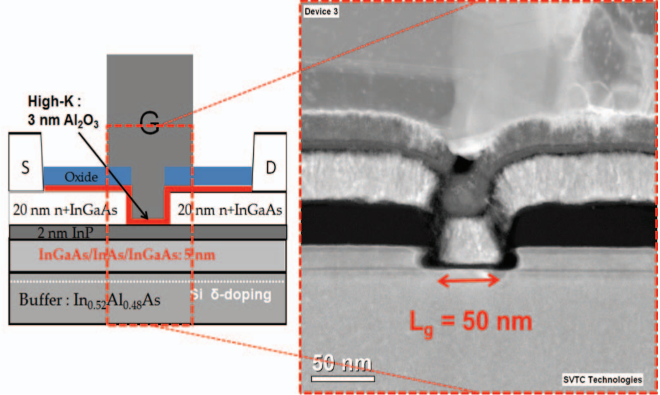


Fig. 1 and 2 Schematic of ET-QW InAs MOSFETs and TEM images for L_g = 50 nm ET-QW InAs MOSFETs with T_{QW} = 5 nm. Note that 3-nm Al_2O_3 was used as a gate insulator, together with MBE-grown 2-nm InP, leading to EOT = 2 nm.

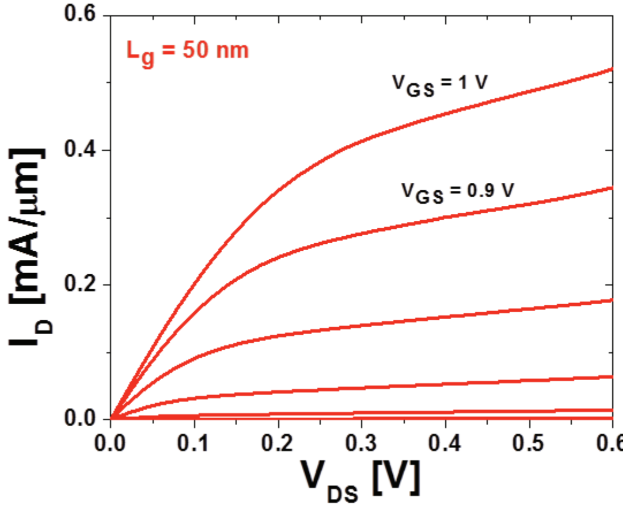


Fig. 3 Output characteristics of L_g = 50 nm ET-QW InAs MOSFETs with Al_2O_3 = 3 nm.

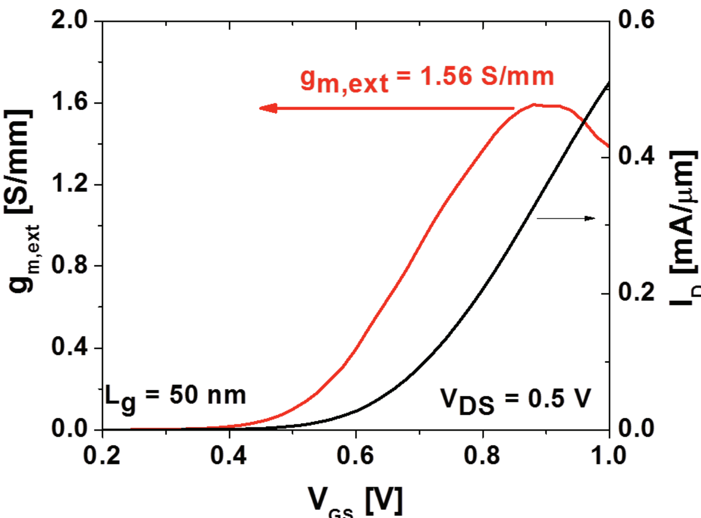


Fig. 5 Transconductance (g_m) and transfer characteristics of L_g = 50 nm ET-QW InAs MOSFETs with Al_2O_3 = 3 nm, at V_{DS} = 0.5 V.

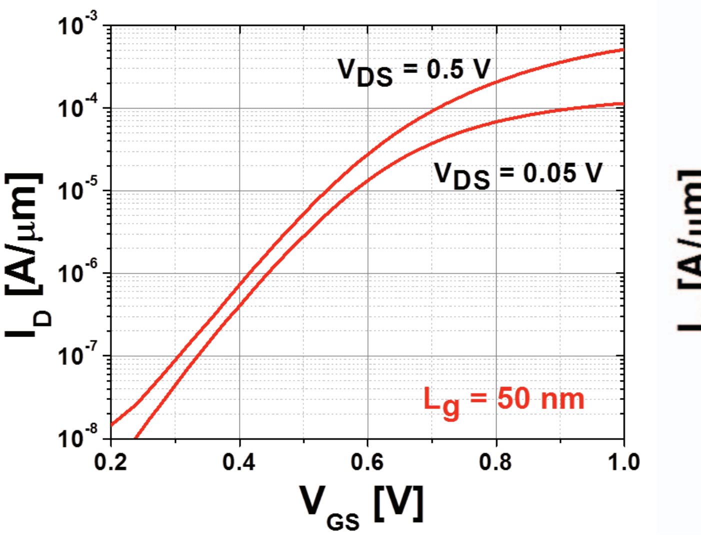


Fig. 4 Subthreshold characteristics of L_g = 50 nm ET-QW InAs MOSFETs with Al_2O_3 = 3 nm, at V_{DS} = 0.05 V and 0.5 V.

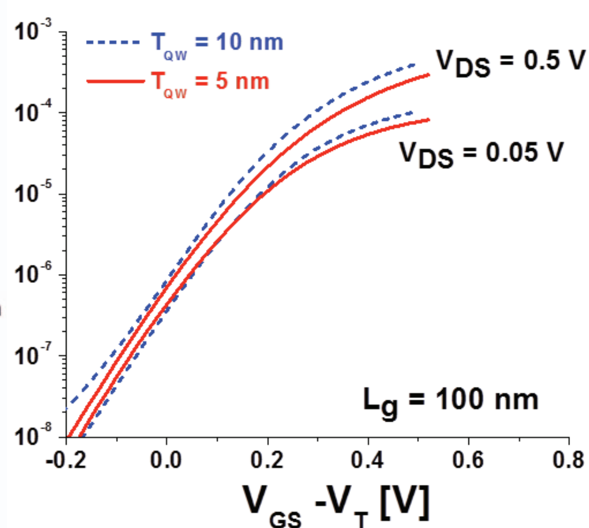


Fig. 6 Subthreshold characteristics for two types of III-V MOSFETs with T_{QW} = 5-nm (this work, red-colored) and T_{QW} = 10-nm ([4], blue-colored).

characteristics with a fairly low value of R_{ON} = 420 Ohm-um. **Fig. 4** shows the subthreshold characteristics of L_g = 50 nm InAs ET-QW MOSFET. Improved short-channel effects (SCEs) that arise from thinning down T_{QW} to 5 nm are evident in the sharp subthreshold characteristics with Subthreshold-Swing (S) = 103 mV/dec., and Drain-Induced-Barrier-Lowering (DIBL) = 73 mV/V for the 50 nm device. The device exhibits I_{ON}/I_{OFF} ratio >10^4 down to L_g = 50 nm at V_{DS} = 0.5 V. The gate leakage (I_g) is lower than 1 nA/μm at all measured bias conditions. This gives rise to an I_{OFF} = 2x10^{-8} A/μm at V_{GS} = 0.2 V and V_{DS} = 0.5 V. **Fig. 5** shows typical transconductance (g_m) characteristics of ETB-QW InAs MOSFET with L_g = 50 nm, where $g_{m,max}$ is 1.56 mS/μm at V_{DS} = 0.5 V. We compare our ETB device (T_{QW} = 5 nm) to T_{QW} = 10 nm device [4] with L_g = 100 nm. **Fig. 6** shows subthreshold characteristics for both devices at L_g = 100 nm. T_{QW} = 5 nm device shows better subthreshold swing and DIBL characteristics. However, the trade-off of the ETB device is evident in **Fig. 7,** which compares the output characteristics for both devices with L_g = 100 nm. Larger R_{ON} and lower $I_{D,sat}$ were observed in T_{QW} = 5 nm device mainly due to the lower electron density in access region plus degradation of electron transport properties. **Fig. 8** shows extracted R_{ON} as a function of L_g. T_{QW} = 5 nm devices show larger value of R_{DS} = 380 Ohm-μm than that of 323 Ohm-μm in T_{QW} = 10 nm devices. Further self-aligned gate architecture and tight gate recess process will mitigate the increase of R_S.

Figs. 9 and **10** benchmark subthreshold-swing (S) and DIBL against L_g, for state-of-the-art Si and III-V devices. The excellent electrostatics integrity and scalability of ETB-QW devices is evident, showing robust immunity to SCE. **Fig. 11** shows the transconductance as a function of

L_g including T_{QW} = 5 nm, 10 nm and other III-V MOSFETs. Better scalability was observed down to L_g = 50 nm

We have performed a rigorous extraction of the virtual-source injection velocity (v_{inj}) in ETB-QW InAs MOSFETs with T_{QW} = 5 nm and compared it with similar extractions on T_{QW} = 10 nm devices, as in [4]. **Fig. 12** shows extracted intrinsic gate capacitance (C_{gi}) and corresponding Q_{i_xo} for both devices. T_{QW} = 5 nm device shows slightly increased C_{gi} and Q_{i_xo} due to reducing physical thickness of channel which improves the charge control. With DIBL and V_T correction, we extracted the v_{inj} for both T_{QW} = 5 nm and T_{QW} = 10 devices, as shown in **Fig. 13**. Extracted v_{inj} for T_{QW} = 5 nm device exhibits 2.4 x 10^7 cm/s at L_g = 50 nm. In the long channel regime, T_{QW} = 5 nm device shows lower v_{inj} corresponding 24 % degraded Hall mobility, but as L_g decreased down to 50 nm, devices show better v_{inj} scalability, consistent with other report [5].

In correspondence with v_{inj}, we measured long channel MOSFET ('FAT-FET') having a W_g = 50 µm and L_g = 20 µm with extremely thin body InAs MOSFET to extract effective mobility. Conventional, capacitance-voltage measurement carried out for gate capacitance and charge density. **Fig. 14** shows extracted effective mobility in T_{QW} = 5 nm InAs MOSFET. Mobility was extracted by 4,200 cm^2/V-sec for ET-QW InAs MOSFET.

Conclusions: We have demonstrated ETB-QW (T_{QW} = 5 nm) InAs MOSFETs with outstanding logic characteristics, such as S = 103 mV/dec, DIBL = 73 mV/V, $I_{OFF} = 5 \times 10^{-8}$ A/µm and $g_{m,max}$ > 1.56 mS/µm at V_{DS} = 0.5 V. The extracted v_{inj} = 2.4 x 10^7 cm/s reveals that although thinning down T_{QW} degrades long channel mobility, there is less impact on velocity, indicating that when aggressively scaled the transport advantages of III-Vs can be maintained and short channel effects controlled with ET channels.

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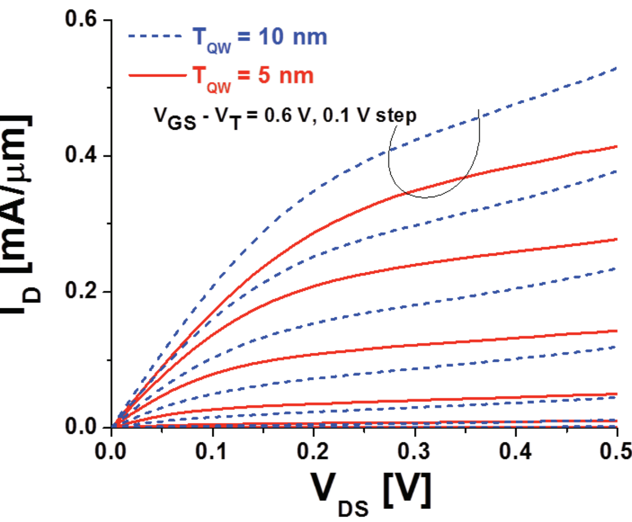

Fig. 7 Output characteristics for two types of III-V MOSFETs with T_{QW} = 5-nm (this work, red-colored) and T_{QW} = 10-nm ([4], blue-colored).

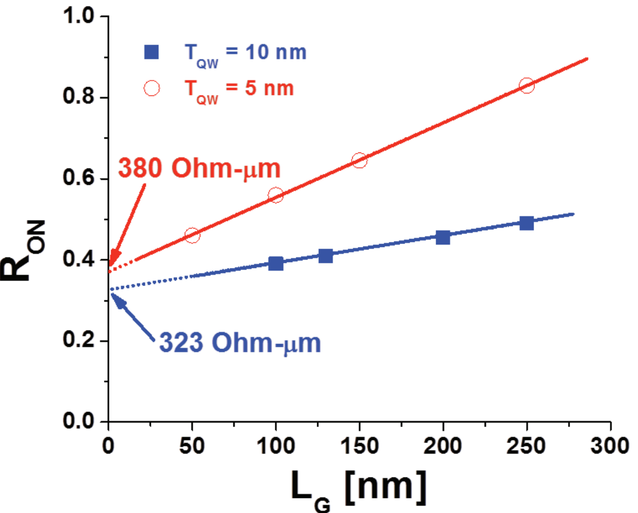

Fig. 8 R_{ON} against L_g, for two types of III-V MOSFETs with T_{QW} = 5-nm and T_{QW} = 10-nm.

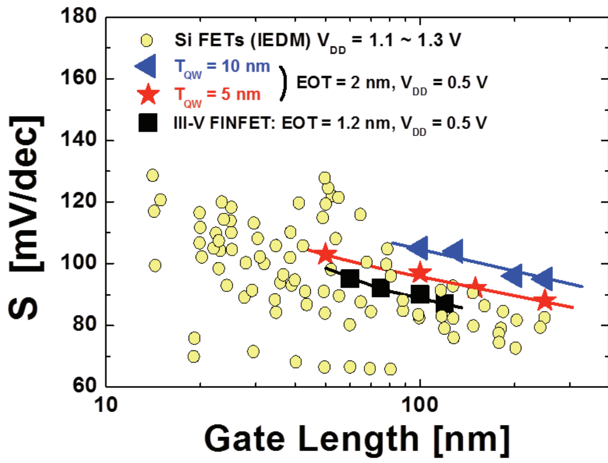

Fig. 9 Subthreshold-Swing (S) against L_g for two types of III-V MOSFETs with T_{QW} = 5-nm (this work, red-colored) and T_{QW} = 10-nm ([4], blue-colored), including other reports on III-V MOSFETs [1] with planar and non-planar architecture plus advanced Si nFETs.

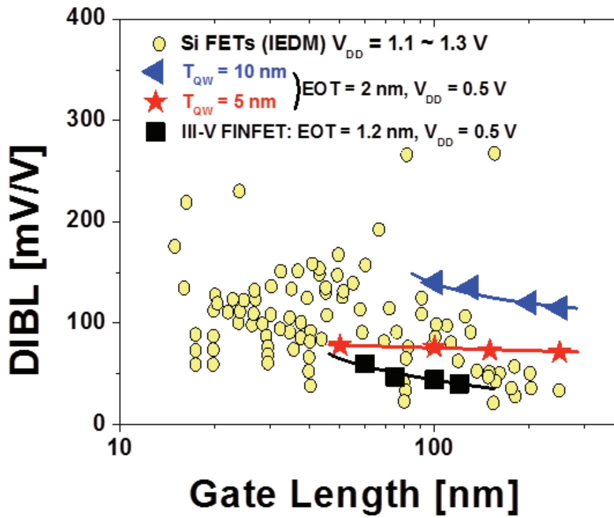

Fig. 10 DIBL against L_g for two types of III-V MOSFETs with T_{QW} = 5-nm (this work, red-colored) and T_{QW} = 10-nm ([4], blue-colored), including other reports on III-V MOSFETs [1] with planar and non-planar architecture plus advanced Si nFETs.

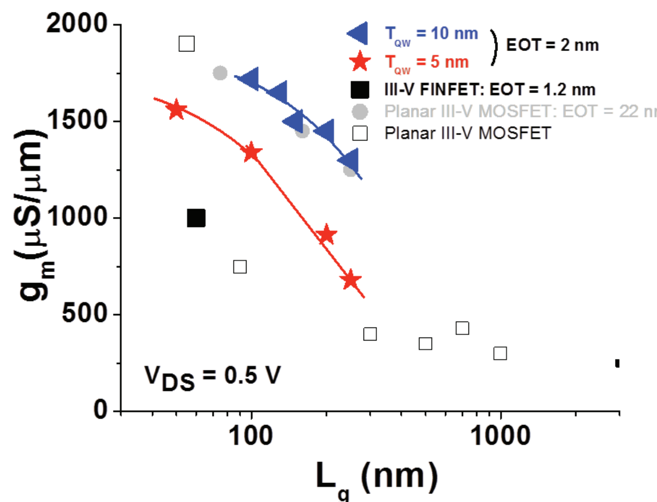

Fig. 11 g_{m_max} against L_g for two types of III-V MOSFETs with T_{QW} = 5-nm (this work, red-colored) and T_{QW} = 10-nm ([4], blue-colored), including other reports on III-V MOSFETs in the literature [6-8].

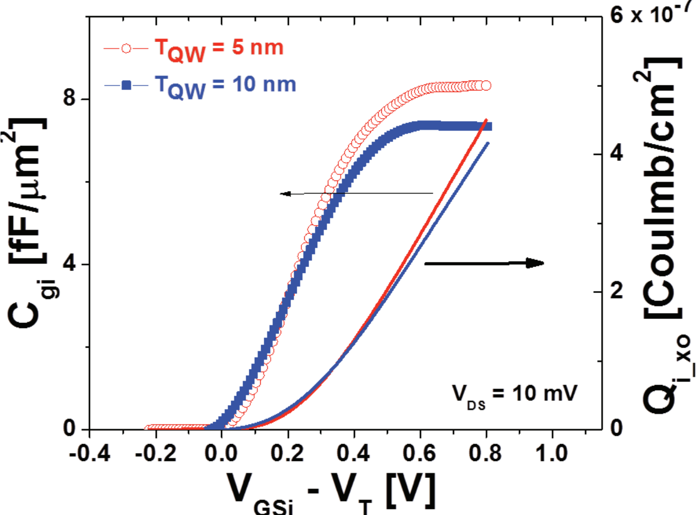

Fig. 12 Extracted intrinsic gate capacitance (C_{gi}) and charge density (Q_{i_x0}) for two types of III-V MOSFETs with T_{QW} = 5-nm (this work, red-colored) and T_{QW} = 10-nm ([4], blue-colored).

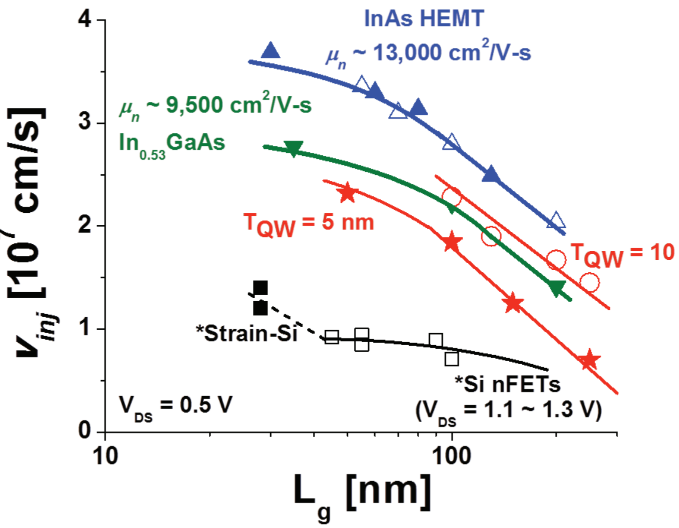

Fig. 13 Extracted virtual-source3 injection velocity (v_{inj}) against L_g, for two types of III-V MOSFETs with T_{QW} = 5-nm (this work, red-colored) and T_{QW} = 10-nm ([4], blue-colored), including other results [9].

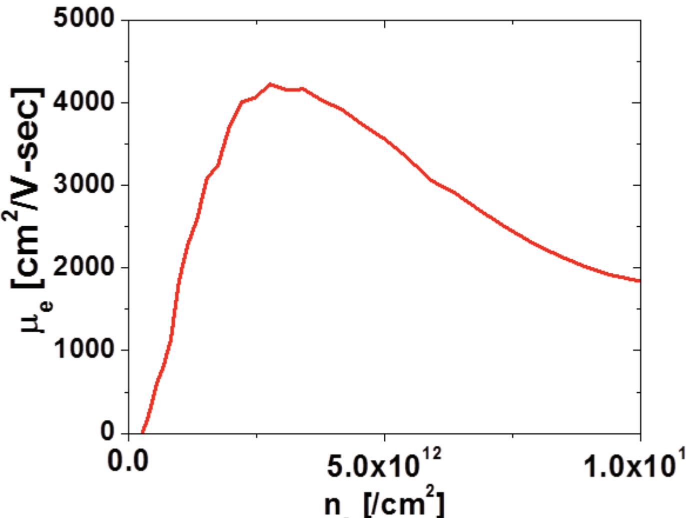

Fig. 14 Extracted low-field mobility (μ_e) against n_s from split CV measurement for FAT-FET devices.