High-Performance Inverted $In_{0.53}Ga_{0.47}As$ MOSHEMTs on a GaAs Substrate With Regrown Source/Drain by MOCVD

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***Abstract*—We report inverted-type $In_{0.51}Al_{0.49}As$/$In_{0.53}Ga_{0.47}As$ MOSHEMTs heteroepitaxially grown on GaAs substrates by metal–organic chemical vapor deposition. High 2-D electron gas Hall mobility values of 8200 $cm^2/V \cdot s$ at 300 K and 33 900 $cm^2/V \cdot s$ at 77 K have been achieved. The buried quantum-well channel design is combined with selectively regrown source/drain (S/D) using a gate-last process. A 120-nm-channel-length MOSHEMT exhibited a maximum drain current of 1884 mA/mm, peak transconductance of 1126 mS/mm at $V_{ds} = 0.5$ V, and a subthreshold slope of 135 mV/dec at $V_{ds} = 0.05$ V. With the regrown S/D, an ultralow ON-state resistance of 156 $\Omega \cdot \mu m$ was obtained.**

***Index Terms*—Effective mobility, InAlAs/InGaAs metal–oxide–semiconductor high-electron-mobility transistor (MOSHEMT), ON-state resistance, selective regrowth.**

I. Introduction

As SILICON CMOS device scaling moves into the sub-22-nm regime, severe short-channel effects and power dissipation constraints lead to huge challenges. To maintain high switching speed while lowering power consumption, III–V and Ge high-mobility-channel field-effect transistors (FETs) are gaining more and more attraction due to their excellent carrier transport properties. Among III–V compounds, InGaAs channel FETs are the most extensively investigated, and various device structures have been explored. Inversion-mode InGaAs MOSFETs have a "silicon MOS-like" device configuration, and impressive device performance has been demonstrated [1]. However, such devices generally suffer from mobility degradation due to interface roughness and Coulomb scattering, as well as remote phonon scattering from a high-k oxide [2]. Another attractive device structure is an InGaAs HEMT-like transistor featuring a buried quantum-well channel design [3], [4], in which a wide bandgap semiconductor barrier is inserted between the oxide and the channel to enhance high effective electron mobility. Apart from that, the heterostructure also offers flexibility in band structure engineering and biaxial strain incorporation.

In addition to channel design, highly doped source/drain (S/D) with concentration up to 10^{20} cm^{-3} is required in III–V MOSFETs to avoid "source starvation" [5]. In inversion-mode InGaAs MOSFETs, S/D ion implantation was commonly used. However, the peak electron density was around 1×10^{19} cm^{-3} because of the limited activation efficiency in S/D annealing. In conventional III–V HEMT structure, the S/D contact layer is on the top of its heterostructure. Therefore, the process of gate recess etching has to be used in the channel region during device fabrication. This gives rise to concerns in threshold voltage uniformity caused by variation in recess etching depth. An alternative solution is to selectively regrow S/D after gate patterning, which could significantly reduce parasitic resistance [6]–[9] and open the possibility of introducing uniaxial strain in the channel [6].

In this letter, we present inverted-type $In_{0.53}Ga_{0.47}As$ MOSHEMTs on GaAs with regrown S/D. Compared with the InP substrate, GaAs is less expensive, more robust, and available in larger wafer scale. Moreover, since GaAs is commonly used as an intermediate layer for the heteroepitaxy of InGaAs/InAlAs on Si [3], it also fosters the ultimate integration of III–V FETs on the Si platform. MOSHEMTs with channel length of 120 nm were fabricated without using critical e-beam lithography processes [10]. Detailed characterization of access resistivity in the S/D regions was carried out, and the best ON-state resistance R_{ON} has been achieved.

II. Material Growth and Device Fabrication

The inverted-type $In_{0.51}Al_{0.49}As$/$In_{0.53}Ga_{0.47}As$ metamorphic HEMT structures were grown on exact-(100)-orientated GaAs substrates using metal–organic chemical vapor deposition (MOCVD). The epitaxial structure is shown in Fig. 1(a). The InP buffer layer was grown using a two-step growth technique to accommodate the 4% lattice mismatch with the GaAs substrate. A 60-nm $In_{0.53}Ga_{0.47}As$ layer was inserted in the InP buffer for surface smoothing. The 10-nm $In_{0.53}Ga_{0.47}As$ quantum-well channel was cladded by a 10-nm $In_{0.51}Al_{0.49}As$ top barrier and a 10-nm $In_{0.51}Al_{0.49}As$ backside spacer for carrier confinement. Si delta doping was inserted below the $In_{0.51}Al_{0.49}As$ backside spacer. The 300-nm undoped $In_{0.51}Al_{0.49}As$ back barrier/buffer with high resistivity provides good electrical isolation between the device and the InP buffer, which resulted in good pinchoff characteristics. High-resolution triple-axis X-ray diffraction has been used to monitor the composition and relaxation state of the layers. A simulated band diagram with corresponding electron distribution is illustrated in Fig. 1(b). Two-dimensional electron gas

Manuscript received May 20, 2012; revised June 8, 2012; accepted June 9, 2012. Date of publication July 23, 2012; date of current version August 21, 2012. This work was supported in part by the Research Grants Council under Grant 614708 and Grant 615509 and in part by the Innovation and Technology Commission of Hong Kong Special Administrative Government under Grant ITP/015/09NP. The review of this letter was arranged by Editor J. A. del Alamo.

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Digital Object Identifier 10.1109/LED.2012.2204431

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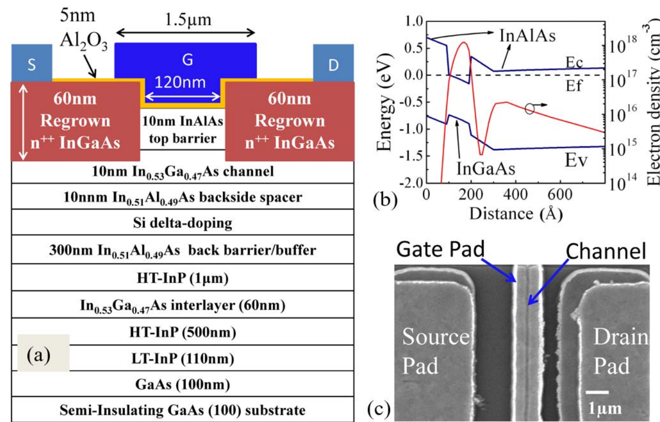

Fig. 1. (a) Cross section of the MOSHEMT (LT: low temperature; HT: high temperature. Note that the figure is not drawn to scale). (b) Simulation of the band structure and carrier distribution. (c) SEM top view of device.

(2DEG) Hall mobility values of 8200 and 33 900 $cm^2/V \cdot s$ were obtained at 300 and 77 K, respectively, with a sheet carrier density of 2×10^{12} cm^{-2}.

A gate-last process was developed to fabricate MOSHEMTs. The as-grown HEMT wafer was first covered by SiO_2 (1000 Å) as a regrowth mask. Then, the SiO_2 was patterned by buffered oxide etch (BOE), followed by S/D recess etching down to the InGaAs channel using a $H_3PO_4 : H_2O_2 : H_2O$ (3 : 1 : 50) solution. The recess etch is not critical as long as it stops somewhere within the channel. The samples were then loaded into the MOCVD reactor for S/D regrowth at 600 °C, with a growth rate of around 15 nm/min. The regrown S/D is 60-nm-thick Si-doped $In_{0.53}Ga_{0.47}As$ with electron density of 4.5×10^{19} cm^{-3} and a (111) sidewall facet, whereas the transistor gate was $\langle 110 \rangle$ oriented. Then, mesa isolation was formed by wet etching down to the InAlAs buffer, and the SiO_2 mask was removed by BOE. After surface cleaning using HCl:H_2O (1 : 10) for 2 min and $(NH_4)_2S$ passivation for 20 min, the sample was immediately loaded into an Oxford OpAL atomic layer deposition (ALD) system. *In situ* trimethylaluminum (TMA) pretreatment was performed in the ALD chamber using 20 cycles of TMA/Ar. Then, Al_2O_3 with different thickness was deposited at 300 °C using TMA and water as precursors. Post deposition annealing was conducted subsequently *in situ* in the ALD chamber at 380 °C for 30 min in an H_2 atmosphere. S/D contact holes were then opened to form nonalloyed ohmic contacts using e-beam-evaporated Ni/Ge/Au/Ge/Ni/Au and lift-off. Finally, Ti/Pt/Au gate metallization was realized. The cross-sectional schematic and the SEM top view of a finished MOSHEMT are depicted in Fig. 1(a) and (c), respectively.

III. Results and Discussion

Fig. 2 shows typical output characteristics of 120-nm-channel-length MOSHEMTs. A maximum drain current I_{dss} of 1884 mA/mm was obtained at $V_{ds} = 0.5$ V and $V_{gs} = 1$ V for device with 5-nm Al_2O_3. An ultralow R_{ON} of 156 $\Omega \cdot \mu m$ was simultaneously achieved, due to the raised highly doped S/D formed by regrowth. The access resistance components, including the contact resistance R_1 between S/D metal and regrown InGaAs, series resistance R_2 contributed from regrown InGaAs, and the regrowth interface resistance R_3 caused by interfacial defects, were extracted using transmission-line matrix

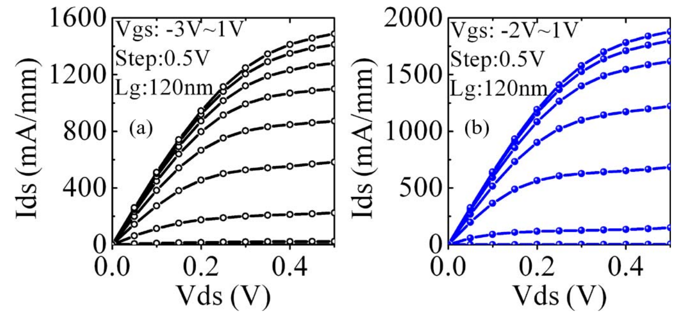

Fig. 2. Output characteristic of MOSHEMTs with (a) 8- and (b) 5-nm Al_2O_3.

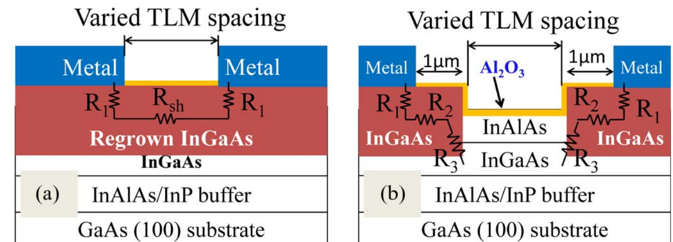

Fig. 3. Extraction of access resistance using (a) TLM-1 and (b) TLM-2.

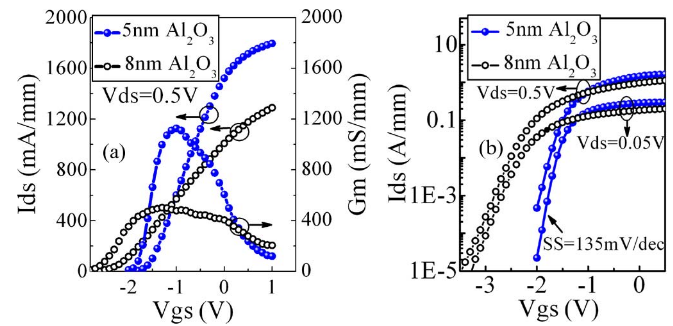

Fig. 4. (a) Transfer and (b) subthreshold curves of 120-nm MOSHEMTs.

(TLM) measurements. As illustrated in Fig. 3, the sheet resistance of regrown InGaAs $R_{sh} = 26$ $\Omega/\square$ and $R_1 = 8$ $\Omega \cdot \mu m$ were determined from TLM-1, whereas $R_2 = 26$ $\Omega \cdot \mu m$ and $R_3 = 31$ $\Omega \cdot \mu m$ were deduced from TLM-2.

Fig. 4 compares the transfer and subthreshold characteristics of MOSHEMTs. The shift of threshold voltage from -2.3 to -1.6 V in Fig. 4(a) is a result of the scaling of equivalent oxide thickness (EOT) of a composite Al_2O_3/InAlAs gate stack from 45 to 35 Å, as determined from C–V measurement. The scaling down of EOT has enhanced gate control over the channel, leading to improved peak extrinsic transconductance Gm_{max} to 1126 mS/mm and reduced subthreshold slope (SS) at $V_{ds} = 50$ mV from 256 (SS = 318 mV/dec at $V_{ds} = 0.5$ V) to 135 mV/dec (SS = 182 mV/dec at $V_{ds} = 0.5$ V). The drain-induced barrier lowering was found to decrease from 400 to 333 mV/V. For comparison, 1-μm-channel-length MOSHEMTs with a 5-nm oxide were also fabricated, and a I_{dss} of 1070 mA/mm, Gm_{max} of 542 mS/mm at $V_{ds} = 0.5$ V, and R_{ON} of 216 $\Omega \cdot \mu m$ were obtained.

Effective mobility μ_{eff} was extracted as a function of channel electron density, using a combination of C–V and I–V measurements [4]. Specifically, the channel carrier density was determined from the C–V measurement of a 160-μm-diameter ring capacitor at 1 MHz, whereas drain conductance was obtained from the I–V curve at $V_{ds} = 50$ mV of a 1-μm-channel-length MOSHEMT. As shown in Fig. 5, a high peak μ_{eff}

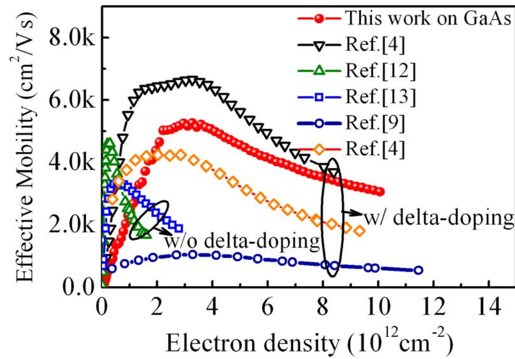

Fig. 5. Comparison of effective mobility in this letter with those on InP.

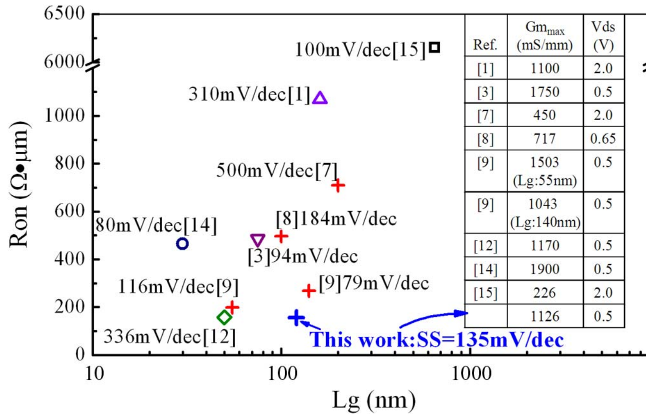

Fig. 6. Benchmarking of InGaAs FETs: □ MOSHEMT on GaAs, ○ HEMT on InP, △ inversion mode MOSFET on InP, ◇ surface channel MOSFET on InP, ▽ buried channel MOSFET on Si, +MOS devices with regrown S/D (note that SS values are labeled near the symbols).

of 5260 $cm^2/V \cdot s$ was obtained. Previous studies found that the mobility of a buried InGaAs quantum well is strongly influenced by the barrier thickness and remote scattering from the high-k/III–V interface [4], [11]. Thus, the high $\mu_{\rm eff}$ in our current device structure can be ascribed to the relatively thick InAlAs top barrier, which provides good carrier confinement and, more importantly, decreases the proximity of 2DEG to the Al_2O_3/InAlAs interface. Further scaling down of the barrier thickness is expected to lower effective channel mobility. Fig. 5 also includes the $\mu_{\rm eff}$ of the reported $In_{0.53}Ga_{0.47}As$ quantum-well channel MOSFETs on InP substrates for comparison. One notable feature for devices with delta doping is that the $\mu_{\rm eff}$ could sustain at a wide range of carrier density, whereas the $\mu_{\rm eff}$ decays rapidly after the peak value in those without delta doping. Numerical simulations have revealed that this behavior arises from the carrier and vertical electric field distributions [4].

Earlier related work, including InGaAs HEMTs [14] and MOSHEMTs [15], inversion-mode MOSFETs [1], buried-channel [3] and surface-channel [12] MOSFETs, as well as MOSFETs with regrown S/D [7]–[9] are benchmarked in Fig. 6. The device presented in this letter exhibits outstanding regrowth quality, the lowest $R_{\rm ON}$ (same as that of a 50-nm MOSFET in [12]), excellent $Gm_{\max}$ at low V_{ds} bias and a reasonably low SS. These results indicate promising characteristics of combining III–V quantum-well channel with regrown S/D, as well as heteroepitaxy of III–V transistor by MOCVD on GaAs for mass production.

IV. Conclusion

Metamorphic inverted $In_{0.53}Ga_{0.47}As$ MOSHEMT grown on GaAs substrates by MOCVD with peak effective mobility of 5260 $cm^2/V \cdot s$ was demonstrated. S/D regrowth was employed to lower parasitic resistance. An I_{dss} of 1.884 A/mm, with an ultralow $R_{\rm ON}$ of 156 $\Omega \cdot \mu$m has been achieved for 120-nm MOSHEMTs.

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