Growth of butt-coupled p-i-n InGaAs waveguide photodetectors by MOCVD

Yu Geng, Shaoqi Feng, Andrew W. Poon, and Kei May Lau
Dept of Electronic and Computer Engineering,
Hong Kong Univ. of Science & Technology, Clear Water Bay, Kowloon, Hong Kong
Tel: +852-2358-7049, Fax: +852-2358-1485, Email: ygeng@ust.hk

The growth of high-performance III-V devices directly on Si substrates by MOCVD is a promising solution for integration of III-V electronics and photonics on a silicon platform. However, the growth of high quality epilayers lattice-matched to InP on Si is challenging because of the large lattice mismatch and formation of anti-phase domains. Good crystalline, strain-free and smooth GaAs layers on silicon substrates can serve as a template for InP growth [1]. Our group has reported vertical p-i-n InGaAs photodetectors on Si using this approach [2]. In order to obtain higher performance, a thinner active region is required to shorten the carrier transit time, but it will lead to a lower efficiency. This inherent bandwidth-efficiency limitation can be overcome by the butt-coupled waveguide-photodiode (BC-WGPD) design as high efficiency and short carrier transit times can be achieved simultaneously [3].

In this work, p-i-n InGaAs BC-WGPD lattice-matched to InP grown on a Si substrate was demonstrated. WGPD was selectively grown inside 0.5mm × 1mm Si wells of 3μm deep, surrounded by SiO/SiN waveguide/SiO mask. The SiN waveguide was 0.4μm thick and 1μm wide with one end at the edge of the well for light coupling into the WGPD fabricated at the edge of the well. The patterned wafer was cleaned by NH_4OH:H_2O_2:H_2O boiling solution followed by a HF dip. Selective growth on the patterned Si substrates was performed in an Aixtron AIX-200/4 MOCVD system. First the sample was pre-heated at 810 ℃ for 30mins while AsH_3 was introduced at the end of annealing. Then the GaAs template was grown using AsH_3 and TEGa with a four-step growth technique. After a 10-nm GaAs nucleation layer which was first deposited at 400 ℃ with a V/III ratio of 100 [4], high temperature (HT) GaAs was grown. Instead of growing at 630 ℃ in our previous work [1], 540 ℃ and 570 ℃ smoothing layers and 600 ℃ high quality layer were grown with AsH_3 flow rate of 1800μmol/min and TEGa of 17μmol/min. The 540 ℃ smoothing layer was about 200nm thick and was crucial to eliminate dislocation induced pits. The 570 ℃ smoothing layer was about 600nm thick with good surface and crystal quality. After the smoothing layers, the temperature was ramped up to 600 ℃ to grow the high quality GaAs layer about 500nm thick. The III and V source flow rate of the HT layers was set to about 1/3 of that for non-patterned growth to compensate the enhanced growth rate at the edge due to severe loading effect. The Root-Mean-Square (RMS) of the GaAs template surface roughness at the edge of the well is 1nm (10μm × 10μm scan) by Atomic Force Microscopy (AFM). Finally, InP buffer was grown which included a thin InP nucleation layer deposited at 430 ℃ and HT InP at 610 ℃. The RMS of the InP buffer at the edge of the well is 6nm (10μm × 10μm) by AFM.

The WGPD p-i-n structure was grown on the InP/GaAs buffer, with 100nm p+ InGaAs, 700nm undoped InGaAs and 100nm n+ InP layers. The WGPD was fabricated at the edge of the well and the light is coupled from SiN waveguide to the edge of the InGaAs absorption layer of the WGPD instead of top illumination as in ref. 2. The InGaAs absorption layer is relatively thick at this initial stage for easy coupling and we will reduce it for speed in the future. Butt-coupled rectangular devices with area of 100μm^2 (10μm × 10μm) were fabricated. The process of device fabrication was the same as that introduced in ref.2. Dark current of 20nA, corresponding to a current density of 20mA/cm^2 at a reverse bias of -1V was obtained. This is comparable with high-performance Ge/Si photodetectors [5,6]. RF performance of the devices is being investigated.

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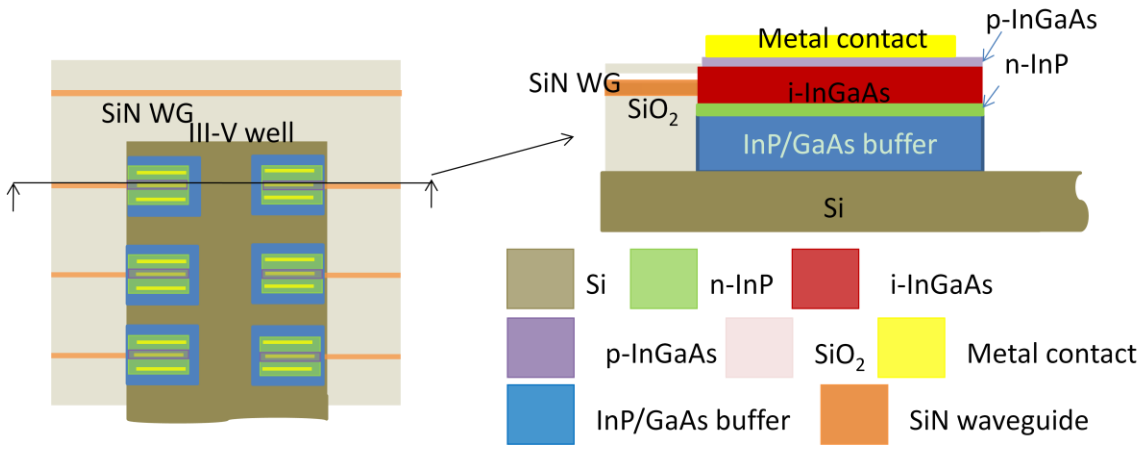

Fig.1. Schematic diagram of part of the BC-WGPD on patterned Si substrate: (a) top view; (b) cross sectional view

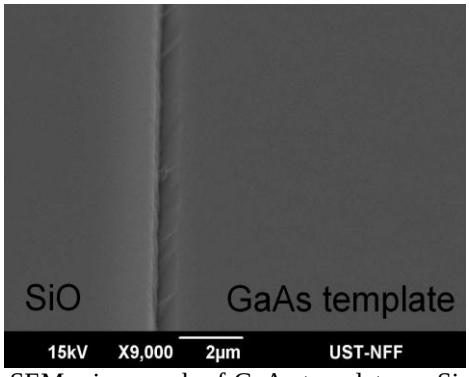

Fig. 2. SEM micrograph of GaAs template on Si (RMS = 1nm)

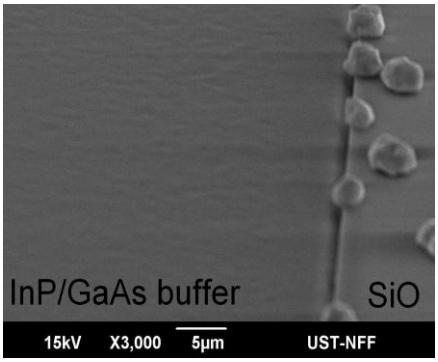

Fig.3. SEM micrograph of InP buffer on GaAs template (RMS = 6nm)

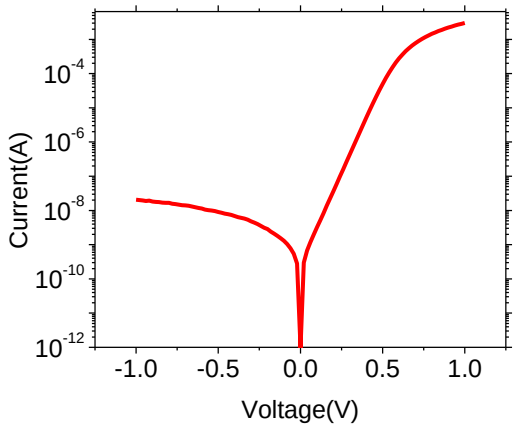

Fig.4 Dark current of the 100μm^2 device