# Epitaxial III-V-on-silicon waveguide butt-coupled photodetectors

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We report silicon waveguide butt-coupled p-i-n InGaAs photodetectors epitaxially grown on silicon-on-insulator substrates by metalorganic chemical vapor deposition. The InGaAs absorption layer that is lattice-matched to InP is selectively grown on patterned SOI substrates, employing metamorphic growth of GaAs and InP buffer layers. We measure a dark current of 2.5 μA and a responsivity of 0.17 A/W at 1550 nm wavelength upon −1 V bias voltage, with a 20 μm × 20 μm InGaAs photodetector area. This device exhibits a 3 dB bandwidth of 9 GHz upon −4 V bias voltage. We demonstrate an open-eye diagram at 10 Gb/s data rate upon −4 V bias voltage. © 2012 Optical Society of America

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Silicon photonics has been widely investigated over the past few years as one promising technology platform for on-chip optical interconnection applications. However, silicon (Si) is inefficient in light emission and essentially transparent at 1550 nm telecommunications wavelengths due to its indirect energy band structure. In order to address these shortcomings, two hybrid-integrated silicon semiconductor platforms have been studied, including germanium (Ge)-on-Si [1–3] and III-V-on-Si [4,5]. Although electrically pumped Ge-on-Si lasers have been demonstrated recently [3], the technology is still in its infancy compared to the more mature III-V counterpart. While hybrid III-V-on-Si platform by wafer bonding [4,5] has been investigated by several groups, the stringent requirements for wafer bonding and the typical size-mismatch between a Si wafer and an III-V wafer render the bonding techniques unfavorable for industrial adoption.

In comparison to the bonding techniques, epitaxially grown III-V-on-Si potentially offers a more direct wafer-level solution for low-cost mass production. Chen *et al.* have developed III-V nanoneedle lasers grown on Si substrates by metalorganic chemical vapor deposition (MOCVD) [6]. Recently, we demonstrated high-speed normal-incidence p-i-n InGaAs photodetectors epitaxially grown on Si substrates by MOCVD [7].

In this Letter, we demonstrate epitaxial III-V-on-Si waveguide butt-coupled photodetectors selectively grown on patterned silicon-on-insulator (SOI) substrates by MOCVD. The waveguide butt-coupled photodetector comprises (i) a submicrometer-sized silicon single-mode waveguide for input butt-coupling and (ii) the III-V-on-Si p-i-n photodetector region, as shown in Fig. 1(a). The light output from the silicon waveguide butt-couples to the InGaAs absorption layer. The photo-generated electrons and holes are collected by the vertical p-i-n diode, which is selectively grown by MOCVD in an III-V well. The III-V well contains an area of single-crystalline silicon layer surrounded by patterned silicon dioxide ($SiO_2$) sidewalls for the selective area growth.

The silicon waveguides are fabricated on a 4 inch (100 mm)-oriented SOI wafer, with a 0.25 μm-thick silicon device layer on a 3 μm-thick buried-oxide (BOX) layer. The silicon waveguides are patterned using i-line (365 nm) projection photolithography followed by $CF_4$-based plasma etching process. The silicon channel waveguides are designed to be 500 nm wide and 250 nm thick. A low-temperature oxide (LTO) layer of 2 μm thick is deposited on the top as an upper cladding for the waveguides and also as a protective layer for the selective area III-V material growth. The well spanning an area of 5 mm × 15 mm and surrounded by 5 μm-thick $SiO_2$ (BOX + LTO) are opened by removing the oxide using dry etching followed by wet etching in order to obtain a smooth silicon surface after the etching process for the MOCVD growth.

Epitaxial layers are grown in an AIXTRON 200/4 MOCVD system. In order to alleviate the 8% lattice mismatch between InP and Si, GaAs and InP buffer layers are grown on the patterned SOI substrate. The rms roughness of the GaAs buffer and the InP buffer at the edge are 1 nm and 6 nm, respectively, according to atomic force microscopy in a 10 μm × 10 μm area. The p-i-n diode structure is grown on the InP/GaAs buffer. The Fig. 1(a)

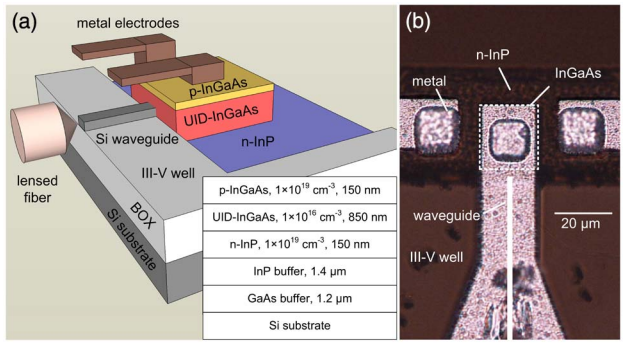


Fig. 1. (Color online) (a) Schematic of the epitaxial III-V-on-Si waveguide butt-coupled photodetector. Inset: the layered structure with the dopant concentrations and the layer thicknesses of the vertical p-i-n diode on buffer layers. (b) Top-view optical micrograph of the fabricated photodetector. The white dashed-line box indicates the 20 μm × 20 μm InGaAs photodetector area. The bold white vertical line indicates the waveguide underneath the metal pad.

 

inset depicts the layered structure. The total buffer layer thickness is about 2.6 μm in order to obtain good vertical alignment between the silicon waveguide and the unintentionally doped (UID)-InGaAs absorption layer of 850 nm thick.

We pattern the p-i-n diode structure using i-line (365 nm) contact photolithography with 1 μm resolution. The alignment error between the projection photolithography for the silicon waveguide and the contact photolithography for the diode is about 1 μm. The fabrication process of the vertical p-i-n diode using wet etching is similar to that of our previous demonstrated normal-incidence photodetectors [7]. Figure 1(b) shows an optical micrograph of the fabricated photodetector with a 20 μm × 20 μm InGaAs photodetector area.

We measure the photocurrent by coupling the TE-polarized (E-field//the chip) 1550 nm light to the silicon waveguide using a single-mode polarization-maintaining lensed fiber. The fiber-to-waveguide coupling loss was 14.7 dB, and the waveguide propagation loss was 15 dB/cm on separate chips without photodetectors, and thus we estimated the coupled input optical power at the end of the waveguide before the photodetector.

Figure 2(a) shows the measured dark current and total current upon the estimated optical power of 240 μW at 1550 nm at the butt-coupled waveguide end, within a bias voltage range of −5 to 1 V. We estimate the series resistance to be 100 Ω. The dark current upon −1 V bias voltage is 2.5 μA, which is considerably higher than that reported of the III-V-on-Si photodetectors using wafer-bonding techniques [4,5]. The measured dark current corresponds to a dark current density of 625 mA/cm$^2$, which is also higher than that of our previous demonstrated normal-incidence photodetectors [7]. The actual mechanism for the large dark current still requires further studies.

Figure 2(b) shows the measured photocurrent as a function of the estimated coupled optical power upon various bias voltages. The inset shows the zoom-in view upon low coupled powers. We measure the responsivity upon low coupled powers as 0.17 and 0.22 A/W under a reverse bias of 1 and 4 V, respectively. We measure the 1 dB saturation power upon −1 V bias voltage as 4.25 mW, which is comparable to that reported by the III-V-on-Si photodetectors using wafer-bonding techniques [4].

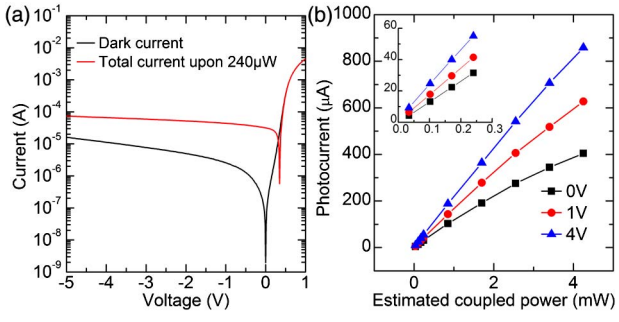


Fig. 2. (Color online) (a) Measured dark current and total current upon the estimated optical power of 240 μW at 1550 nm at the butt-coupled waveguide end as a function of bias voltages. (b) Measured photocurrent as a function of the estimated coupled input power upon various bias voltages. Inset: zoom-in view of the curves under low coupled input power.

We attribute the relatively low responsivity to the light coupling loss between the silicon waveguide output end face and the InGaAs absorption layer end face. Due to the selective area growth at the edge of the III-V wells, a gap spacing of around 2 μm wide exists between the silicon waveguide end face and the sloped InGaAs absorption layer end face, as shown in Figs. 3(a) and 3(b). The slope angle ranges from ~45° to ~60°. The gap at the end of the growth process is filled with an as-grown III-V byproduct, which will be removed by wet etching during the fabrication and later on filled with polybenzobisoxazole (PBO) with a refractive index of 1.6.

The optical beam outcoupling from the submicrometer-sized waveguide diffracts and rapidly expands in the PBO-filled gap. The Fig. 3(c) inset shows the calculated (according to the beam-propagation method) expanded optical intensity pattern in PBO projected on the InGaAs end face. Taking into account the optical beam reflection at normal incidence at the Si waveguide-PBO interface and at an oblique incidence (assuming 45° incidence angle) at the sloped PBO-InGaAs interface, we estimate the power-coupling efficiency between the silicon waveguide and the InGaAs absorption layer to be around 30% at a 2 μm gap spacing. Figure 3(c) shows the calculated power-coupling efficiency as a function of the gap separation. In order to improve the responsivity, we may in the future narrow the gap separation and make the InGaAs absorption layer end face more vertical by optimizing the metamorphic growth.

We measure the radio frequency (RF) response by using a 20 GHz vector network analyzer. The RF signal is applied to a 30 GHz $LiNbO_3$ modulator, and the modulated optical signal is coupled to the photodetector. We use a 40 GHz RF probe to measure the photodetector response. The frequency response is calibrated using a commercial 30 GHz photodetector. Figure 4(a) shows the measured frequency responses upon various reverse-bias voltages. The frequency responses are normalized to the response at 10 MHz. The bandwidth increases with increasing bias voltage until it saturates at a reverse bias of 4 V. The 3 dB bandwidths upon −1 and −4 V bias voltages are 2 and 9 GHz, respectively.

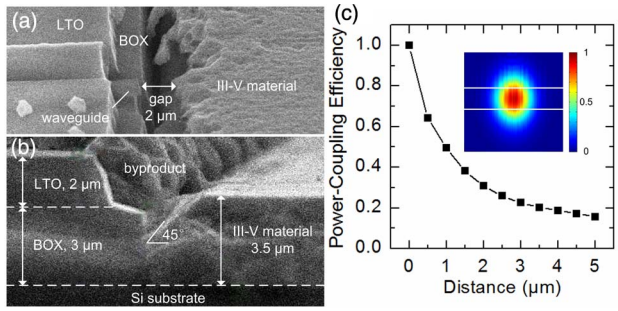


Fig. 3. (Color online) (a) Top-view and (b) cross-sectional view scanning electron microscope pictures of the as-grown sample. (c) Calculated power-coupling efficiency between the silicon waveguide and the InGaAs absorption layer as a function of the gap separation. Inset: Calculated expanded optical intensity pattern at a distance of 2 μm away from the silicon waveguide end. The two white lines depict the InGaAs absorption layer.

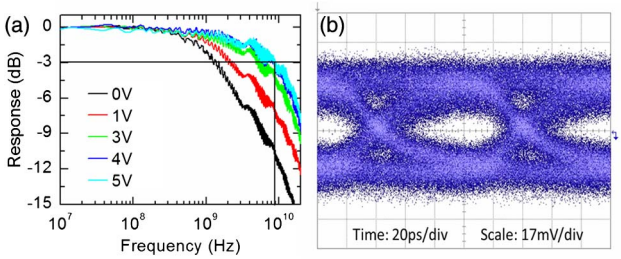


Fig. 4. (Color online) (a) Measured frequency responses upon a reverse-bias voltage ranging from 0 to 5 V and (b) measured eye diagram at 10 Gb/s data rate upon –4 V bias voltage.

The 3 dB bandwidth of the photodetector is mainly determined by the carrier transit time in the InGaAs absorption layer and the resistance-capacitance (RC) time constant of the device. Given the 850 nm-thick InGaAs absorption layer, and the hole and electron saturation velocities under a high electric field of ~50 kV/cm upon –5 V bias [8], we calculate the transit-time-limited bandwidth to be 28 GHz. We therefore believe that the measured device bandwidth is limited by the junction capacitance and the parasitic capacitance, which we estimate to be 30 and 21 fF, respectively, according to an equivalent circuit model [9]. Both the InGaAs photodetector area giving the junction capacitance and the metal electrode size giving the parasitic capacitance need to be shrunk to attain a wider bandwidth.

We measure the non-return-to-zero eye pattern using an 80 GHz oscilloscope. The RF signal from a pseudo-random bit sequence generator with a $2^{31}-1$ pattern length is amplified with a 40 GHz modulator driver and is employed to modulate the 1550 nm light through the modulator. The laser source is amplified through an erbium-doped fiber amplifier (EDFA) and the amplified spontaneous emission (ASE) noise is partially removed by an optical tunable filter. The photodetector output is amplified by using a low-noise amplifier. We observe an open eye at 10 Gb/s data rate upon –4 V bias voltage, as shown in Fig. 4(b). We attribute the noise in the eye diagram to the remaining EDFA ASE noise and the intrinsic noise of the electrical amplifier and the oscilloscope.

Table 1 summarizes the device performances of photodetectors on Si substrates demonstrated by various technology platforms. The III-V-on-Si photodetectors by epitaxial growth shown in our previous work [7] and this work exhibit larger dark current density than either Ge-on-Si growth [1] or III-V-on-Si bonding [5] photodetectors. The epitaxial growth of III-V materials on patterned SOI substrates is only in its infancy and needs to be further improved. In order to attain comparable bandwidth to Ge photodetectors, the device area also needs to be reduced by developing the dry etching process for the III-V materials.

In conclusion, we have selectively grown epitaxial III-V layers on patterned SOI substrates and fabricated silicon waveguide butt-coupled III-V-on-Si photodetectors.

**Table 1. Comparison Among Photodetectors on Si Substrates by Various Technology Platforms[a]**

| | Res. A/W | DC nA | DC Dens. mA/cm$^2$ | BW GHz | Area μm$^2$ |
|---|---|---|---|---|---|
| Ge growth [1] | 0.8 | 3 | 40 | 45 | 5 |
| Ge growth [2] | 0.8 | 4000 | 80,000 | >50 | 5 |
| III-V bonding [5] | 0.45 | 1.6 | 3 | 33 | 50 |
| III-V growth [7] | 0.57 | 200 | 64 | 10 | 314 |
| This work | 0.22 | 2500 | 625 | 9 | 400 |

[a]Res., responsivity; DC, dark current; DC Dens., dark current density; BW, 3 dB bandwidth.

The devices demonstrated promising performances for on-chip optical interconnection applications. The developed epitaxial III-V-on-Si technology with silicon waveguide integration can be naturally extended into integration with more sophisticated silicon photonic devices. However, the holy grail of integration with complementary metal–oxide–semiconductor electronics in the long term involves thermal budget and contamination issues that need to be further studied.

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