# High-Speed Normal-Incidence p-i-n InGaAs Photodetectors Grown on Silicon Substrates by MOCVD

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***Abstract*— High-speed normal-incidence p-i-n InGaAs photodetectors epitaxially grown on silicon substrates by metal–organic chemical vapor deposition has been demonstrated. The InGaAs active layer lattice-matched to InP was successfully grown on Si substrates employing metamorphic growth of InP and GaAs buffers with a two-step growth technique, in addition to cyclic thermal annealing and strain-balancing layer stacks. Circular devices with diameters ranging from 20 to 60 $\mu$m were fabricated. Dark current diminished and 3-dB bandwidth increased with a reduction of the device area. A dark current of 0.2 $\mu$A and a responsivity of 0.5 A/W at 1550 nm were measured at −1 V for a device 20 $\mu$m in diameter. This device exhibited an optical 3-dB bandwidth of 10 GHz at −5 V. An open eye diagram at 10 Gb/s at a low reverse bias of 1 V was also demonstrated.**

***Index Terms*— InGaAs photodetectors, metal–organic chemical vapor deposition (MOCVD), metamorphic technology, Si substrates.**

## I. Introduction

INTEGRATION of III–V based electronics and photonics onto the same silicon substrate has been widely investigated for various applications such as differential amplifiers [1] and optical interconnections [2]. In these applications, either epitaxial growth of III–V on silicon or bonding III–V to a silicon substrate has been utilized. The more commonly used bonding technology requires smooth surfaces, extra transfer and substrate removal processes and may encounter bubble or low thermal conductivity problems [2]. In comparison to bonding technique, direct epitaxial growth is a more straightforward wafer-level solution for low-cost mass production, if challenges of the hetero-growth can be properly managed. Direct growth takes advantages of the availability of large wafer sizes, good thermal conductivity and the mechanical robustness of Si substrates.

Monolithic integration of photodetectors with Si circuits for telecommunications or with other photonic components for optical interconnections at the optical wavelength of 1.55 $\mu$m is an attractive subject. Direct growth of device-quality III–V photodetectors on the Si platform has been of particular interest. Bartels et al. [3] have demonstrated a 1.5GHz metal-semiconductor-metal InGaAs photodetector grown on Si substrates. Recently, p-i-n InGaAs/Si photodetectors with a dark current of 1 $\mu$A, a responsivity of 0.34 A/W at 1.55 $\mu$m and an open eye pattern at 10 Gb/s have been reported [4]. These devices were grown by a combination of molecular beam epitaxy (MBE) and MOCVD, which is rather complicated and not the optimal for mass production. P-I-N Ge/Si photodetectors emerge in recent years and seem to be a serious contender to InGaAs/Si photodetectors [5-6]. In this work, high-performance top-illuminated p-i-n InGaAs photodetectors grown on Si substrates by MOCVD are demonstrated. III–V based alternatives for active devices will be available for silicon photonic circuit designers in choosing components with specific performance or material requirements.

| P contact: $p^+$ GaAsSb, $2\times10^{19}/cm^3$, 160 nm |
|---|
| Absorption layer: UID InGaAs, 850 nm |
| N contact: $n^+$ InP, $5\times10^{18}/cm^3$, 150 nm |
| InP buffer: 400 nm |
| Strain layer stacks: InGaAs/InP, 110 nm |
| InP buffer: 1000 nm |
| GaAs buffer: 500 nm |
| Si substrate |

Fig. 1. Layer structure of the p-i-n InGaAs photodetectors on silicon substrates grown by MOCVD.

## II. Growth and Fabrications

A schematic representation of the layer structure for the p-i-n InGaAs/Si photodetectors is shown in Fig. 1.

All the epitaxial layers were grown on a 4-inch p-type (100)-oriented Si substrate in an AIXTRON 200/4 system [7]. To alleviate the 8% lattice mismatch between InP and Si, a 500 nm thick GaAs buffer layer and an 1000 nm InP buffer layer were grown on the Si substrate, using a two-temperature growth technique. The sources used were standard trimethylgallium, arsine, trimethylindium, and phosphine. The low temperature (LT) GaAs nucleation layer was grown at 450 °C and the optimized thickness and V/III ratio were 10nm and 200. The epitaxial high temperature (HT) GaAs layer was grown at 650 °C with a V/III ratio of 40. The LT-

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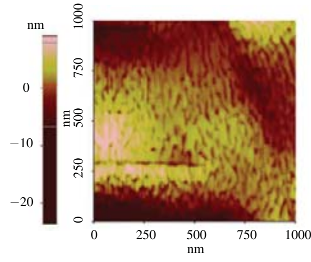

Fig. 2. AFM image of a $1 \times 1$ $\mu m^2$ scanned area on the surface of a detector structure grown on a silicon substrate.

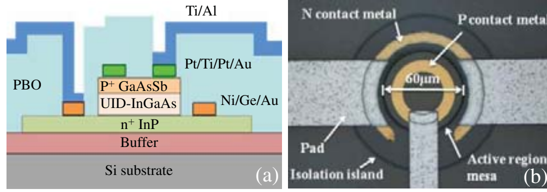


Fig. 3. (a) Cross-sectional view of the p-i-n InGaAs photodetector on a silicon substrate. (b) Microscope image of the p-i-n InGaAs photodetector (60-$\mu$m diameter) after processing.

InP and HT-InP buffers were grown at 450 °C and 600 °C, respectively. Then cyclic thermal annealing between 300 °C and 650 °C was carried out to improve the crystalline quality. Strain-balancing layer stacks (SLS) with 5 periods of $In_{0.59}Ga_{0.41}As/InP$ were inserted to block the dislocations and help relieve stress during the cooling down period. After inserting another 400 nm InP buffer, the p-i-n structure was grown on top, which included 160nm p+ $GaAs_{0.51}Sb_{0.49}$, 850nm unintentionally doped (UID) $In_{0.53}Ga_{0.47}As$ and 150nm n+ InP layers. P-GaAsSb was used instead of p-InGaAs because the process required was established and easier to be realized in our system. Atomic force microscopy (AFM) was used to characterize the surface morphology. Figure 2 shows an AFM micrograph of a typical detector structure. The Root Mean Square (RMS) value of the surface roughness is 3.5 nm across a scanned area of $1 \times 1$ $\mu m^2$.

Top-illuminated circular devices with various active areas (60, 40, 30, and 20$\mu$m diameters) were fabricated. A cross-sectional schematic of the mesa-type p-i-n InGaAs photodetector and the microscope image of a 60$\mu$m-diameter device after processing are shown in Figs. 3(a) and (b).

The active region of the photodetector was defined by wet-etching of the p-GaAsSb and UID-InGaAs layers. Pt/Ti/Pt/Au and Ni/Ge/Au were deposited as the p and n ohmic contact metals. Devices were isolated by removing the n-InP and InP buffer layer above the SLS layers. High-resolution photo-definable polybenzobisoxazole (PBO) was used as the passivation layer to help suppress the dark current. Contact holes were opened by photolithography. After contact opening, Ti/Al was sputtered and the ground-signal-ground (GSG) pads were patterned for measurement. No anti-reflection coating was used.

## III. Device Characterization

Figure 4 shows the measured dark current and total current with optical input power of 4.8 mW at 1550nm for a 20$\mu$m photodetector and a 60$\mu$m photodetector. The top-illuminating

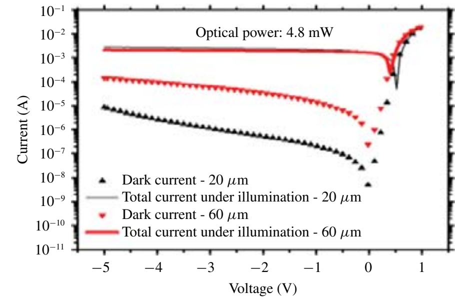


Fig. 4. Measured dark current and total current with optical input power of 4.8 mW at 1550 nm for photodetectors with diameters of 20 and 60 $\mu$m.

light was coupled to the optical windows of devices using a lensed single-mode fiber. Optical windows were defined by the inner ring of the p-contact metal. The lensed fiber was used to focus the laser beam to a 2$\mu$m-diameter spot. The dark current diminished with a reduction of the device area. The dark current reduction ratio of the 20$\mu$m device to the 60$\mu$m device was ~20 at −5V which exceeds the area reduction ratio of 9. Although it seems that the area reduction is effective to suppress the dark current, the explanation of the observed dark current reduction will require further device fabrications and experiments. A dark current of 0.2 $\mu$A at a reverse bias of 1V was obtained for the 20$\mu$m device. This corresponds to a current density of about 64mA/cm$^2$, which is comparable with the reported Ge/Si photodetectors [5-6]. The relatively large leakage current was a result of defects in the hetero-epitaxial growth that can be further minimized.

The total current was nearly flat across the reverse bias range starting from 0V to 5V, which indicates that significant built-in electric field existed in the InGaAs layer at zero bias. Photocurrent was obtained by subtracting the dark current from the total current under illumination. Both the 60$\mu$m and 20$\mu$m devices showed a relatively high responsivity of about 0.5 A/W at 1550nm with zero bias, and about 0.57 A/W with −5V bias. The responsivity at 0V corresponded to an external quantum efficiency of 40%. The calculated internal quantum efficiency of the 850nm InGaAs layer was 57% assuming the absorption coefficient of InGaAs at 1.55 $\mu$m to be $10^4$/cm [9]. We attribute this difference to the light reflection at the air/PBO and PBO/GaAsSb interfaces, absorption in PBO and GaAsSb layers and carrier recombination at the trap centers in the InGaAs layer and at the interfaces. The measured responsivity was flat across the wavelength range between 1510-1580nm, which is the available range of our tunable laser.

The radio frequency (RF) response was evaluated using an Agilent N5230A network analyzer. The RF signal was applied to a 15GHz $LiNbO_3$ modulator, and the modulated optical signal was fiber coupled to the photodetector under test. A 40G microwave probe was used to measure the photodetector output. The frequency response of the devices was calibrated using a commercial 40GHz photodetector.

We have fabricated two batches of devices. For devices from the first process batch, a limited optical 3dB bandwidth of ~2 GHz was measured for all sizes of devices. Their speed was limited by the large parasitic capacitance between the p signal electrode pad and the conductive ground substrate.

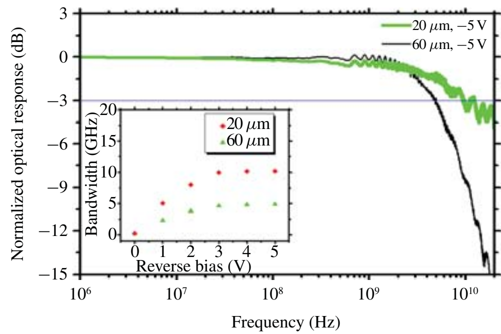


Fig. 5. Measured frequency response for the 20-$\mu$m photodetector and 60-$\mu$m photodetector at −5 V. Inset: 3dB bandwidth versus reverse bias of the 20-$\mu$m and 60-$\mu$m devices.

This capacitance is estimated to be 1.8 pF, which is much larger than the estimated junction capacitance of the 20$\mu$m device (0.04 pF).

Because of the conductive silicon substrate used, it was not possible to obtain small parasitic capacitance by putting the large pads on the substrate as typically done on semi-insulating substrates. Thus, in the second process batch, the PBO thickness was increased from 1.5$\mu$m to 1.9$\mu$m and the pad size was reduced from 500$\mu$m × 200$\mu$m to about 100$\mu$m × 100$\mu$m. Figure 5 shows the normalized optical response versus frequency for the 60$\mu$m and 20$\mu$m devices at −5V. The 3dB bandwidth increases with smaller device, showing the size effect. The optical bandwidth of the 20$\mu$m device was 10 GHz and that of the 60$\mu$m device was 5 GHz. The corresponding electrical bandwidths were 6.3 GHz and 3.2 GHz. The inset shows the measured bandwidth as a function of reverse bias for the 60$\mu$m and 20$\mu$m devices. The bandwidth saturated at a reverse bias of 3V. An optical bandwidth exceeding 2 GHz was obtained for the 60$\mu$m device and about 5 GHz was obtained for the 20$\mu$m device at −1V.

As in common PIN diodes, the lifetime of photo-generated carriers in the p-GaAsSb layer was short due to the high doping level of $>10^{19}$ cm$^{-3}$. The 3dB bandwidth was mainly determined by the carrier transit time in the InGaAs layer and the resistance-capacitance (RC) time constant of the device and peripheral components. The electrical bandwidths of the 20$\mu$m and 60$\mu$m devices were calculated to be 8.6 GHz and 4.1 GHz [10] with the estimated parasitic capacitance $C_p$ of 0.2pF. These values are close to the measured results. $C_p$ was also extracted by fitting the calculated reflection coefficient $S_{22}$ from the small-signal equivalent circuit [11] with a measured $S_{22}$. The extracted value was 0.21 pF, which is consistent with the estimated value of 0.2pF.

For the 20$\mu$m device, an estimated 83% of the capacitance came from the parasitic capacitance between the pad and the substrate. The response of the small device can be made closer to the transit-time-limited bandwidth by growing photodetectors on high-resistivity silicon substrates or Silicon-On-Insulator (SOI) substrates. In the future, we will use high-resistivity silicon or SOI wafers instead of standard p-type Si wafers. The RC-limited bandwidth can also be greatly improved in integrated circuits as large pads are not used.

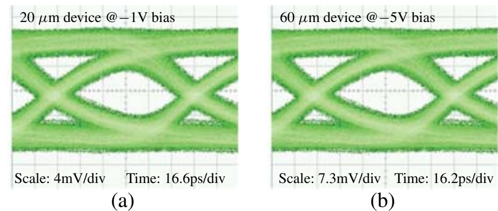


Fig. 6. Measured eye diagrams at 10 Gb/s for (a) 20-$\mu$m photodetector at −1 V. (b) 60-$\mu$m photodetector at −5 V.

10Gb/s non-return-to-zero (NRZ) eye pattern was measured to ensure the InGaAs/Si detector could be used in 10Gb/s data transmission link. The RF signal from a pseudo-random bit sequence (PRBS) generator with $2^{10} - 1$ pattern length was used to modulate the 1550nm light through a 10Gb/s $LiNbO_3$ modulator. Open eyes were observed for 20$\mu$m devices biased at −1V and 60$\mu$m devices biased at −5V. Figure 6 shows the measured eye diagrams at 10Gb/s for the 20$\mu$m device with −1V and the 60$\mu$m device with −5V bias.

## IV. Conclusion

In conclusion, we have demonstrated high-speed normal-incidence p-i-n InGaAs photodetectors epitaxially grown on silicon substrates by MOCVD. Dark current diminishes and 3dB bandwidth increases with a reduction of the device area. Parasitic capacitance between the pad and the conductive silicon substrate is a limiting factor of the RF response. Growing waveguide InGaAs photodetectors on SOI wafers is likely to result in a lower dark current and a higher speed due to compact waveguide device sizes with a smaller parasitic capacitance.

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